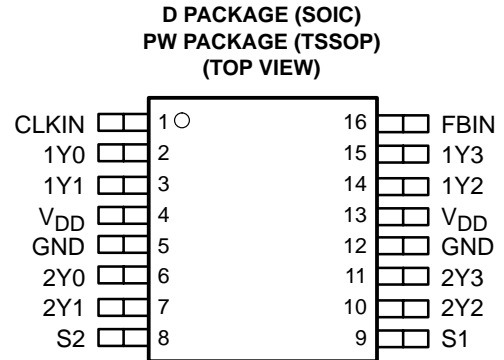


CDCVF25081

3.3-V PHASED-LOCK LOOP CLOCK DRIVER

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

- Phase-Locked Loop-Based Zero-Delay Buffer
- Operating Frequency: 8 MHz to 200 MHz
- Low Jitter (Cycle-Cycle): ± 100 ps Over the Range 66 MHz to 200 MHz
- Distributes One Clock Input to Two Banks of Four Outputs
- Auto Frequency Detection to Disable Device (Power Down Mode)
- Consumes Less Than 20 μ A in Power Down Mode
- Operates From Single 3.3-V Supply
- Industrial Temperature Range -40°C to 85°C
- 25- Ω On-Chip Series Damping Resistors
- No External RC Network Required
- Spread Spectrum Clock Compatible (SSC)
- Available in 16-Pin TSSOP or 16-Pin SOIC Packages



description

The CDCVF25081 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal. The CDCVF25081 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Two banks of four outputs each provide low-skew, low-jitter copies of CLKIN. All outputs operate at the same frequency. Output duty cycles are adjusted to 50%, independent of duty cycle at CLKIN. The device automatically goes into power-down mode when no input signal is applied to CLKIN and the outputs go into a low state. Unlike many products containing PLLs, the CDCVF25081 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost.

Because it is based on a PLL circuitry, the CDCVF25081 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKIN and any following changes to the PLL reference.

The CDCVF25081 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

S2	S1	1Y0–1Y3	2Y0–2Y3	OUTPUT SOURCE	PLL SHUTDOWN
0	0	Hi-Z	Hi-Z	N/A.	Yes
0	1	Active	Hi-Z	PLL [†]	No
1	0	Active	Active	Input clock (PLL bypass)	Yes
1	1	Active	Active	PLL [†]	No

[†] CLK input frequency < 2 MHz switches the outputs to low level



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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CDCVF25081

3.3-V PHASED-LOCK LOOP CLOCK DRIVER

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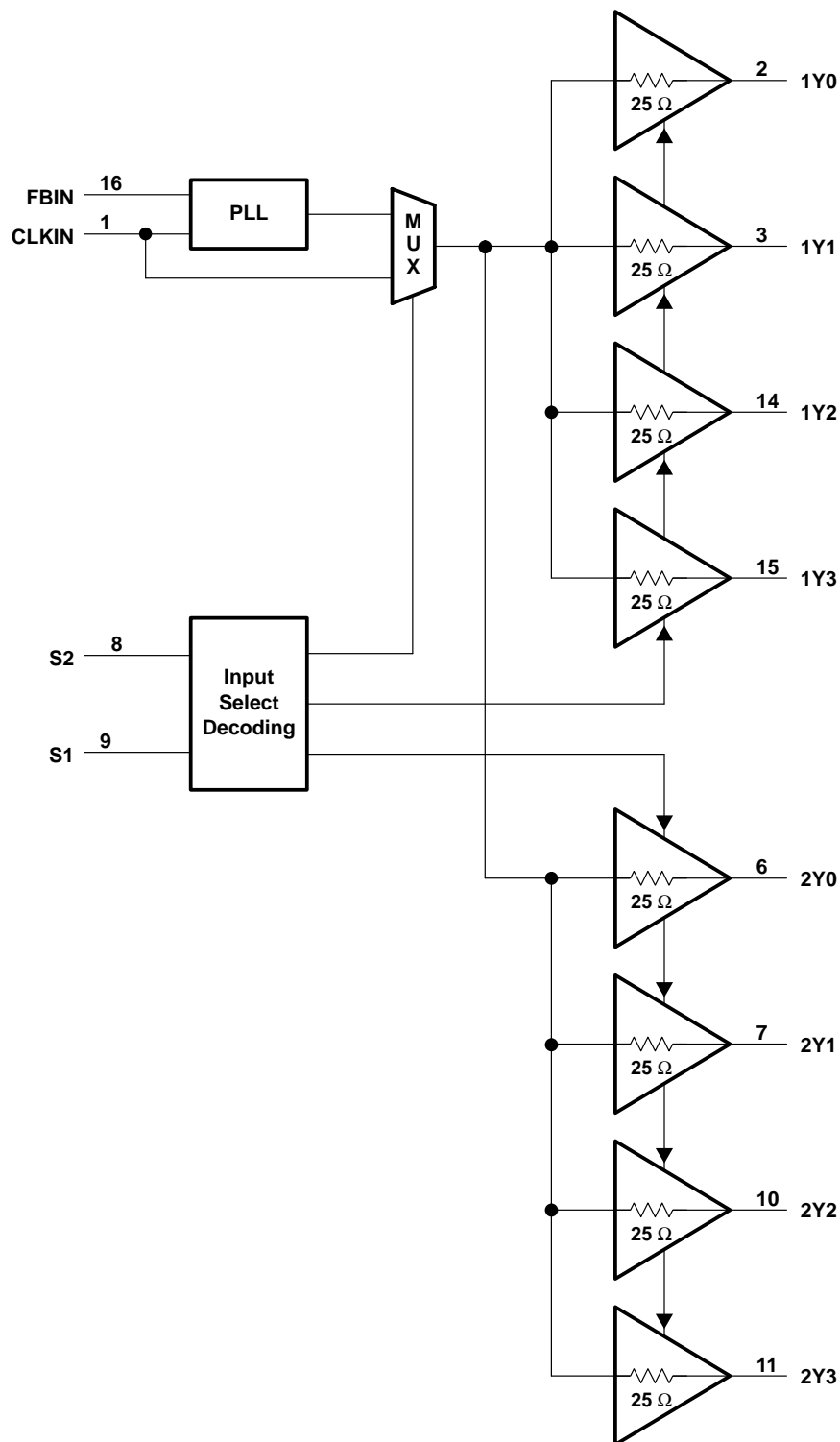
Terminal Functions

TERMINAL NAME	PIN NO.	TYPE	DESCRIPTION
1Y[0:3]	2, 3, 14, 15	O	Bank 1Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.
2Y[0:3]	6, 7, 10, 11	O	Bank 2Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF25081 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the output signal. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN.
FBIN	16	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock.
GND	5, 12	Ground	Ground
S1, S2	9, 8	I	Select pins to determine mode of operation. See the <i>FUNCTION TABLE</i> for mode selection options.
V _{DD}	4, 13	Power	Supply voltage. The supply voltage range is 3 V to 3.6 V



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functional block diagram



CDCVF25081

3.3-V PHASED-LOCK LOOP CLOCK DRIVER

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Input voltage range, V_I (see Notes 1 and 2)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{DD} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous total output current, I_O ($V_O = 0$ to V_{DD})	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package	147°C/W
D package	112°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Low level input voltage, V_{IL}			0.8	V
High level input voltage, V_{IH}	2			V
Input voltage, V_I	0		3.6	V
High-level output current, I_{OH}			–12	mA
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	–40		85	°C

timing requirements over recommended ranges of supply voltage, load and operating free-air temperature

		MIN	NOM	MAX	UNIT
Clock frequency, f_{clk}	$C_L = 25$ pF	8		100	MHz
	$C_L = 15$ pF	66		200	



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	Input voltage	V _{DD} = 3 V, I _I = -18 mA			-1.2	V
I _I	Input current	V _I = 0 V or V _{DD}			±5	μA
I _{PD} ‡	Power down current	f _{CLKIN} = 0 MHz, V _{DD} = 3.3 V			20	μA
I _{OZ}	Output 3-state	V _O = 0 V or V _{DD} , V _{DD} = 3.6 V			±5	μA
C _I	Input capacitance at FBIN, CLKIN	V _I = 0 V or V _{DD}		4		pF
C _I	Input capacitance at S1, S2	V _I = 0 V or V _{DD}		2.2		pF
C _O	Output capacitance	V _I = 0 V or V _{DD}		3		pF
V _{OH}	High-level output voltage	V _{DD} = min to max, I _{OH} = -100 μA	V _{DD} - 0.2			V
		V _{DD} = 3 V, I _{OH} = -12 mA	2.1			
		V _{DD} = 3 V, I _{OH} = -6 mA	2.4			
V _{OL}	Low-level output voltage	V _{DD} = min to max, I _{OL} = 100 μA	0.2			V
		V _{DD} = 3 V, I _{OL} = 12 mA	0.8			
		V _{DD} = 3 V, I _{OL} = 6 mA	0.55			
I _{OH}	High-level output current	V _{DD} = 3 V, V _O = 1 V	-24			mA
		V _{DD} = 3.3 V, V _O = 1.65 V	-30			
		V _{DD} = 3.6 V, V _O = 3.135 V	-15			
I _{OL}	Low-level output current	V _{DD} = 3 V, V _O = 1.95 V	26			mA
		V _{DD} = 3.3 V, V _O = 1.65 V	33			
		V _{DD} = 3.6 V, V _O = 0.4 V	14			

† All typical values are at respective nominal V_{DD}.

‡ For I_{DD} over frequency see Figure 7.

CDCVF25081

3.3-V PHASED-LOCK LOOP CLOCK DRIVER

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{\text{(lock)}}$	PLL lock time	$f = 100 \text{ MHz}$		10		μs
$t_{\text{(phoffset)}}$	Phase offset (CLKIN to FBIN)	$f = 8 \text{ MHz to } 66 \text{ MHz},$ $V_{\text{th}} = V_{\text{DD}}/2$ (see Note 5)	-200		200	ps
		$f = 66 \text{ MHz to } 200 \text{ MHz},$ $V_{\text{th}} = V_{\text{DD}}/2$ (see Note 5)	-150		150	
t_{PLH}	Low-to-high level output propagation delay	$S2 = \text{High},$ $S1 = \text{Low (PLL bypass)}$	2.5		6	ns
t_{PHL}	High-to-low level output propagation delay	$f = 1 \text{ MHz},$ $C_L = 25 \text{ pF}$				
$t_{\text{sk(o)}}$	Output skew (Y_n to Y_n) (see Note 4)				150	ps
$t_{\text{sk(pp)}}$	Part-to-part skew	$S2 = \text{high},$ $S1 = \text{high (PLL mode)}$			600	ps
		$S2 = \text{high},$ $S1 = \text{low (PLL bypass)}$			700	
$t_{\text{jit(cc)}}$	Jitter (cycle-to-cycle)	$f = 66 \text{ MHz to } 200 \text{ MHz}, C_L = 15 \text{ pF}$			± 100	ps
		$f = 66 \text{ MHz to } 100 \text{ MHz}, C_L = 25 \text{ pF}$ $f = 8 \text{ MHz to } 66 \text{ MHz}$ (see Figure 6)			± 150	
odc	Output duty cycle	$f = 8 \text{ MHz to } 200 \text{ MHz}$	43%		57%	
$t_{\text{sk(p)}}$	Pulse skew	$S2 = \text{High},$ $S1 = \text{low (PLL bypass)}$ $f = 1 \text{ MHz},$ $C_L = 25 \text{ pF}$			0.7	ns
t_r	Rise time rate	$C_L = 15 \text{ pF},$ See Figure 4	0.8		3.3	V/ns
		$C_L = 25 \text{ pF},$ See Figure 4	0.5		2	
t_f	Fall time rate	$C_L = 15 \text{ pF},$ See Figure 4	0.8		3.3	V/ns
		$C_L = 25 \text{ pF},$ See Figure 4	0.5		2	

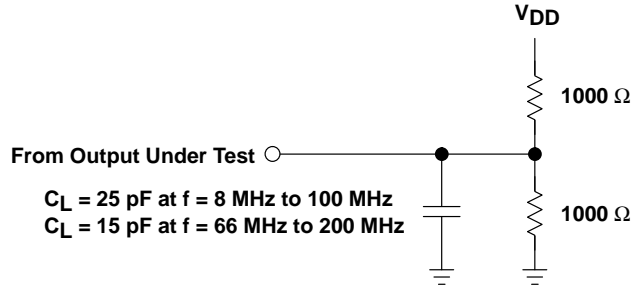
† All typical values are at respective nominal V_{DD} .

NOTES: 4. The $t_{\text{sk(o)}}$ specification is only valid for equal loading of all outputs.

5. Similar waveform at CLKIN and FBIN are required. For phase displacement between CLKIN and Y-outputs see Figure 5.



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $Z_O = 50 \Omega$, $t_r < 1.2 \text{ ns}$, $t_f < 1.2 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Test Load Circuit

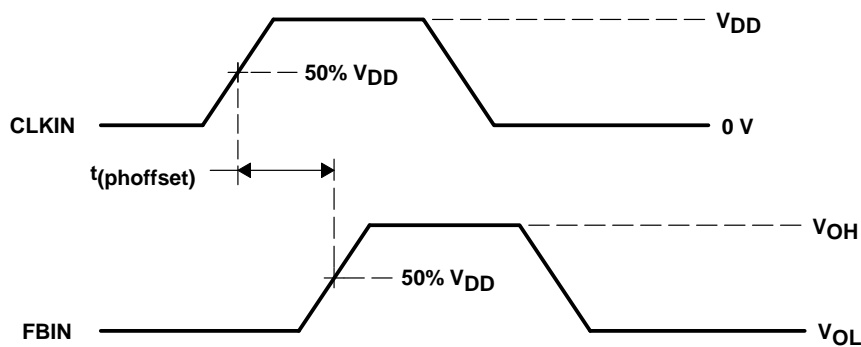
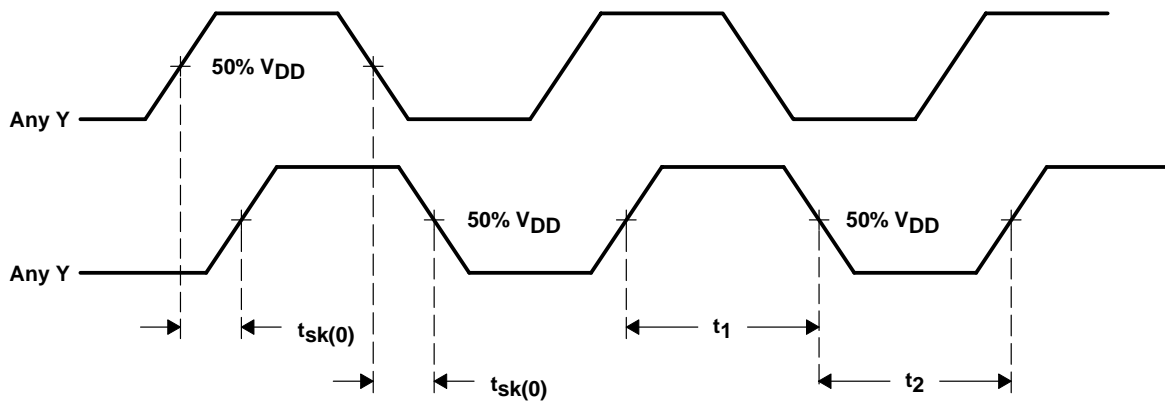


Figure 2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)



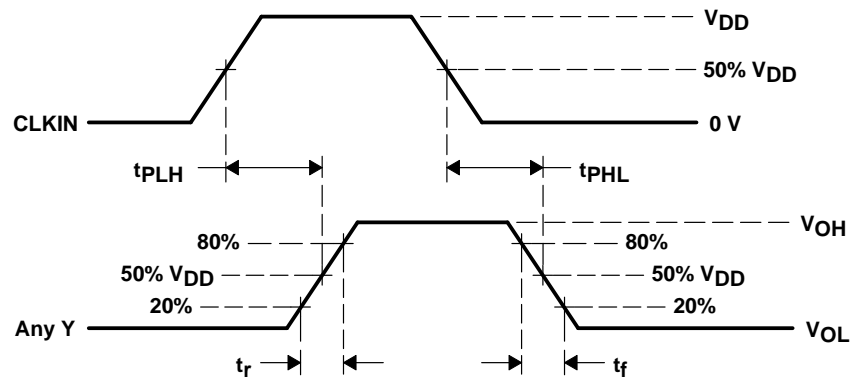
NOTE: $\text{odc} = t_1 / (t_1 + t_2) \times 100\%$

Figure 3. Output Skew and Output Duty Cycle (PLL Mode)

CDCVF25081
3.3-V PHASED-LOCK LOOP CLOCK DRIVER

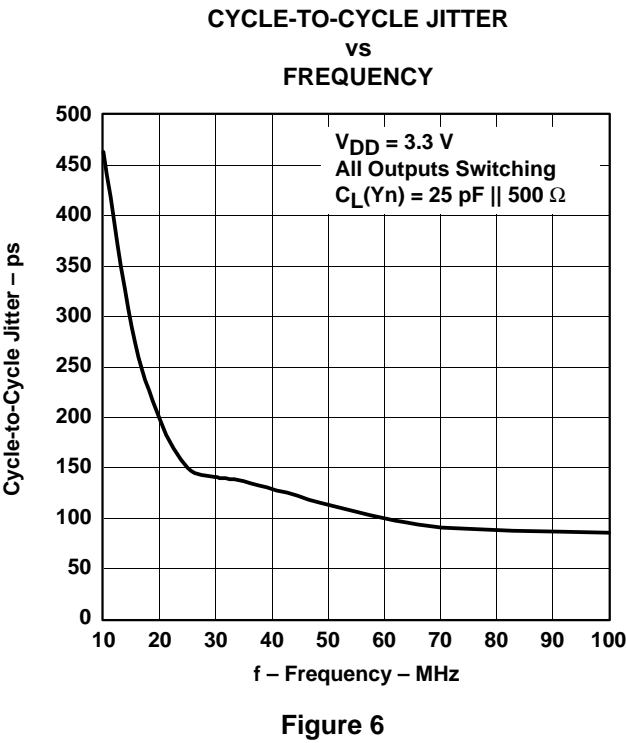
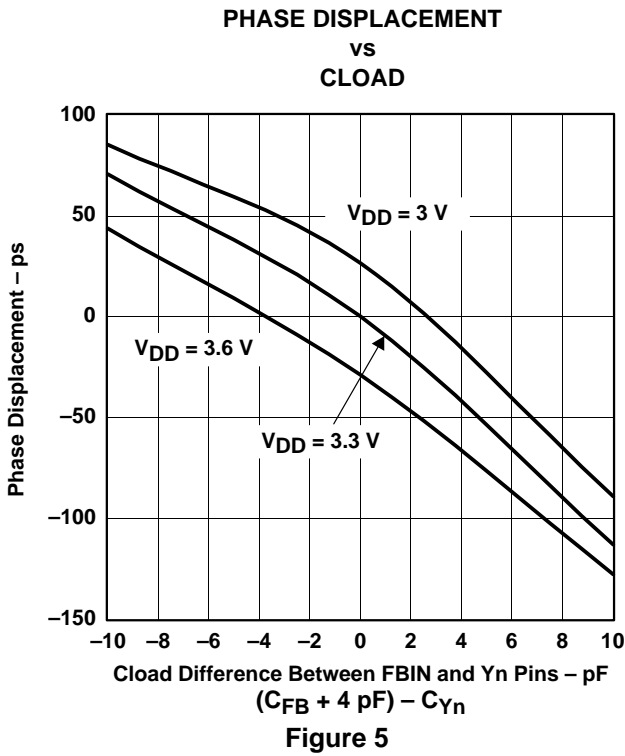
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PARAMETER MEASUREMENT INFORMATION

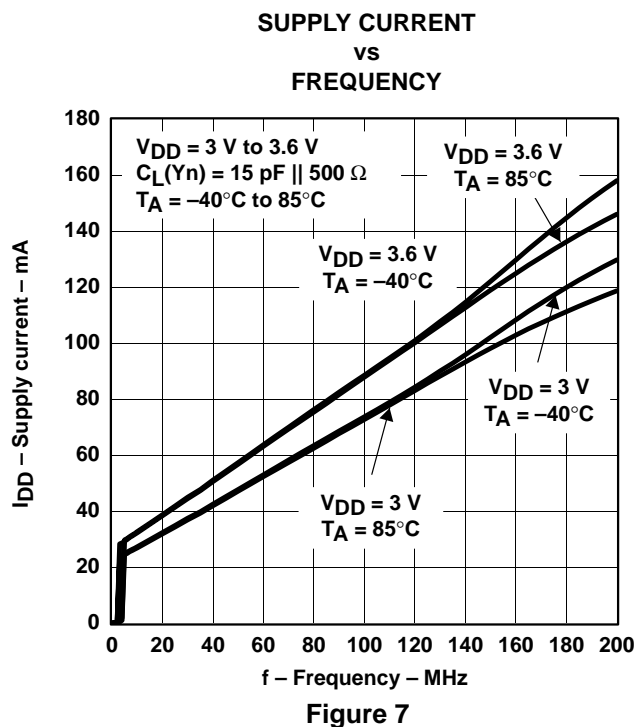


NOTE: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 4. Propagation Delay and Pulse Skew (Non-PLL Mode)



PARAMETER MEASUREMENT INFORMATION



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF25081D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF25081DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CDCVF25081PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF25081DR	SOIC	D	16	2500	350.0	350.0	43.0
CDCVF25081PWR	TSSOP	PW	16	2000	853.0	449.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

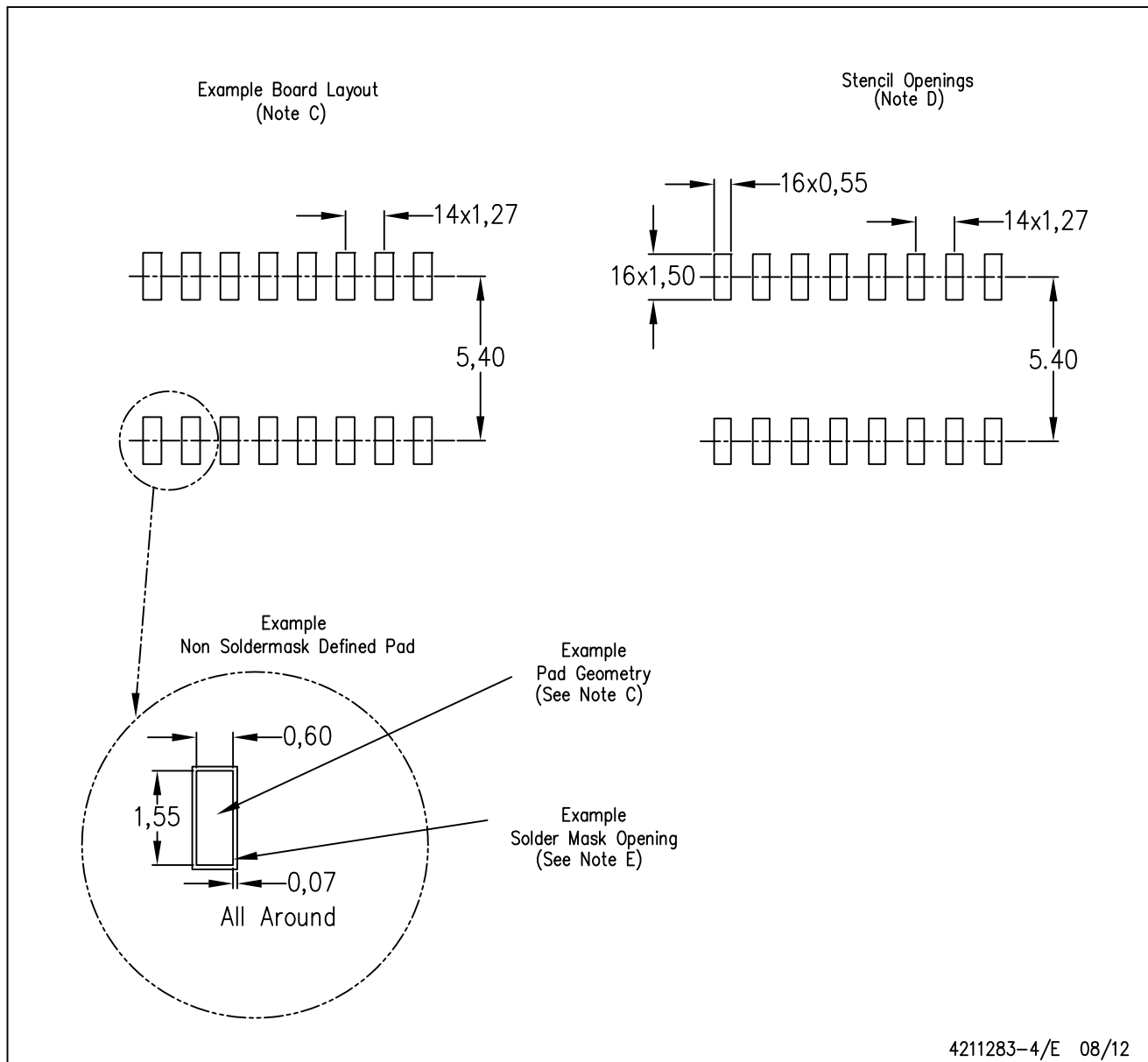


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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NOTES:

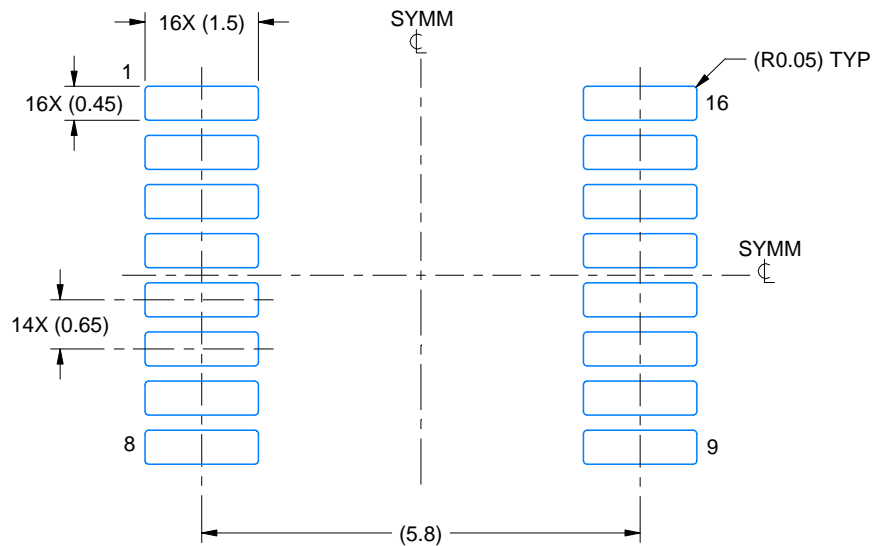
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

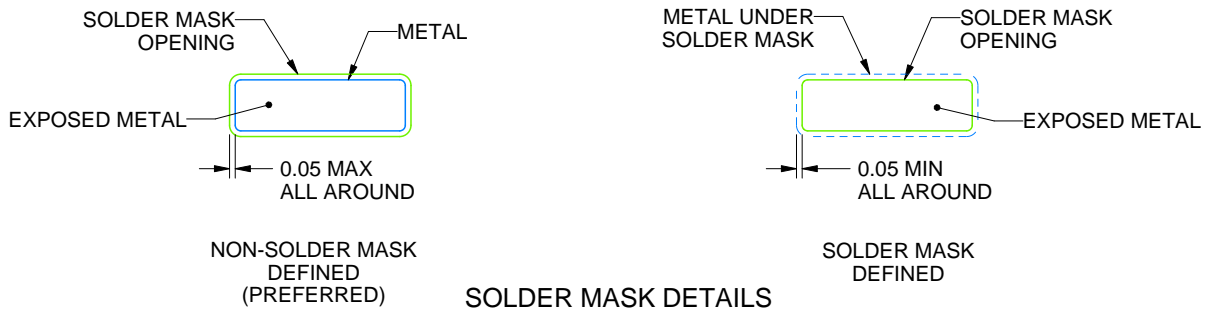
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

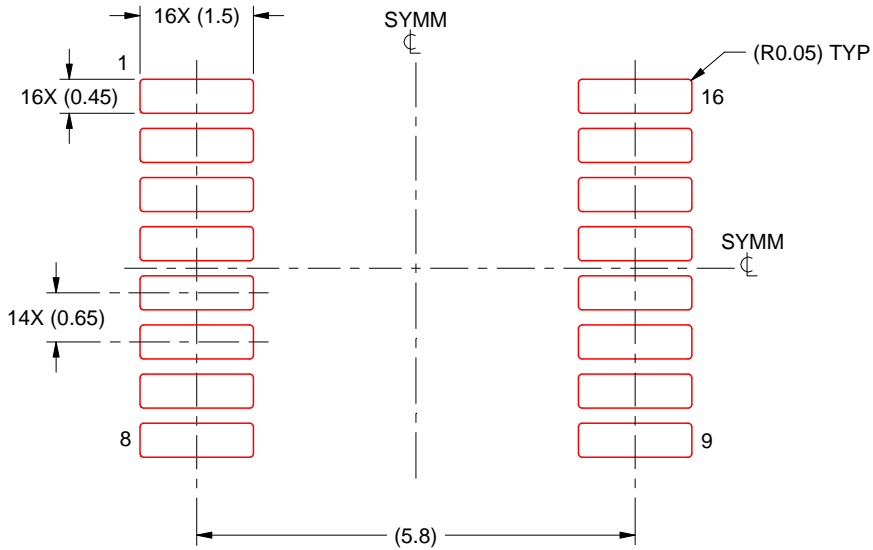
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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