TPS22990 5.5-V, 10-A, 3.9-mΩ On-Resistance Load Switch

1 Features

- Integrated Single Channel Load Switch
- VBIAS Voltage Range: 2.5 V to 5.5 V
- VIN Voltage Range: 0.6 V to V_{BIAS}
- On-Resistance
  - R_{ON} = 3.9 mΩ (typical) at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 3.9 mΩ (typical) at V_{IN} = 3.3 V (V_{BIAS} = 3.3 V)
- 10-A Maximum Continuous Switch Current
- Quiescent Current
  - $I_{Q,VBIAS}$ = 63 µA at V_{BIAS} = 5 V
- Shutdown Current
  - $I_{SD,VBIAS}$ = 5.5 µA at V_{BIAS} = 5 V
  - $I_{SD,VIN}$ = 4 nA at V_{BIAS} = 5 V, V_{IN} = 5 V
- Controlled and Adjustable Slew Rate through CT
- Power Good (PG) Indicator
- Quick Output Discharge (QOD) (TPS22990 Only)
- 3-mm × 2-mm SON 10-pin Package with Thermal Pad
- ESD Performance Tested per JESD 22
  - 2-kV HBM and 1-kV CDM

2 Applications

- Notebooks, Chromebooks and Tablets
- Desktop PC and Industrial PC
- Solid State Drives (SSDs)
- Servers
- Telecom systems

3 Description

The TPS22990 product family consists of two devices: TPS22990 and TPS22990N. Each device is a 3.9-mΩ, single-channel load switch with a controlled and adjustable turn on and integrated PG indicator.

The devices contain an N-channel MOSFET that can operate over an input voltage range of 0.6 V to 5.5 V and can support a maximum continuous current of 10 A. The wide input voltage range and high current capability enable the devices to be used across multiple designs and end equipments. 3.9-mΩ On-resistance minimizes the voltage drop across the load switch and power loss from the load switch.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through CT provides the design flexibility to trade off inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

The TPS22990 has an optional 218-Ω On-chip resistor for quick discharge of the output when switch is disabled to avoid any unknown state caused by floating supply to the downstream load.

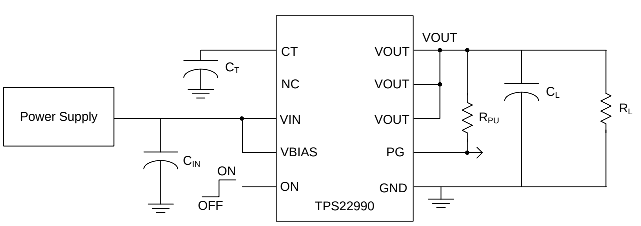
The TPS22990 is available in a small, space-saving 3-mm × 2-mm 10-SON package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Device Information(1)

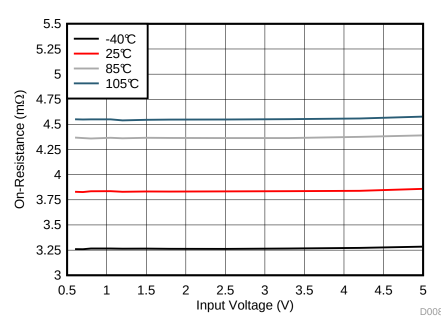
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22990 TPS22990N	WSON (10)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



On-Resistance vs Input Voltage



V_{BIAS} = 5 V, I_{OUT} = –200 mA

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4 Revision History

Changes from Revision B (September 2016) to Revision C **Page**

- Updated V_{IH} in *Recommended Operating Conditions* ... 4

Changes from Revision A (July 2016) to Revision B **Page**

- Removed the status column from *Device Comparison Table* ... 3
- Added the comment “(TPS22990 Only)” to the “R_{PD}” cell in both *Electrical Characteristics* tables ... 7

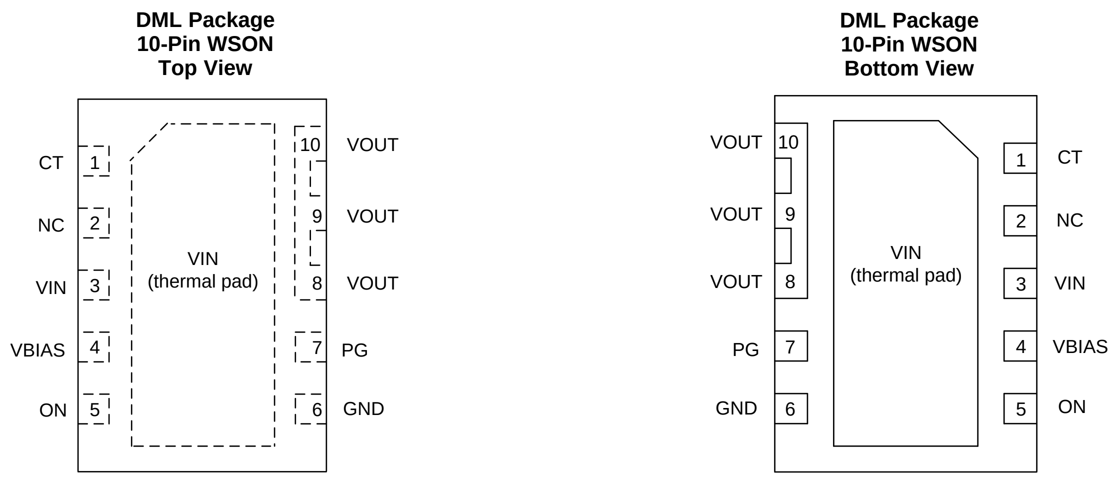
Changes from Original (May 2016) to Revision A **Page**

- Changed device status from *Product Preview* to *Production Data* ... 1

5 Device Comparison Table

DEVICE	R_{ON} at V_{BIAS} = 5 V	QOD	I_{MAX}	ENABLE
TPS22990	3.9 mΩ	Yes	10 A	Active high
TPS22990N	3.9 mΩ	No	10 A	Active high

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CT	O	VOUT slew rate control
2	NC	—	Not internally connected
3	VIN	I	Switch input. Bypass this input with a ceramic capacitor to GND
4	VBIAS	P	Bias voltage. Power supply to the device
5	ON	I	Active high switch control input. Do not leave floating
6	GND	GND	Device ground
7	PG	O	Power good. Active high, open drain output. Tie to GND if not used
8	VOUT	O	Switch output
9			
10			
—	VIN (Thermal Pad)	I	Switch input. VIN and thermal pad (exposed center pad) to alleviate thermal stress. See the *Layout* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	ON voltage	–0.3	6	V
V_{PG}	PG voltage	–0.3	6	V
V_{CT}	CT voltage	–0.3	15	V
I_{MAX}	Maximum continuous switch current at T_J = 125°C		10	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		12	A
T_J	Maximum junction temperature		125	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.6	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.5	V
V_{OUT}	Output voltage			VIN	V
V_{ON}	ON voltage		0	5.5	V
V_{PG}	PG voltage		0	5.5	V
$V_{IH, ON}$	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5 V, T_A< 85°C	1.05	5.5	V
		V_{BIAS} = 2.5 V to 5.5 V, T_A< 105°C	1.2	5.5	
$V_{IL, ON}$	Low-level input voltage, ON		0	0.5	V
C_{IN}	Input capacitor		1(1)		µF
T_A	Operating free-air temperature		–40	105	°C

(1) See the *Application Information* section.

7.4 Thermal Information

THERMAL METRIC[1]		TPS22990 DML (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temp –40°C ≤ T_A ≤ +105°C (full) and V_{BIAS} = 5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q,\ VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0 A, V_{IN} = V_{ON} = 5 V		–40°C to +85°C		63	76	µA
				–40°C to +105°C			77	
$I_{SD,\ VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V		–40°C to +85°C		5.5	7	µA
				–40°C to +105°C			7	
$I_{SD,\ VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		0.004	4	µA
				–40°C to +105°C			10	
			V_{IN} = 3.3 V	–40°C to +85°C		0.003	3	
				–40°C to +105°C			7	
			V_{IN} = 2.5 V	–40°C to +85°C		0.002	2	
				–40°C to +105°C			5	
			V_{IN} = 1.8 V	–40°C to +85°C		0.002	2	
				–40°C to +105°C			4	
			V_{IN} = 1.05 V	–40°C to +85°C		0.001	1	
				–40°C to +105°C			3	
			V_{IN} = 0.6 V	–40°C to +85°C		0.001	1	
				–40°C to +105°C			2	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
$V_{HYS,ON}$	ON pin hysteresis	V_{IN} = 5 V		25°C		123		mV
$I_{PG,\ LKG}$	Leakage current into PG pin	V_{PG} = 5 V		–40°C to +105°C			0.5	µA
$V_{PG,OL}$	PG output low voltage	V_{ON} = 0 V, I_{PG} = 1 mA		–40°C to +105°C			0.2	V
RESISTANCE CHARACTERISTICS								

Electrical Characteristics—V_{BIAS} = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temp –40°C ≤ T_A ≤ +105°C (full) and V_{BIAS} = 5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	On-state resistance	I_{OUT} = –200 mA, V_{ON} = 5 V	V_{IN} = 5 V	25°C		3.9	4.8	mΩ
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 3.3 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 2.5 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 1.8 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 1.05 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 0.6 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
R_{PD}	Output pull-down resistance (TPS22990 Only)	V_{IN} = V_{OUT} = 5 V, V_{ON} = 0 V		–40°C to +105°C		218	253	Ω

7.6 Electrical Characteristics—V_{BIAS} = 3.3 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temp –40°C ≤ T_A ≤ +105°C (full) and V_{BIAS} = 3.3 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q,\ VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0 A, V_{IN} = V_{ON} = 3.3 V		–40°C to +85°C		48	58	µA
				–40°C to +105°C			59	
$I_{SD,\ VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V		–40°C to +85°C		4.5	6	µA
				–40°C to +105°C			7	
$I_{SD,\ VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 3.3 V	–40°C to +85°C		0.003	3	µA
				–40°C to +105°C			7	
			V_{IN} = 2.5 V	–40°C to +85°C		0.002	2	
				–40°C to +105°C			5	
			V_{IN} = 1.8 V	–40°C to +85°C		0.002	2	
				–40°C to +105°C			4	
			V_{IN} = 1.05 V	–40°C to +85°C		0.001	1	
				–40°C to +105°C			3	
			V_{IN} = 0.6 V	–40°C to +85°C		0.001	1	
				–40°C to +105°C			2	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
$V_{HYS,ON}$	ON pin hysteresis	V_{IN} = 3.3 V		25°C		100		mV
$I_{PG,\ LKG}$	Leakage current into PG pin	V_{PG} = 5 V		–40°C to +105°C			0.5	µA
$V_{PG,OL}$	PG output low voltage	V_{ON} = 0 V, I_{PG} = 1 mA		–40°C to +105°C			0.2	V
RESISTANCE CHARACTERISTICS								

Electrical Characteristics—V_{BIAS} = 3.3 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temp –40°C ≤ T_A ≤ +105°C (full) and V_{BIAS} = 3.3 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	On-state resistance	I_{OUT} = –200 mA, V_{ON} = 5 V	V_{IN} = 3.3 V	25°C		3.9	4.8	mΩ
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 2.5 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 1.8 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 1.05 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
			V_{IN} = 0.6 V	25°C		3.9	4.8	
				–40°C to +85°C			5.7	
				–40°C to +105°C			6	
R_{PD}	Output pull-down resistance (TPS22990 Only)	V_{IN} = V_{OUT} = 3.3 V, V_{ON} = 0 V		–40°C to +105°C		219	256	Ω

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		34		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		5.4		
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		31		
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		2.3		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		21		
$t_{PG,ON}$	PG turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		152		
$t_{PG,OFF}$	PG turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		1.3		
V_{IN} = 1.05 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		30		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		8		
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		13		
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		2.2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		24		
$t_{PG,ON}$	PG turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		134		
$t_{PG,OFF}$	PG turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		1.3		
V_{IN} = 0.6 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		29		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		8.8		
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		10		
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		2.2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		24		
$t_{PG,ON}$	PG turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		131		
$t_{PG,OFF}$	PG turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		1.3		

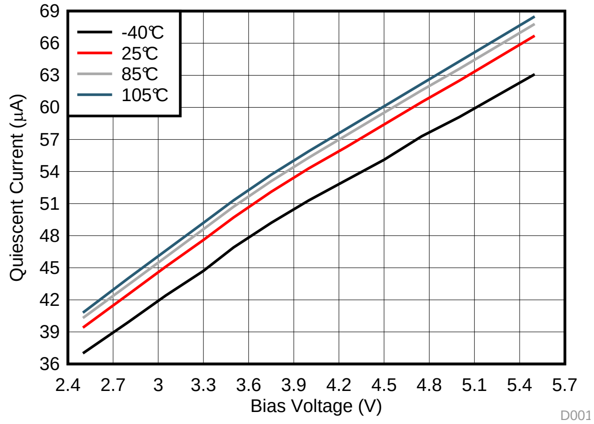
(1) Turnoff time and fall time are dependent on the time constant at the load. For TPS22990N, there is no QOD. The time constant is R_L×C_L. For TPS22990, internal pull down R_{PD} is enabled when the switch is disabled. The time constant is (R_{PD}//R_L)×C_L.

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

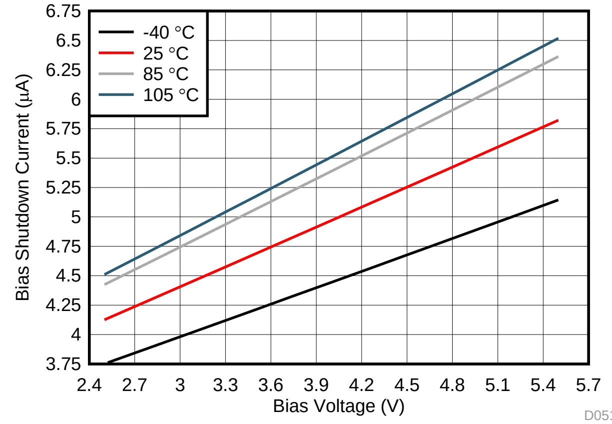
PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 3.3 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		33		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		6.2		µs
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		24		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		2.4		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		22		µs
$t_{PG,ON}$	PG turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		132		µs
$t_{PG,OFF}$	PG turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		1.5		µs
V_{IN} = 1.05 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		30		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		8.7		µs
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		12		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		2.3		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		24		µs
$t_{PG,ON}$	PG turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		122		µs
$t_{PG,OFF}$	PG turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		1.5		µs
V_{IN} = 0.6 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		30		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		9.4		µs
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		9		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		2.3		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		25		µs
$t_{PG,ON}$	PG turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		119		µs
$t_{PG,OFF}$	PG turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN}= 1 µF		1.5		µs

7.8 Typical Characteristics



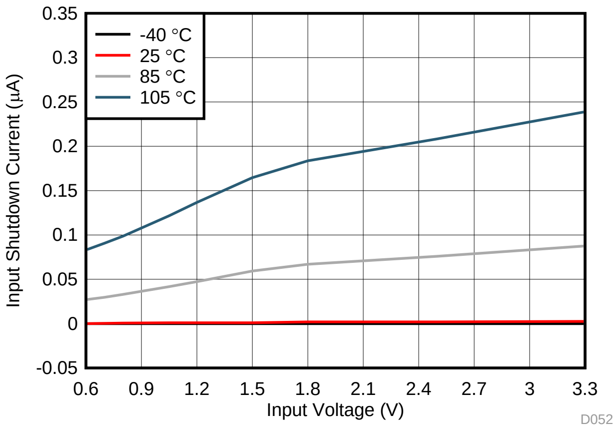
V_{ON} = 5 V I_{OUT} = 0 A V_{IN} = V_{BIAS}

Figure 1. Quiescent Current vs Bias Voltage



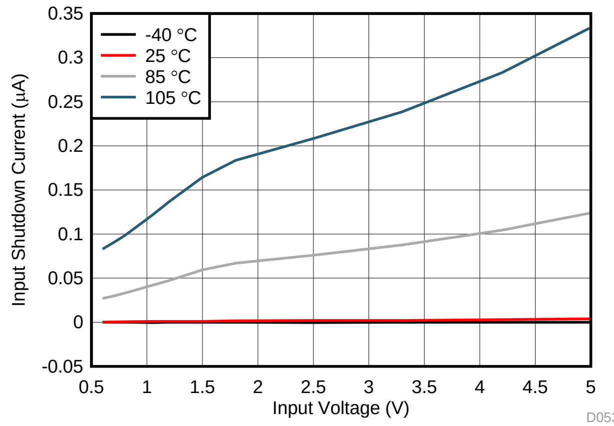
V_{ON} = 0 V V_{OUT} = 0 V V_{IN} = V_{BIAS}

Figure 2. Bias Shutdown Current vs Bias Voltage



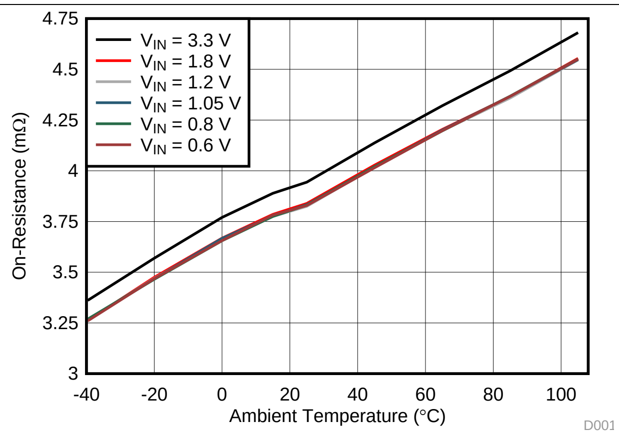
V_{ON} = 0 V V_{BIAS} = 3.3 V V_{OUT} = 0 V

Figure 3. Input Shutdown Current vs Input Voltage



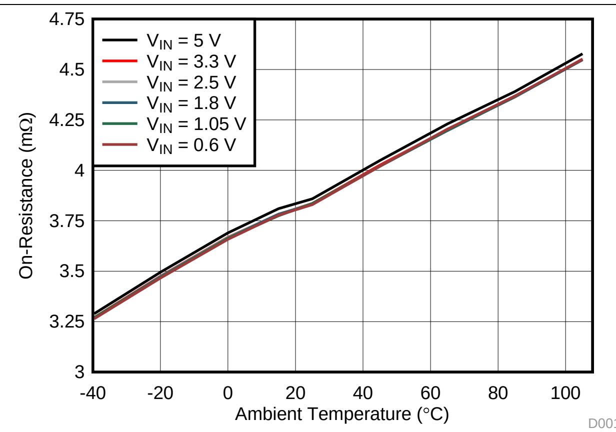
V_{ON} = 0 V V_{BIAS} = 5 V V_{OUT} = 0 V

Figure 4. Input Shutdown Current vs Input Voltage



V_{ON} = 5 V V_{BIAS} = 3.3 V I_{OUT} = –200mA

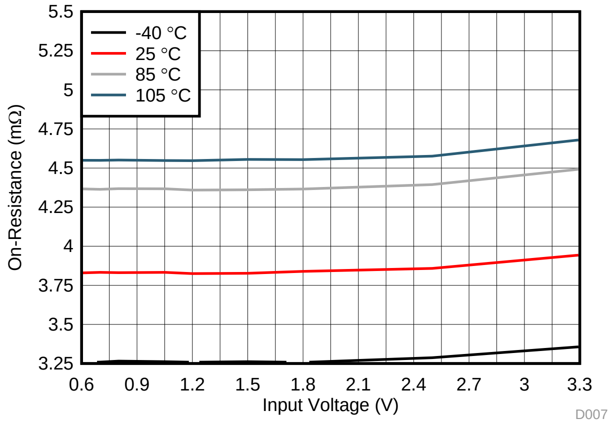
Figure 5. On-Resistance vs Ambient Temperature



V_{ON} = 5 V V_{BIAS} = 5 V I_{OUT} = –200mA

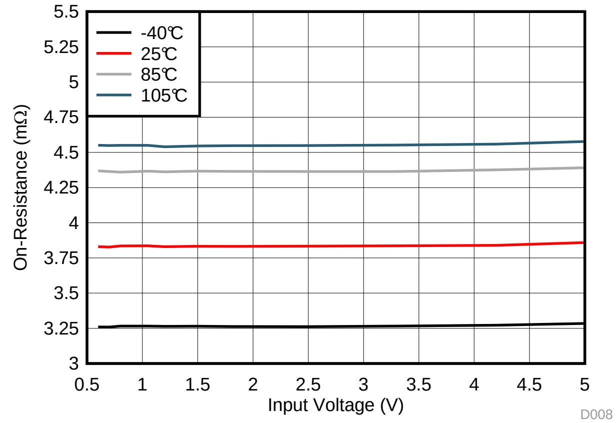
Figure 6. On-Resistance vs Ambient Temperature

Typical Characteristics (continued)



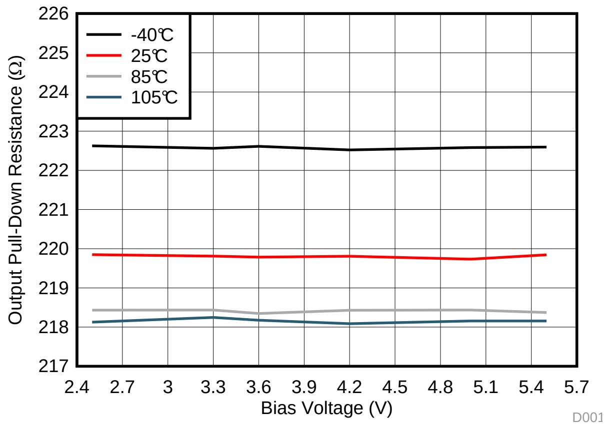
V_{ON} = 5 V V_{BIAS} = 3.3 V I_{OUT} = –200mA

Figure 7. On-Resistance vs Input Voltage



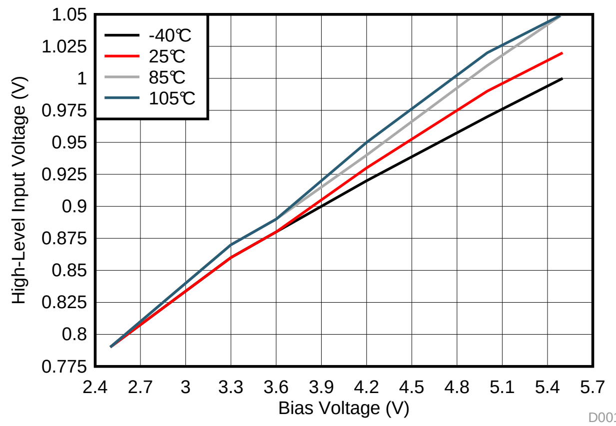
V_{ON} = 5 V V_{BIAS} = 5 V I_{OUT} = –200mA

Figure 8. On-Resistance vs Input Voltage



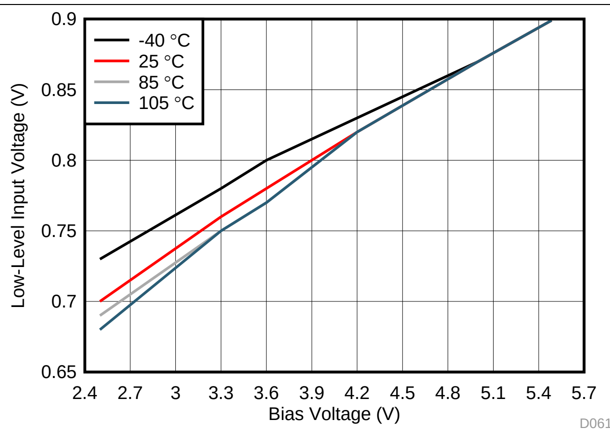
V_{ON} = 0 V V_{OUT} = V_{IN} = 1.05 V

Figure 9. Output Pull-Down Resistance vs Bias Voltage



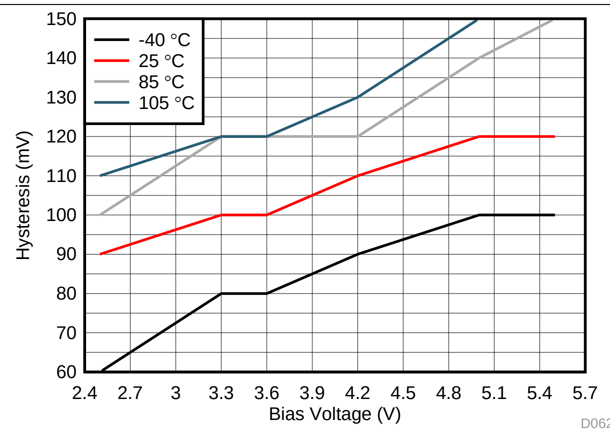
I_{OUT} = 0 A

Figure 10. High-Level Input Voltage vs Bias Voltage



I_{OUT} = 0 A

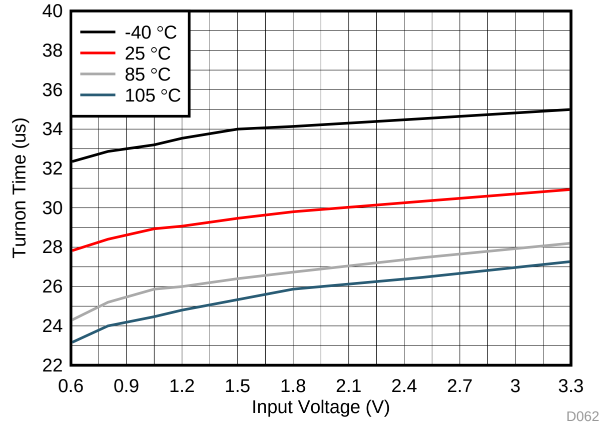
Figure 11. Low-Level Input Voltage vs Bias Voltage



I_{OUT} = 0 A

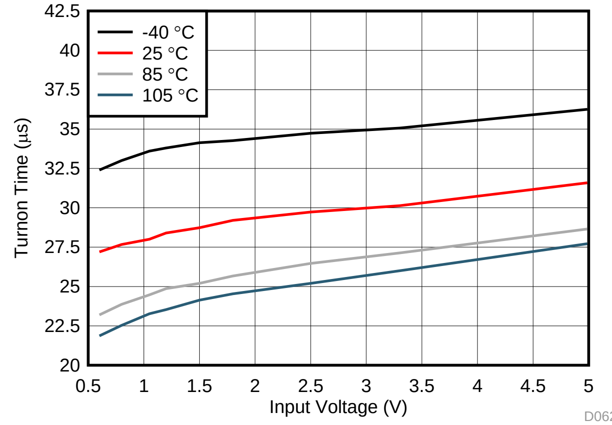
Figure 12. Hysteresis vs Bias Voltage

Typical Characteristics (continued)



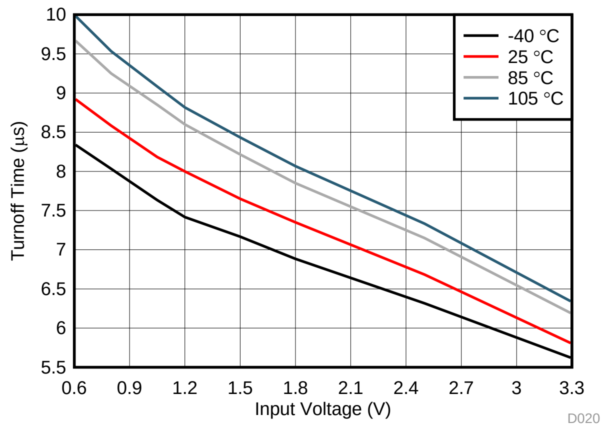
V_{BIAS} = 3.3 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 13. Turnon Time vs Input Voltage



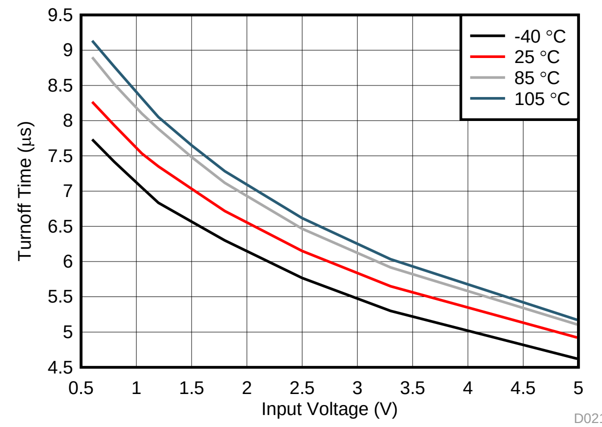
V_{BIAS} = 5 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 14. Turnon Time vs Input Voltage



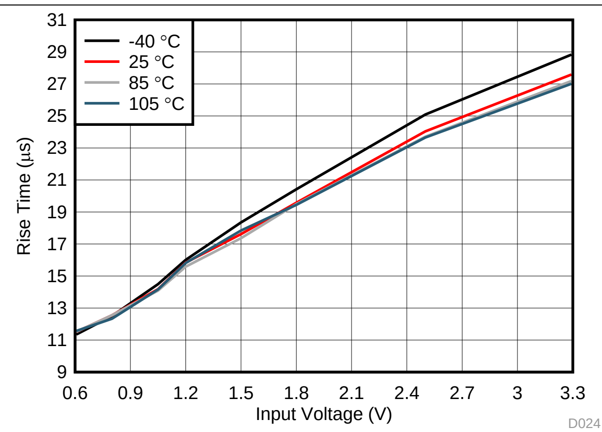
V_{BIAS} = 3.3 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 15. Turnoff Time vs Input Voltage



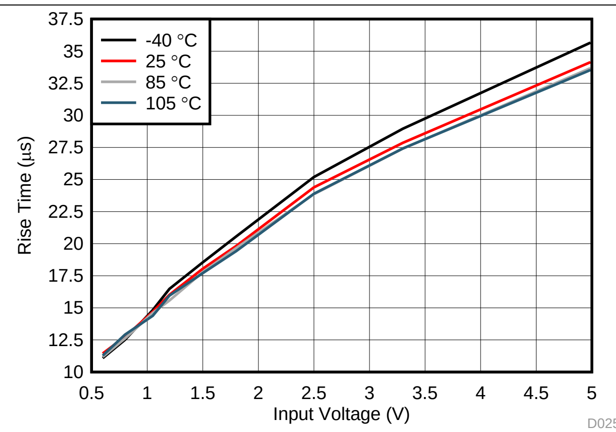
V_{BIAS} = 5 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 16. Turnoff Time vs Input Voltage



V_{BIAS} = 3.3 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

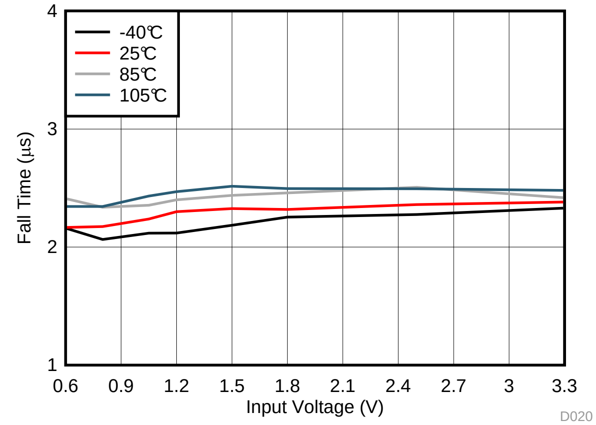
Figure 17. Rise Time vs Input Voltage



V_{BIAS} = 5 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

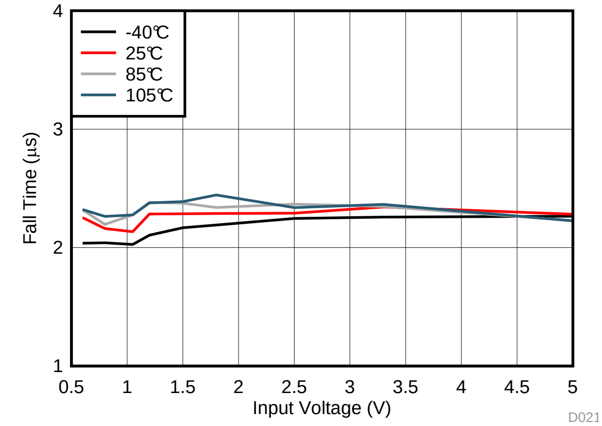
Figure 18. Rise Time vs Input Voltage

Typical Characteristics (continued)



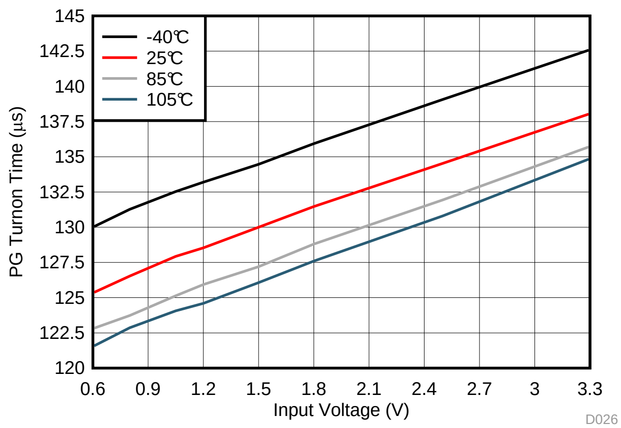
V_{BIAS} = 3.3 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 19. Fall Time vs Input Voltage



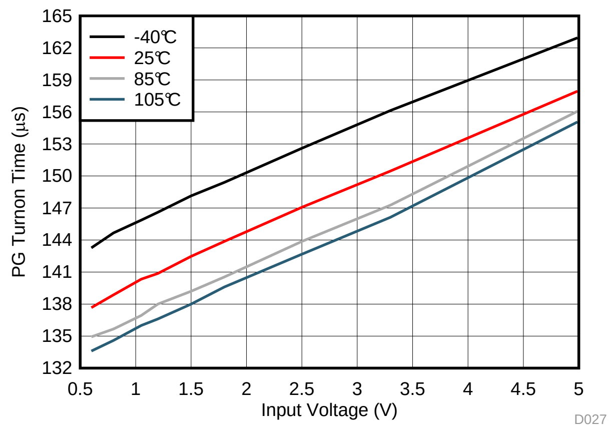
V_{BIAS} = 5 V V_{ON} = 5 V C_T = 0 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 20. Fall Time vs Input Voltage



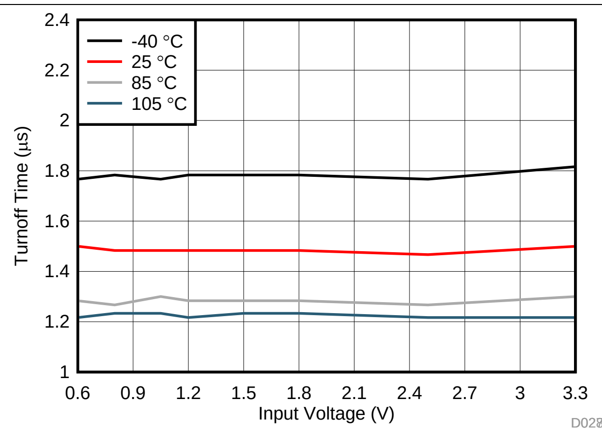
V_{BIAS} = 3.3 V V_{ON} = 5 V C_T = 0 pF
R_{PU} = 10 kΩ C_L = 0.1 µF R_L = 10 Ω

Figure 21. PG Turnon Time vs Input Voltage



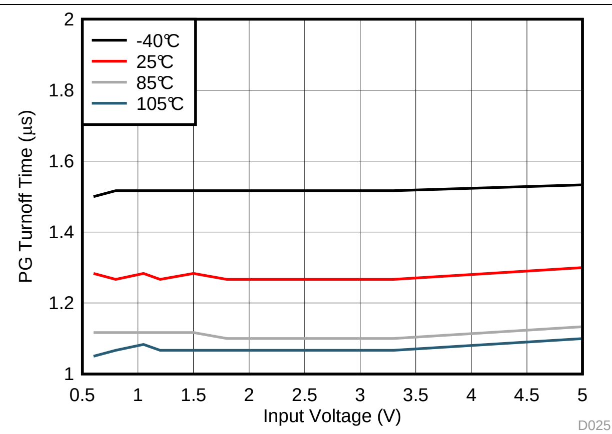
V_{BIAS} = 5 V V_{ON} = 5 V C_T = 0 pF
R_{PU} = 10 kΩ C_L = 0.1 µF R_L = 10 Ω

Figure 22. PG Turnon Time vs Input Voltage



V_{BIAS} = 3.3 V V_{ON} = 5 V C_T = 0 pF
R_{PU} = 10 kΩ C_L = 0.1 µF R_L = 10 Ω

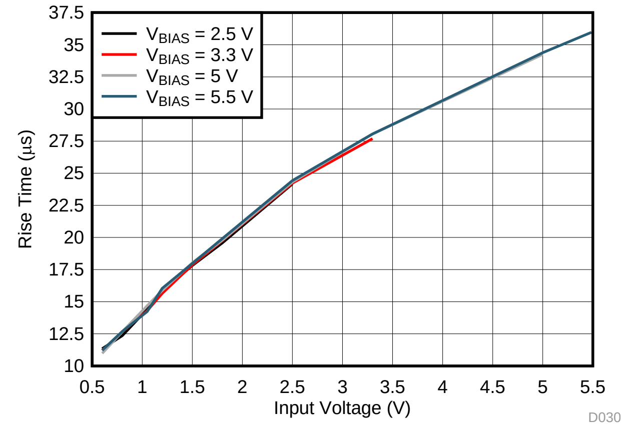
Figure 23. PG Turnoff vs Input Voltage



V_{BIAS} = 5 V V_{ON} = 5 V C_T = 0 pF
R_{PU} = 10 kΩ C_L = 0.1 µF R_L = 10 Ω

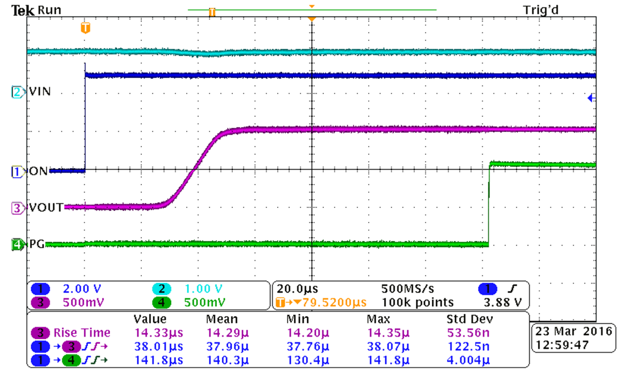
Figure 24. PG Turnoff Time vs Input Voltage

Typical Characteristics (continued)



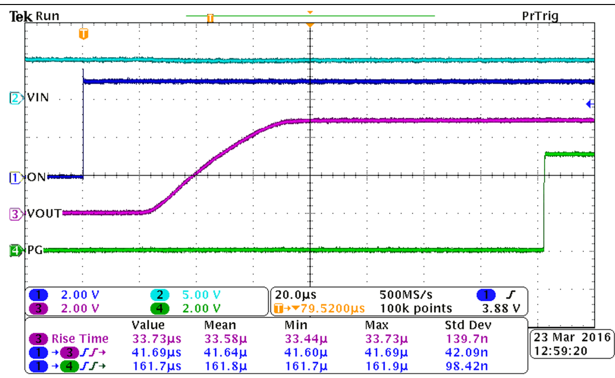
T_A= 25°C C_{IN} = 1 µF C_L = 0.1 µF C_T = 0 pF R_L = 10 Ω

Figure 25. Rise Time vs Input Voltage



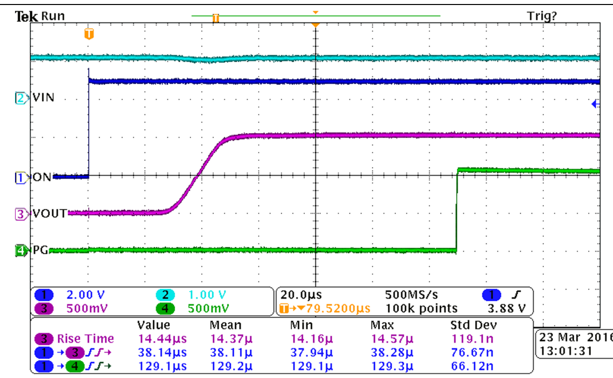
V_{BIAS} = 5 V C_{IN} = 1 µF V_{IN} = 1.05 V C_L = 0.1 µF C_T = 0 pF R_L = 10 Ω

Figure 26. Turnon Response



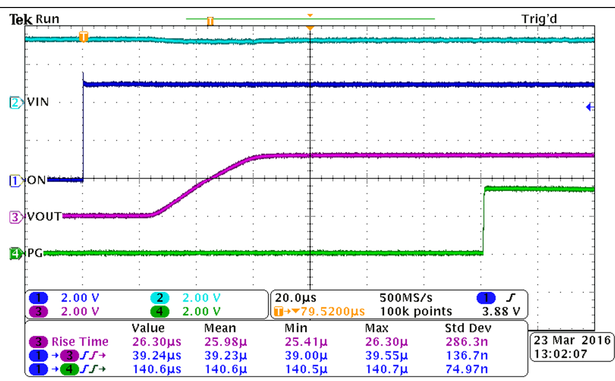
V_{BIAS} = 5 V C_{IN} = 1 µF V_{IN} = 5 V C_L = 0.1 µF C_T = 0 pF R_L = 10 Ω

Figure 27. Turnon Response



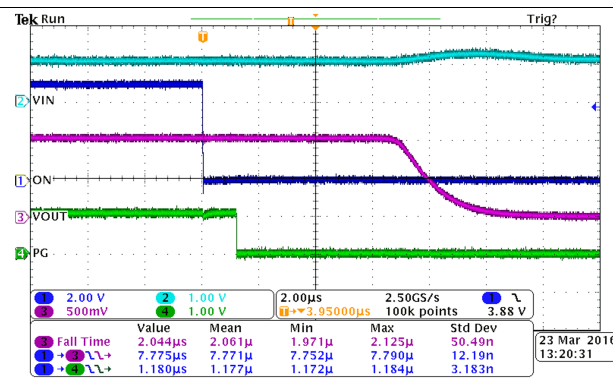
V_{BIAS} = 3.3 V C_{IN} = 1 µF V_{IN} = 1.05 V C_L = 0.1 µF C_T = 0 pF R_L = 10 Ω

Figure 28. Turnon Response



V_{BIAS} = 3.3 V C_{IN} = 1 µF V_{IN} = 3.3 V C_L = 0.1 µF C_T = 0 pF R_L = 10 Ω

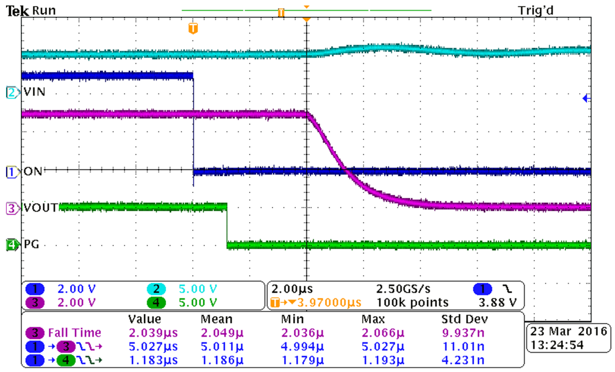
Figure 29. Turnon Response



V_{BIAS} = 5 V C_{IN} = 1 µF V_{IN} = 1.05 V C_L = 0.1 µF C_T = 0 pF R_L = 10 Ω

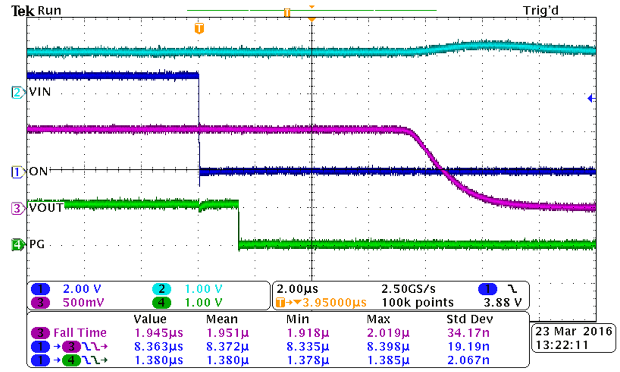
Figure 30. Turnon Response

Typical Characteristics (continued)



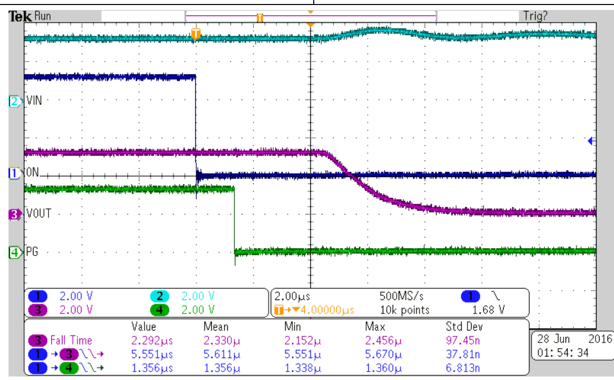
V_{BIAS} = 5 V, V_{IN} = 5 V, C_T = 0 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 31. Turnoff Response



V_{BIAS} = 3.3 V, V_{IN} = 1.05 V, C_T = 0 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 32. Turnoff Response



V_{BIAS} = 3.3 V, V_{IN} = 3.3 V, C_T = 0 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 33. Turnoff Response

8 Parameter Measurement Information

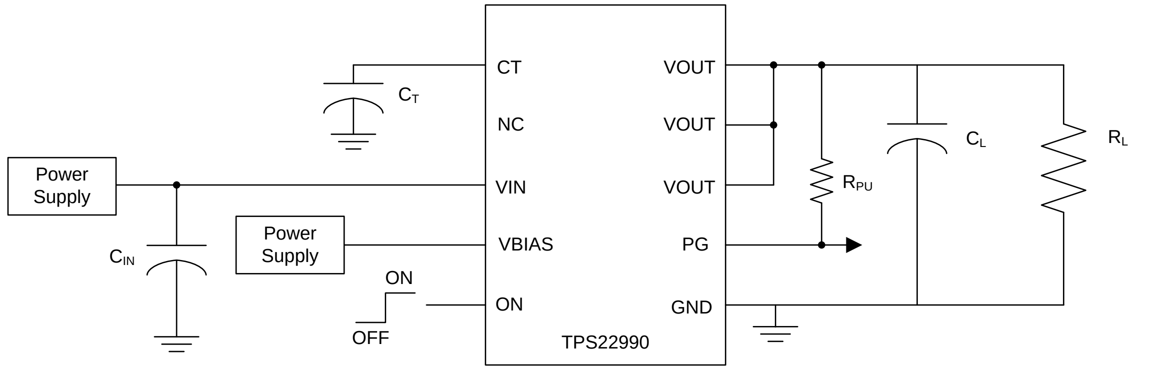
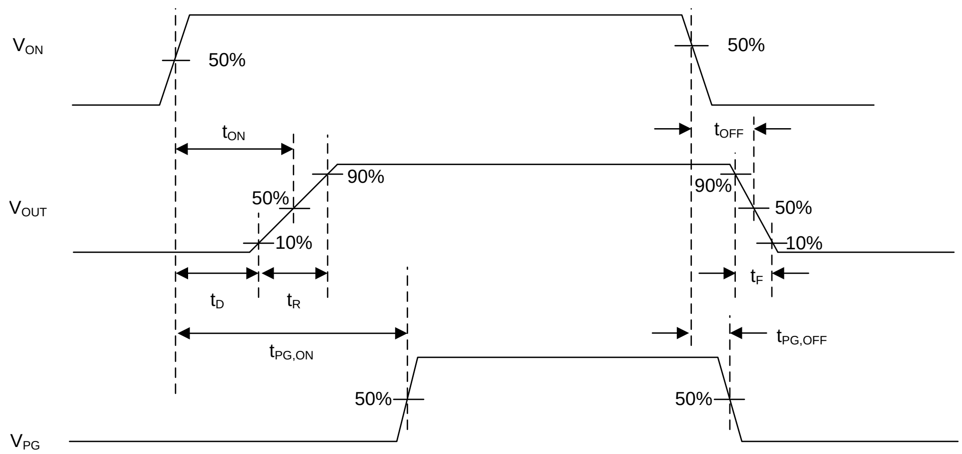


Figure 34. Timing Test Circuit



Rise and fall times of the control signals is 100 ns.

Figure 35. Timing Waveforms

9 Detailed Description

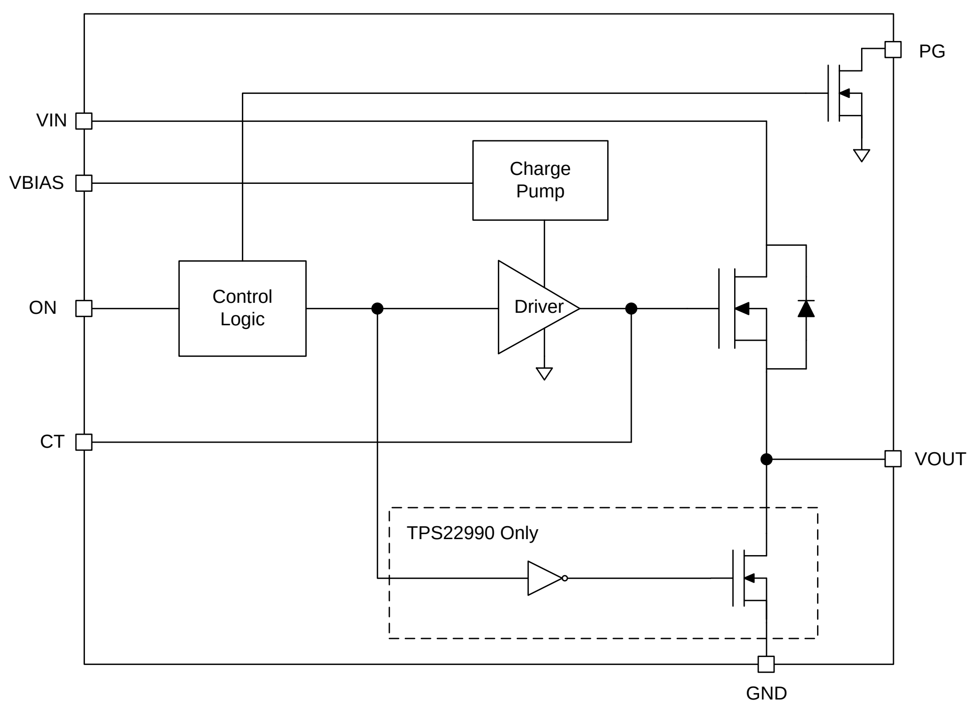
9.1 Overview

The TPS22990 device is a single channel load switch with a controlled adjustable turnon and integrated PG indicator. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6 V to 5.5 V and can support a maximum continuous current of 10 A. The wide input voltage range and high current capability enable the devices to be used across multiple designs and end equipment. 3.9-mΩ On-resistance minimizes the voltage drop across the load switch and power loss from the load switch.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through CT provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

During shutdown, the device has very low leakage current, thereby reducing unnecessary leakages for downstream modules during standby. The TPS22990 has an optional 218-Ω On-chip resistor for quick discharge of the output when switch is disabled.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On and Off Control

The ON pin controls the state of the load switch. Asserting the pin high enables the switch. The minimum voltage that guarantees logic high is 1.2 V. This pin cannot be left floating and must be tied either high or low for proper functionality.

Feature Description (continued)

9.3.2 Adjustable Rise Time

The TPS22990 has controlled rise time for inrush current control. A capacitor to GND on the CT pin adjusts the rise time. Without any capacitor on the CT, the rise time is at its minimum for fastest timing. The voltage on the CT pin can be as high as 15 V; therefore the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate equation for the relationship between C_T, V_{IN} and rise time when V_{BIAS} is set to 5 V is shown in Equation 1. As shown in Figure 35, rise time is defined as from 10% to 90% measurement on V_{OUT}.

$$t_R = (0.011 \times V_{IN} + 0.002) \times C_T + 4.7 \times V_{IN} + 7.8$$

where

- t_R is the rise time (in µs)
- V_{IN} is the input voltage (in V)
- C_T is the capacitance value on the CT pin (in pF) (1)

Table 1 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

Table 1. Rise Time vs CT Capacitor

C_T (pF)	Rise Time (µs) at 25°C C_L = 0.1 uF, C_{IN} = 1 uF, R_L = 10 Ω, V_{BIAS} = 5 V				
	V_{IN} = 5 V	V_{IN} = 3.3 V	V_{IN} = 1.8 V	V_{IN} = 1.05 V	V_{IN} = 0.6 V
0	30.5	24.8	17.5	12.6	9.5
220	44.6	34	22.7	15.8	11.4
470	56.6	42.2	27.1	18.8	13.2
1000	85	61.1	38.9	25.2	17.9
2200	154.6	107	64.7	40.9	27.7
4700	284.6	193.5	114.4	72.8	48.1
10000	598.5	404.8	233.2	146.9	98.6

9.3.3 Power Good (PG)

The TPS22990 has a power good (PG) output signal to indicate the gate of the pass FET is driven high and the switch is on with the On-resistance close to its final value (full load ready). The signal is an active high and open drain output which can be connected to a voltage source through an external pull up resistor, R_{PU}. This voltage source can be VOUT from the TPS22990 or another external voltage. VBIAS is required for PG to have a valid output. Equation 2 below shows the approximate equation for the relationship between C_T, V_{IN} and PG turnon time ($t_{PG,ON}$) when V_{BIAS} is set to 5 V.

$$t_{PG,ON} = (0.013 * V_{IN} + 0.04) * C_T + 4.7 * V_{IN} + 129$$

where

- $t_{PG,ON}$ is the PG turnon time (in µs)
- V_{IN} is the input voltage (in V)
- C_T is the capacitance value on the CT pin (in pF) (2)

Table 2 contains PG turnon time values measured on a typical device.

Table 2. PG Turnon Time vs CT Capacitor

C_T (pF)	Typical PG turnon time (us) at 25°C C_L = 0.1 uF, C_{IN} = 1 uF, R_L = 10 Ω, V_{BIAS} = 5 V, R_{PU} = 10 kΩ				
	V_{IN} = 5 V	V_{IN} = 3.3 V	V_{IN} = 1.8 V	V_{IN} = 1.05 V	V_{IN} = 0.6 V
0	151.9	144.4	137.5	133.9	131.3
220	177.7	164.6	153.3	147.1	143.5
470	200.9	183.2	167.4	159.2	154.4
1000	257.2	227.8	202.5	189.5	181.3
2200	390.6	332.3	282.4	257.1	241.6
4700	636.4	525.6	429.8	382.7	353.3
10000	1239	999.8	792.4	689.4	627.4

9.3.4 Quick Output Discharge (QOD) (TPS22990 Only)

The TPS22990 family includes an optional QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 218 Ω and prevents the output from floating while the switch is disabled.

9.4 Device Functional Modes

Table 3 shows the function table for TPS22990.

Table 3. Function Table

ON	VIN to VOUT	OUTPUT DISCHARGE (1)
L	OFF	ENABLED
H	ON	DISABLED

(1) This feature is in the TPS22990 only (not in TPS22990N).

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} condition of the device. See the R_{ON} specification in the *Electrical Characteristics—V_{BIAS} = 5 V* table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 3 to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV is the voltage drop from VIN to VOUT
- I_{LOAD} is the load current
- R_{ON} is the on-resistance of the device for a specific VIN and VBIAS
- An appropriate I_{LOAD} must be chosen such that the IMAX specification of the device is not violated (3)

10.1.2 Input Capacitor

It is recommended to use a capacitor between VIN and GND close to the device pins. This helps limit the voltage drop on the input supply caused by transient inrush currents when the switch is turned on into a discharged capacitor at the load. A 1-µF ceramic capacitor, C_{IN}, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup, where C_L is the load capacitance.

10.1.3 Thermal Consideration

The maximum junction temperature should be limited to below 125°C. Use Equation 4 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output load current and ambient temperature. $R_{\theta JA}$ is highly dependent upon board layout.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the junction-to-air thermal impedance (4)

10.1.4 PG Pull Up Resistor

The PG output is an open drain signal which connects to a voltage source through a pull up resistor R_{PU}. The PG signal can be used to drive the enable pins of downstream devices, EN. PG is active high, and its voltage is given by Equation 5.

Application Information (continued)

$$V_{PG} = V_{OUT} - \left(I_{PG,LK} + I_{EN,LK}\right) \times R_{PU}$$

where

- V_{OUT} is the voltage where PG is tied to
- $I_{PG,LK}$ is the leakage current into PG pin
- $I_{EN,LK}$ is the leakage current into the EN pin driven by PG
- R_{PU} is the pull up resistance (5)

V_{PG} needs to be higher than $V_{IH,\ MIN}$ of the EN pin to be treated as logic high. The maximum R_{PU} is determined by Equation 6.

$$R_{PU,MAX} = \frac{V_{OUT} - V_{IH,MIN}}{I_{PG,LK} + I_{EN,LK}} \tag{6}$$

When PG is disabled, with 1 mA current into PG pin (I_{PG} = 1 mA), $V_{PG,OL}$ is less than 0.2 V and treated as logic low as long as $V_{IL,MAX}$ of the EN pin is greater than 0.2 V. The minimum R_{PU} is determined by Equation 7.

$$R_{PU,MIN} = \frac{V_{OUT}}{I_{PG} + I_{EN,LK}} \tag{7}$$

R_{PU} can be chosen within the range defined by $R_{PU,MIN}$ and $R_{PU,MAX}$. R_{PU} = 10 kΩ is used for characterization.

10.1.5 Power Sequencing

The TPS22990 has an integrated power good indicator which can be used for power sequencing. As shown in Figure 36, the switch to the second load is controlled by the PG signal from the first switch. This ensures that the power to load 2 is only enabled after the power to load 1 is enabled and the first switch is full load ready.

Application Information (continued)

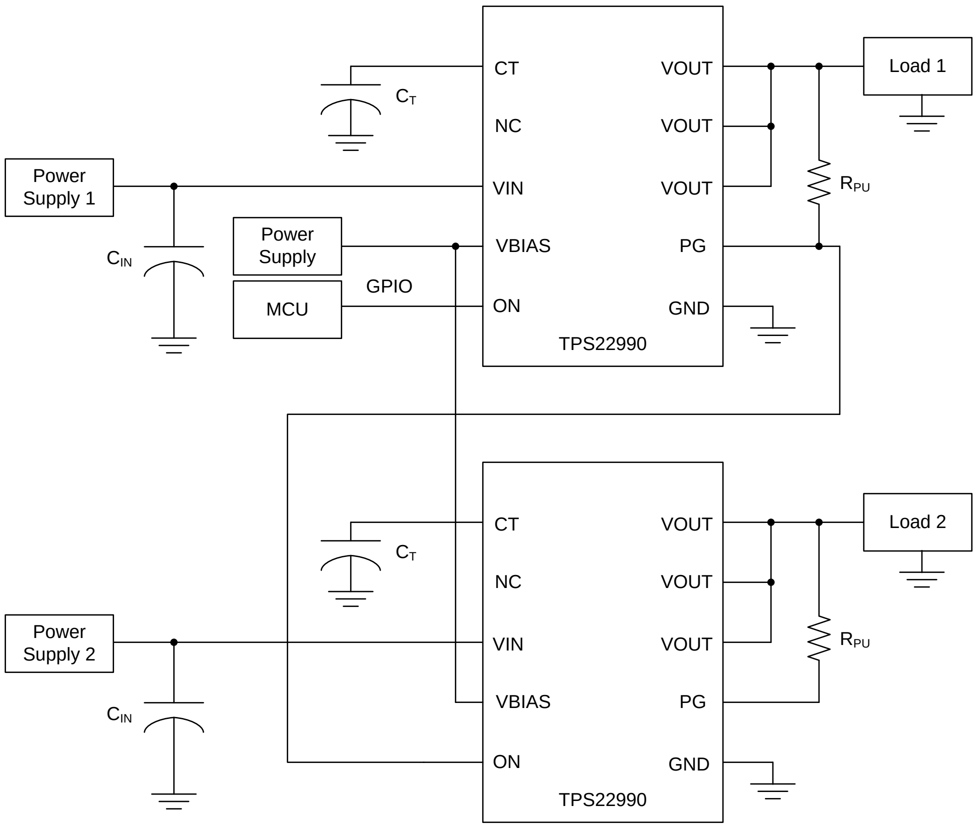


Figure 36. Power Sequencing

10.1.6 Standby Power Reduction

Any end equipment that is being powered from a battery has a need to reduce current consumption in order to maintain the battery charge for a longer time. The TPS22990 devices help to accomplish this reduction by turning off the supply to the downstream modules that are in standby state and significantly reduce the leakage current overhead of the standby modules as shown in Figure 37.

Application Information (continued)

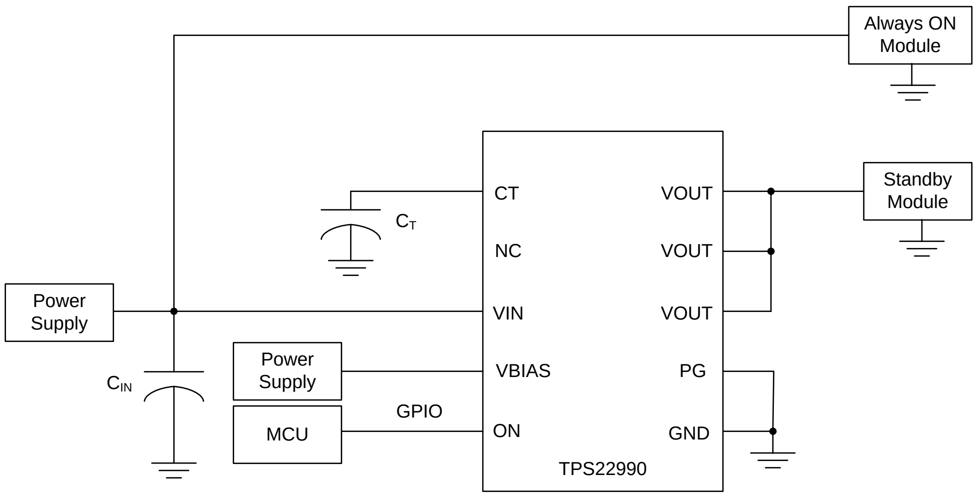


Figure 37. Standby Power Reduction

10.2 Typical Application

Figure 38 demonstrates how to use TPS22990 to limit inrush current to output capacitance.

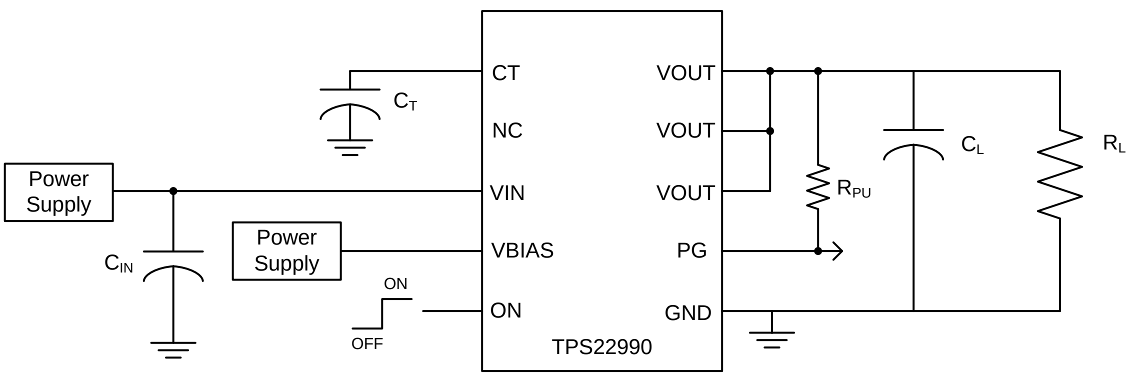


Figure 38. Powering a Downstream Module

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 4.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BIAS}	3.3 V
V_{IN}	1.05 V
C_L	10 µF
R_L	None
Maximum acceptable inrush current	100 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to V_{IN}. This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 8.

$$I_{INRUSH} = C_L \times \frac{dV}{dt} \approx C_L \times \frac{0.8 \times V_{IN}}{t_R}$$

where
- I_{INRUSH} is the Inrush current
- C_L is the Load capacitance
- *dV/dt* is the Output slew rate
- V_{IN} is the Input voltage
- t_R is the rise time (8)

Minimum acceptable rise time can be calculated using the design requirements and the inrush current equation. See Equation 9.

$$t_R = \frac{0.8 \times V_{IN} \times C_L}{I_{INRUSH}} = 84 \mu s \quad (9)$$

The TPS22990 has very fast timing without a CT capacitor (C_T). The typical rise time is 12 µs at V_{BIAS} = 3.3 V, V_{IN} = 1.05 V, R_L = 10 Ω, and C_L = 0.1 µF. As shown in Figure 39, the rise time is much smaller than 84 µs and the inrush current is 460 mA without C_T. The C_T for the required rise time must be calculated using Equation 1. For 84 µs, the calculated C_T = 5259 pF. Figure 40 shows the inrush current is less than 100 mA with C_T = 6800 pF.

10.2.3 Application Curves

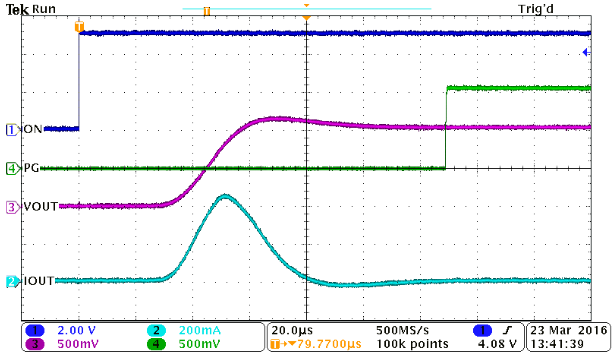


Figure 39. . Inrush Current with C_T = 0 pF

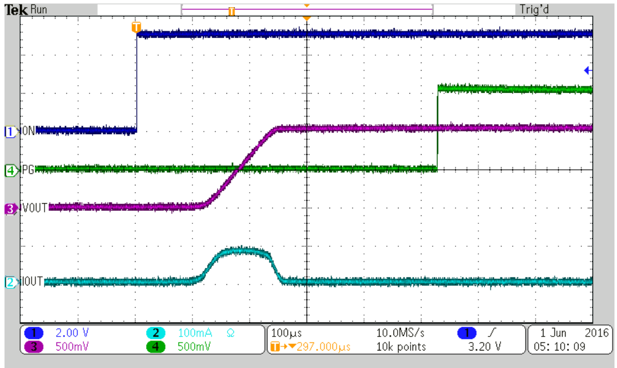


Figure 40. Inrush Current with C_T = 6800 pF

11 Power Supply Recommendations

The device is designed to operate with a V_{BIAS} range of 2.5 V to 5.5 V, and a V_{IN} range of 0.6 V to V_{BIAS}. The supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. In the case where the power supply is slow to respond to a large load current step, additional bulk may also be required. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects. The CT trace must be as short as possible to reduce parasitic capacitance.

12.2 Layout Example

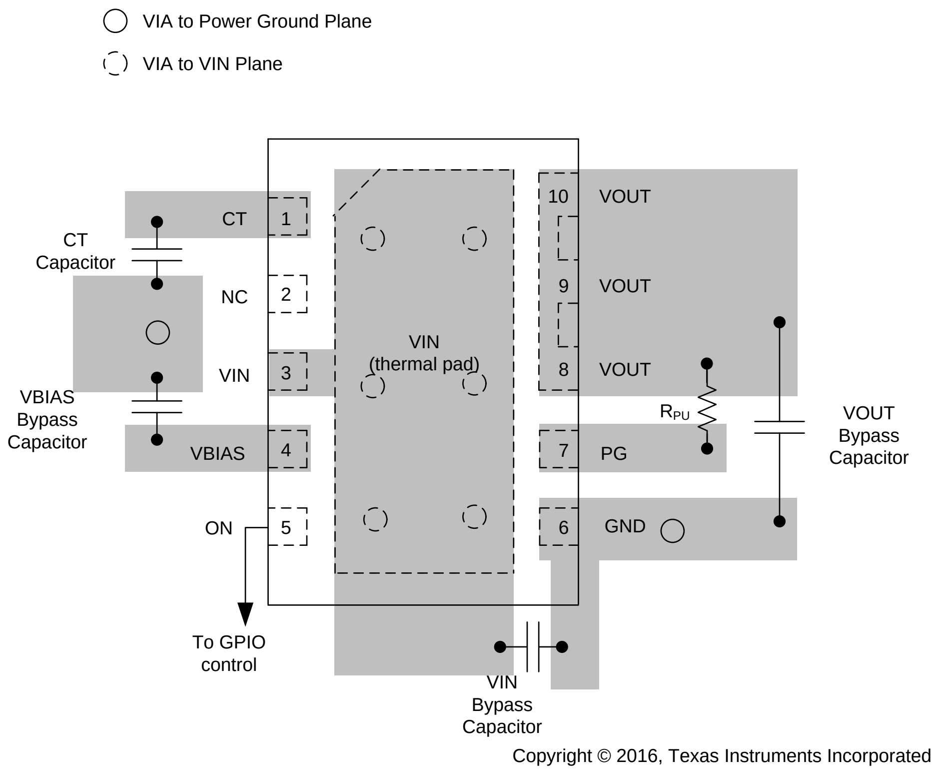


Figure 41. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *TPS22990 Load Switch Evaluation Module*, SLVUAS2
- *Fundamentals of On-Resistance in Load Switches*, SLVA771

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22990DMLR	ACTIVE	WSON	DML	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990	Samples
TPS22990DMLT	ACTIVE	WSON	DML	10	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990	Samples
TPS22990NDMLR	ACTIVE	WSON	DML	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990N	Samples
TPS22990NDMLT	ACTIVE	WSON	DML	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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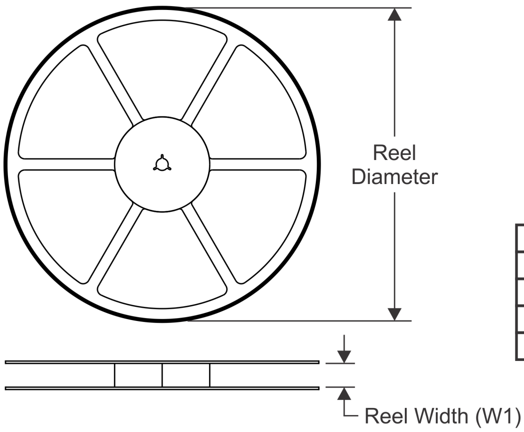
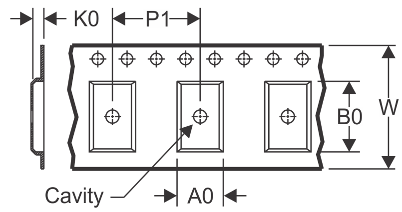
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

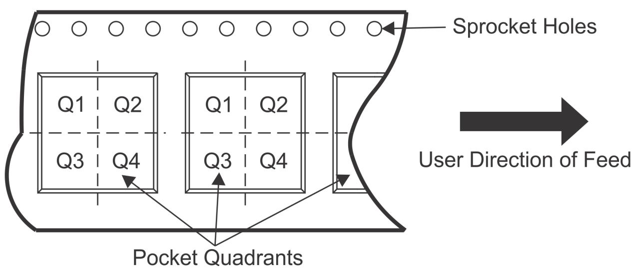


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

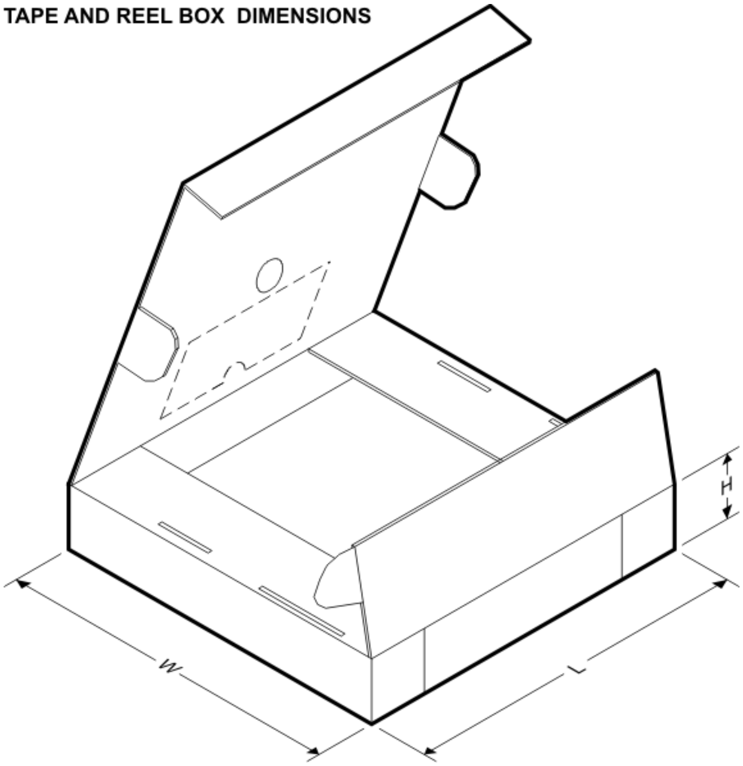
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

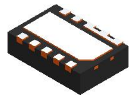
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22990NDMLR	WSON	DML	10	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22990NDMLT	WSON	DML	10	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

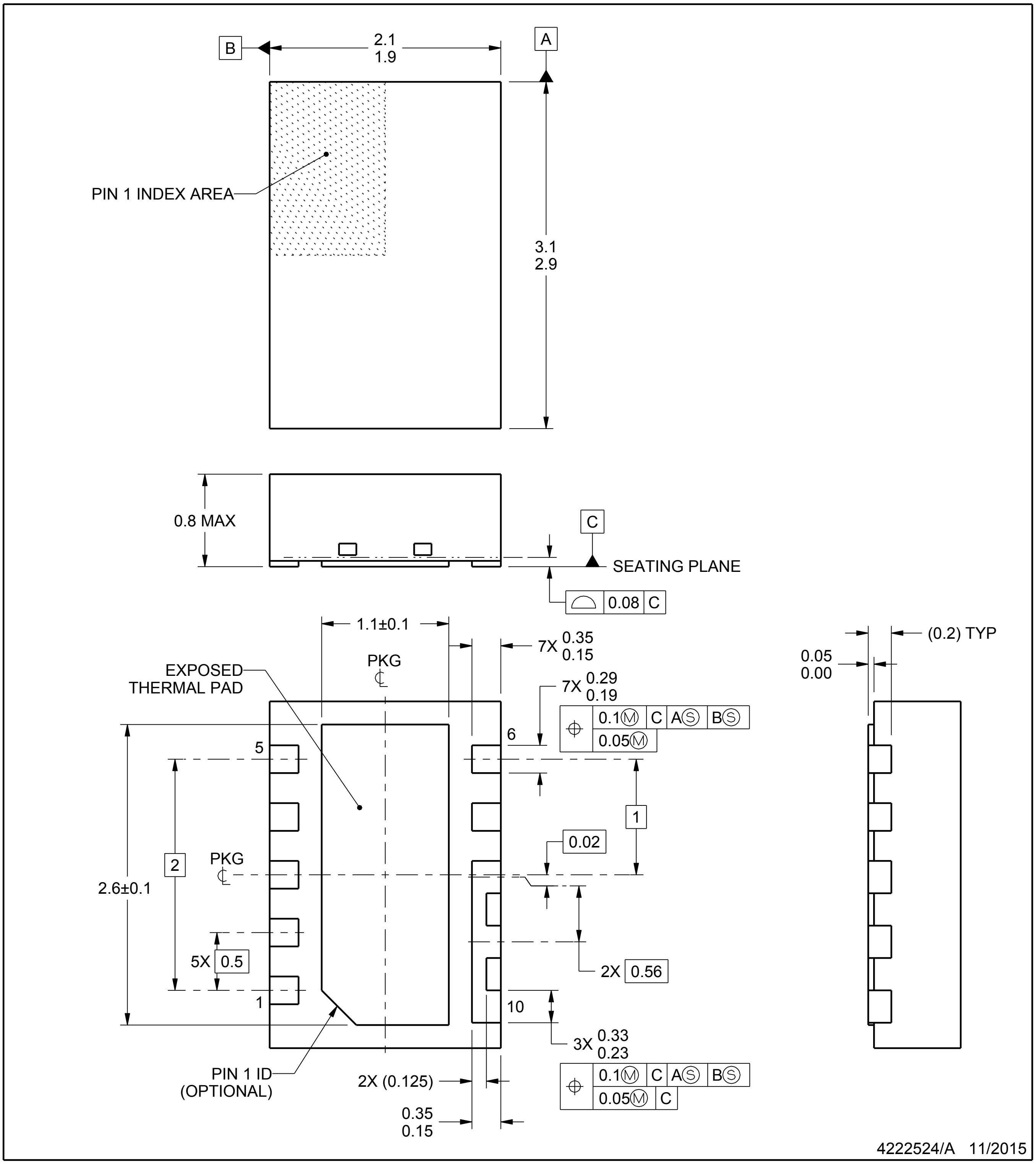
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

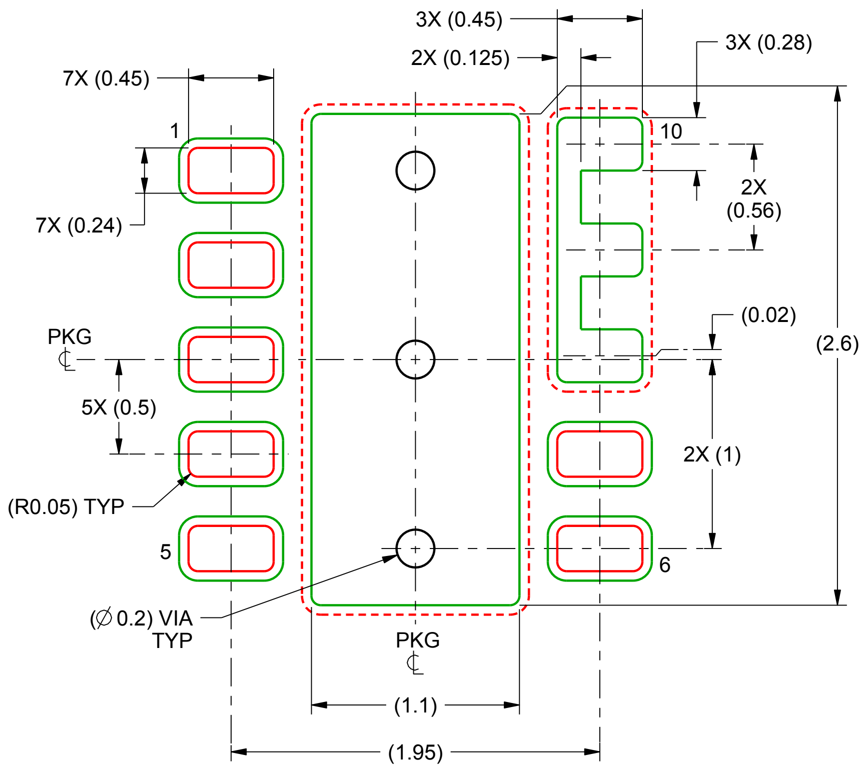
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22990NDMLR	WSON	DML	10	3000	213.0	191.0	35.0
TPS22990NDMLT	WSON	DML	10	250	213.0	191.0	35.0



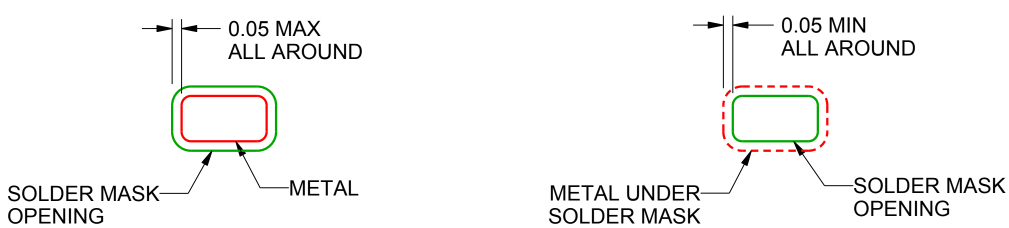


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK
DEFINED

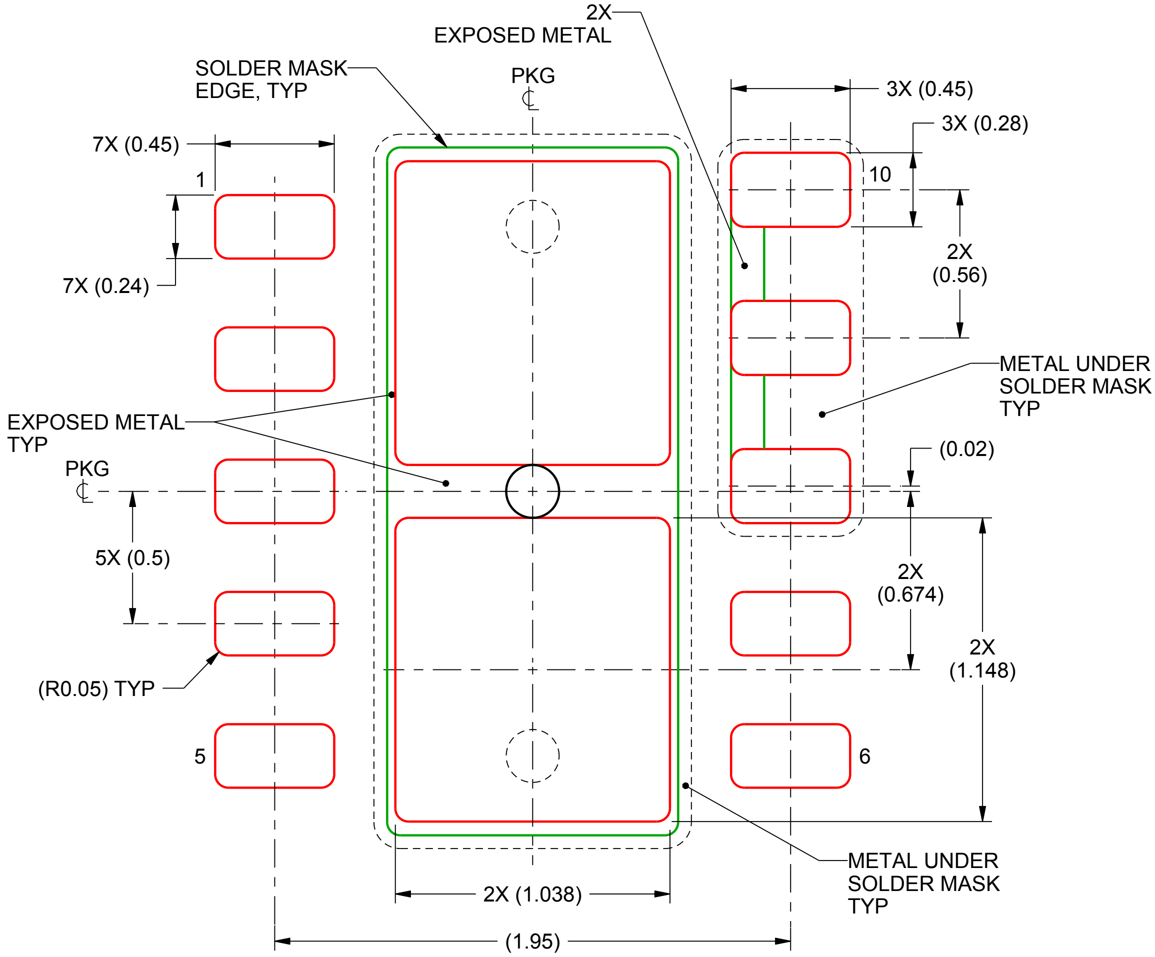
SOLDER MASK
DEFINED
THERMAL PAD & PADS 8-10

SOLDER MASK DETAILS

4222524/A 11/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:35X

4222524/A 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.