THIS SPEC IS OBSOLETE

Spec No: 001-06510

Spec Title: CY62136VN MOBL(R) 2-MBIT (128K X 16) STATIC RAM

Sunset Owner: Anuj Chakrapani (aju)

Replaced by: NONE

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2-Mbit (128K x 16) Static RAM

Features

- **Temperature Ranges**
  - **— Industrial: –40°C to 85°C**
  - **— Automotive-A: –40°C to 85°C**
- **High speed: 55 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in standard 44-pin TSOP Type II and 48-ball FBGA packages**

Functional Description

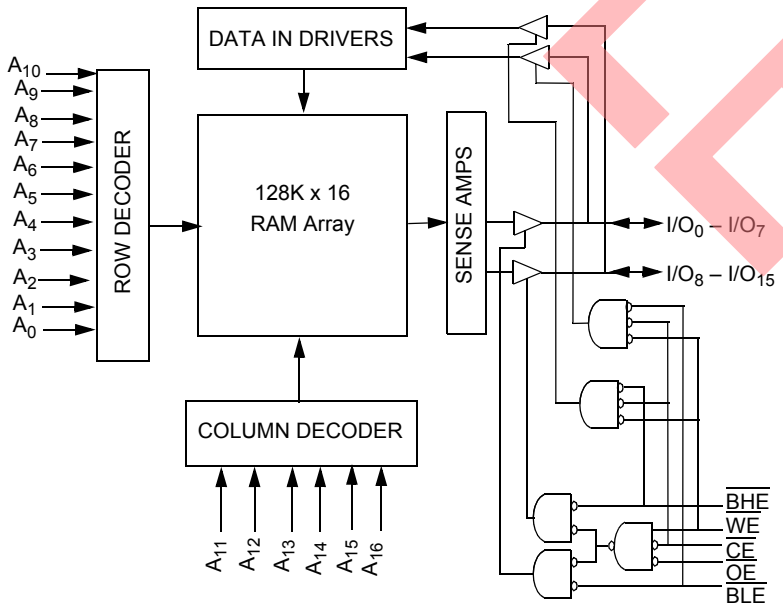
The CY62136VN is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (CE HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

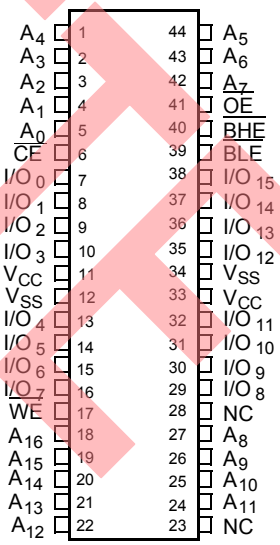
For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



PinConfigurations[3]

TSOP II (Forward)
Top View



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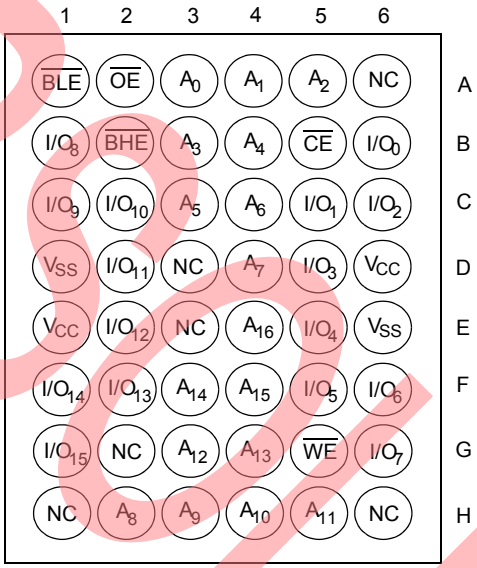
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Product Portfolio

Product	V_{CC} Range (V)			Speed	Ranges	Power Dissipation			
						Operating, I_{CC} (mA)		Standby, I_{SB2} (µA)	
	Min	Typ.[1]	Max			Typ.[1]	Maximum	Typ.[1]	Maximum
CY62136VNLL	2.7	3.0	3.6	55	Automotive-A	7	20	1	15
				70	Industrial	7	15	1	15
				70	Automotive-A	7	15	1	15

Pin Configurations[2]

FBGA
Top View



Notes:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.
2. NC pins are not connected on the die.

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Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[3] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature [T_A][4]	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V
Automotive-A	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			-55			-70			Unit
					Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V, I_{OH} = –1.0 mA			2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V, I_{OL} = 2.1 mA					0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 3.6V			2.2		V_{CC} + 0.5V	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.7V			–0.5		0.8	–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		Ind'l				–1		+1	µA
				Auto-A	–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		Ind'l				–1		+1	µA
				Auto-A	–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = 3.6V, I_{OUT} = 0 mA, CMOS Levels	Ind'l					7	15	mA
				Auto-A		7	20		7	15	
		f = 1 MHz		Ind'l					1	2	mA
				Auto-A		1	2		1	2	
I_{SB1}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}		Ind'l						100	µA
				Auto-A			100			100	µA
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0		Ind'l					1	15	µA
				Auto-A		1	15		1	15	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
3. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
4. T_A is the "Instant-On" case temperature.
5. Tested initially and after any design or process changes that may affect these parameters.

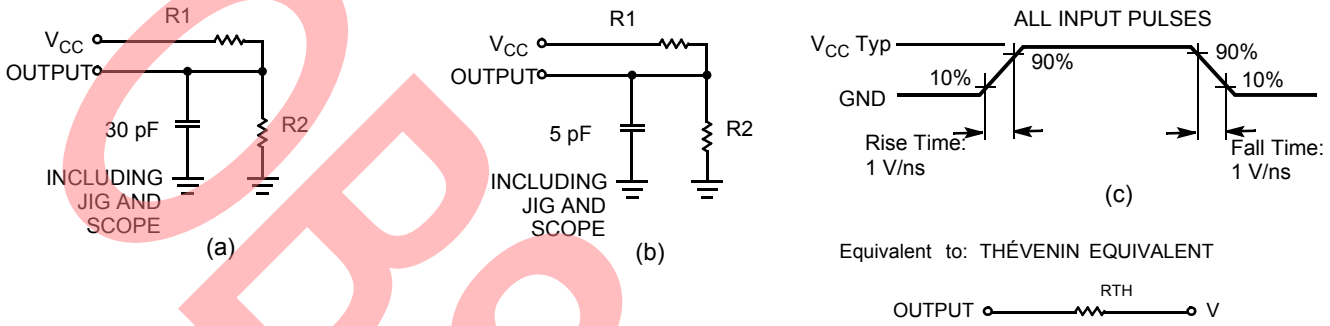
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Thermal Resistance[5]

Parameter	Description	Test Conditions	TSOPII	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	60	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		22	16	°C/W

AC Test Loads and Waveforms

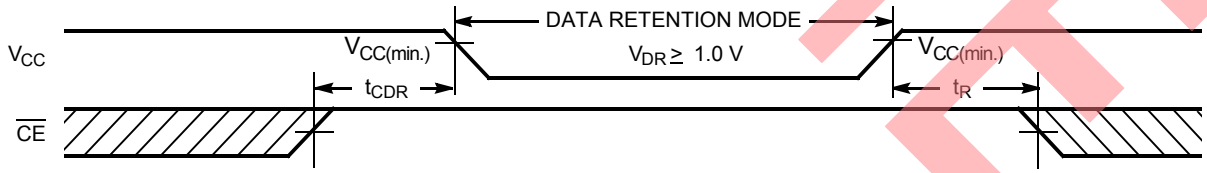


Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[8]	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	V_{CC} = 1.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$,		0.5	7.5	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0			ns
t_R[6]	Operation Recovery Time		70			ns

Data Retention Waveform



Note:
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ ms or stable at $V_{CC(min)} \geq 100$ ms.
7. No input may exceed V_{CC} + 0.3V

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Switching Characteristics Over the Operating Range [8]

Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[9]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[9, 10]		25		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[9]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[9, 10]		25		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		55		70	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		25		35	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z[9, 10]	5		5		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z[11]		25		25	ns
Write Cycle[11, 12]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	50		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9, 10]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	5		10		ns

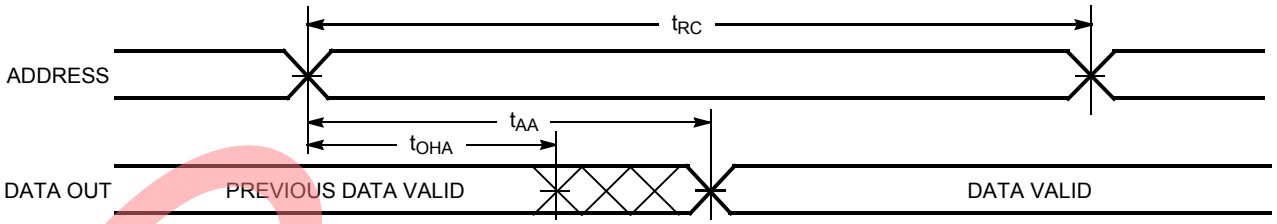
Notes:
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

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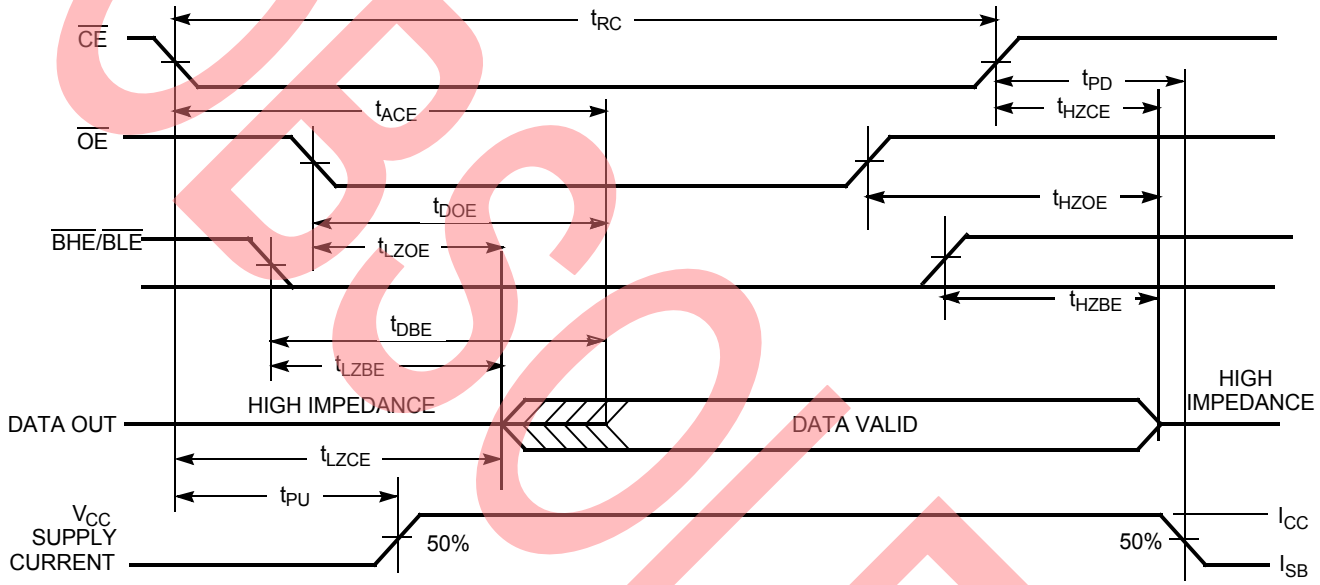
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Switching Waveforms

Read Cycle No. 1[13, 14]



Read Cycle No. 2[14, 15]



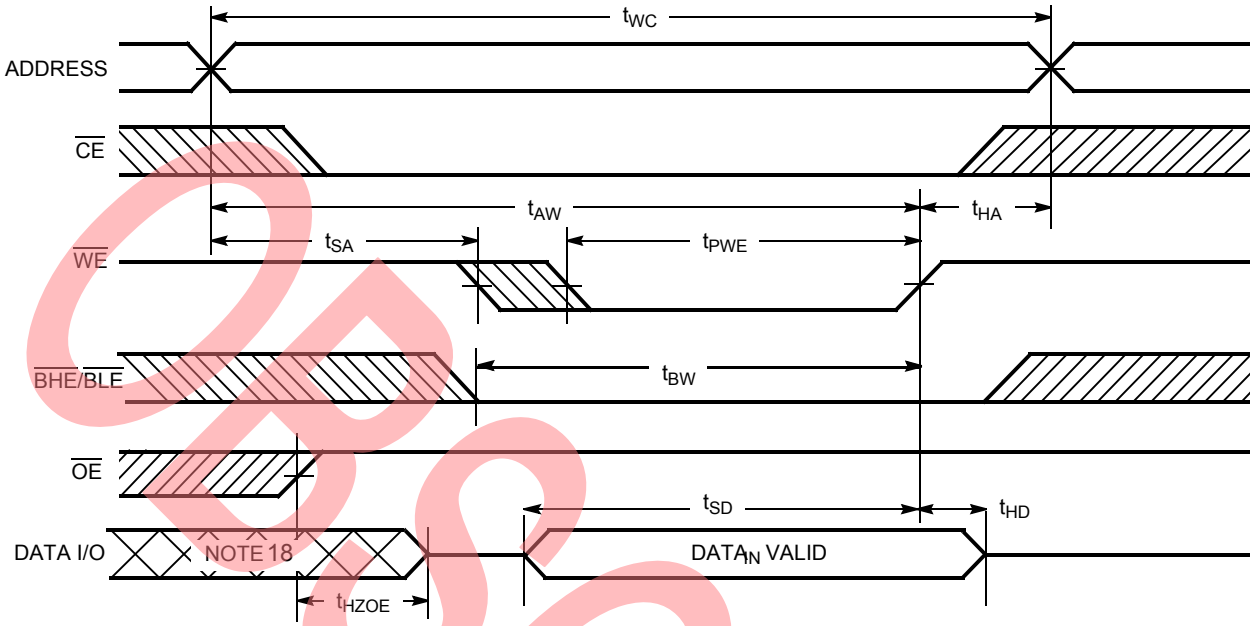
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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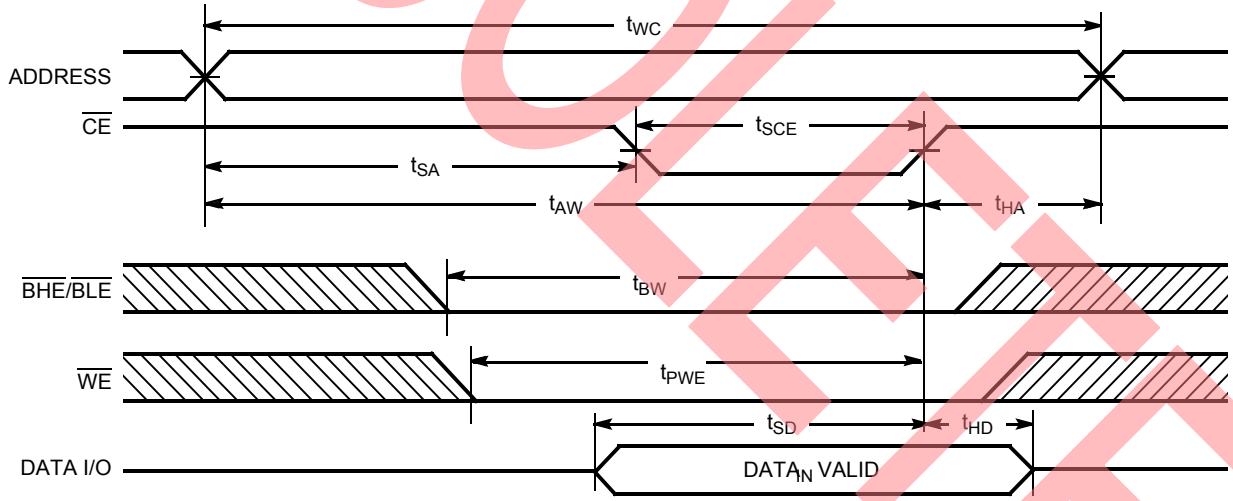
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Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)[11, 16, 17]



Write Cycle No. 2 (CE Controlled)[11, 16, 17]



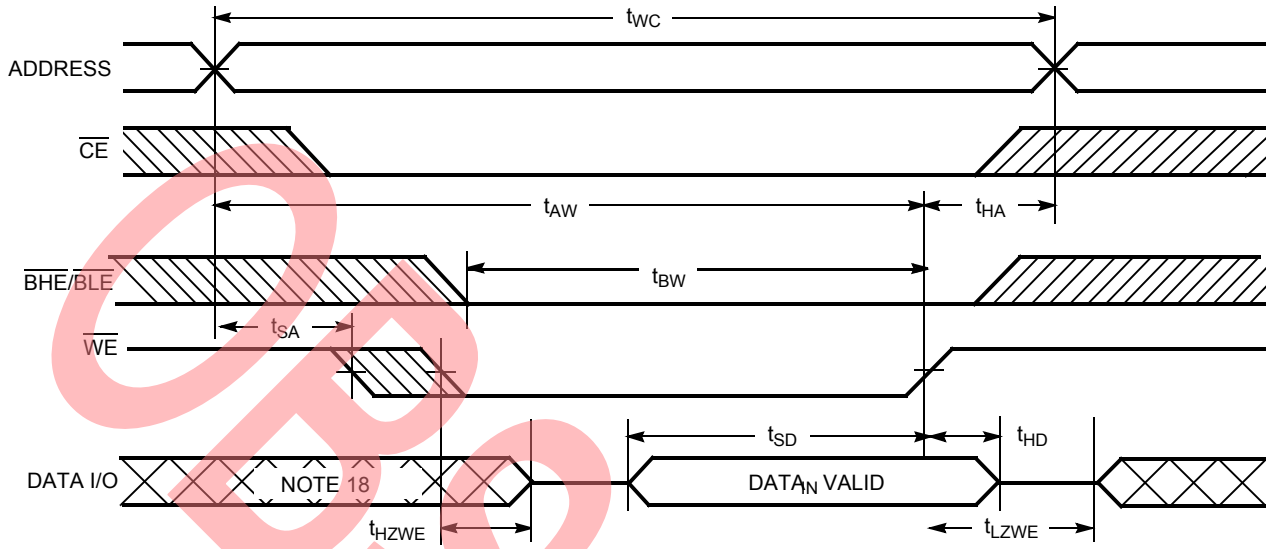
Notes:
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

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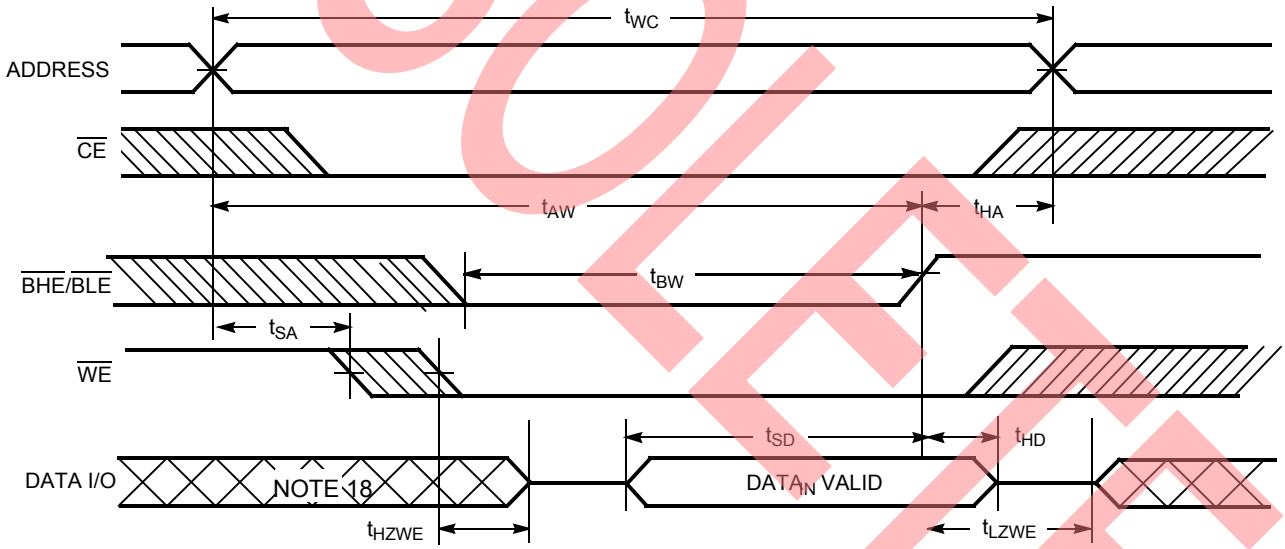
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Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW)[12, 17]



Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)[18]

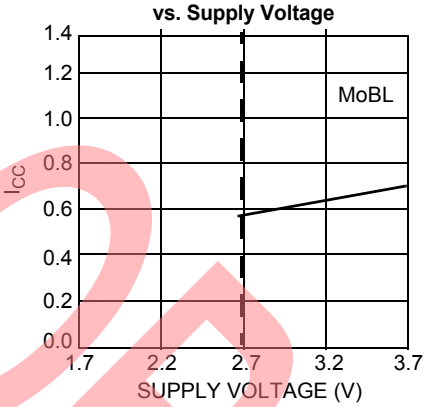


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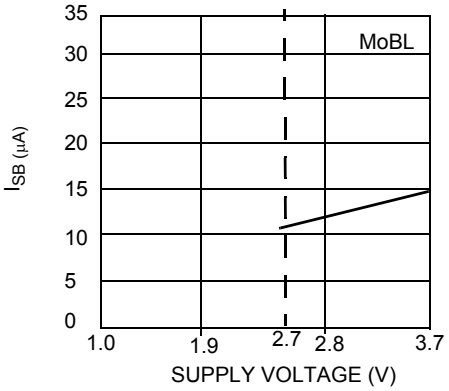
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Typical DC and AC Characteristics

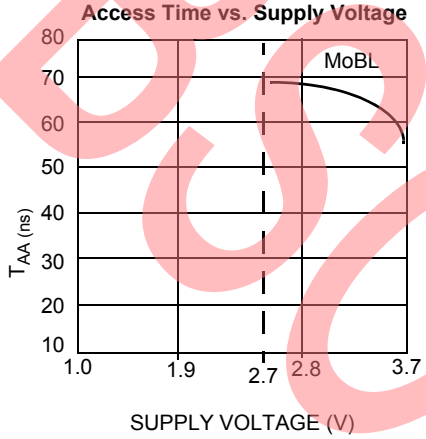
Normalized Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0 –I/O_7 in High-Z	Write	Active (I_{CC})

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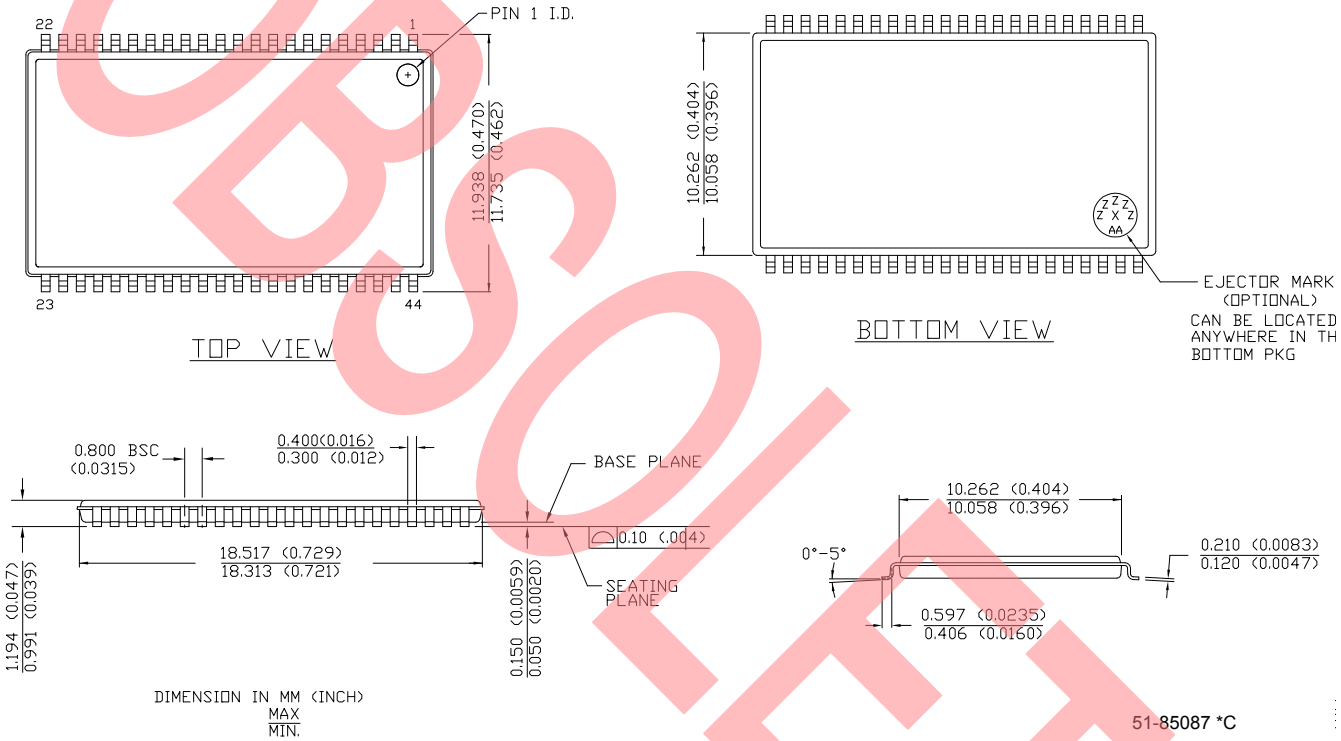
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62136VNLL-55ZSXA	51-85087	44-pin TSOP II (Pb-Free)	Automotive-A
70	CY62136VNLL-70BAI	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA	Industrial
	CY62136VNLL-70ZSXA	51-85087	44-pin TSOP II (Pb-Free)	Automotive-A

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams (continued)

Figure 1. 44-pin TSOP II (51-85087)

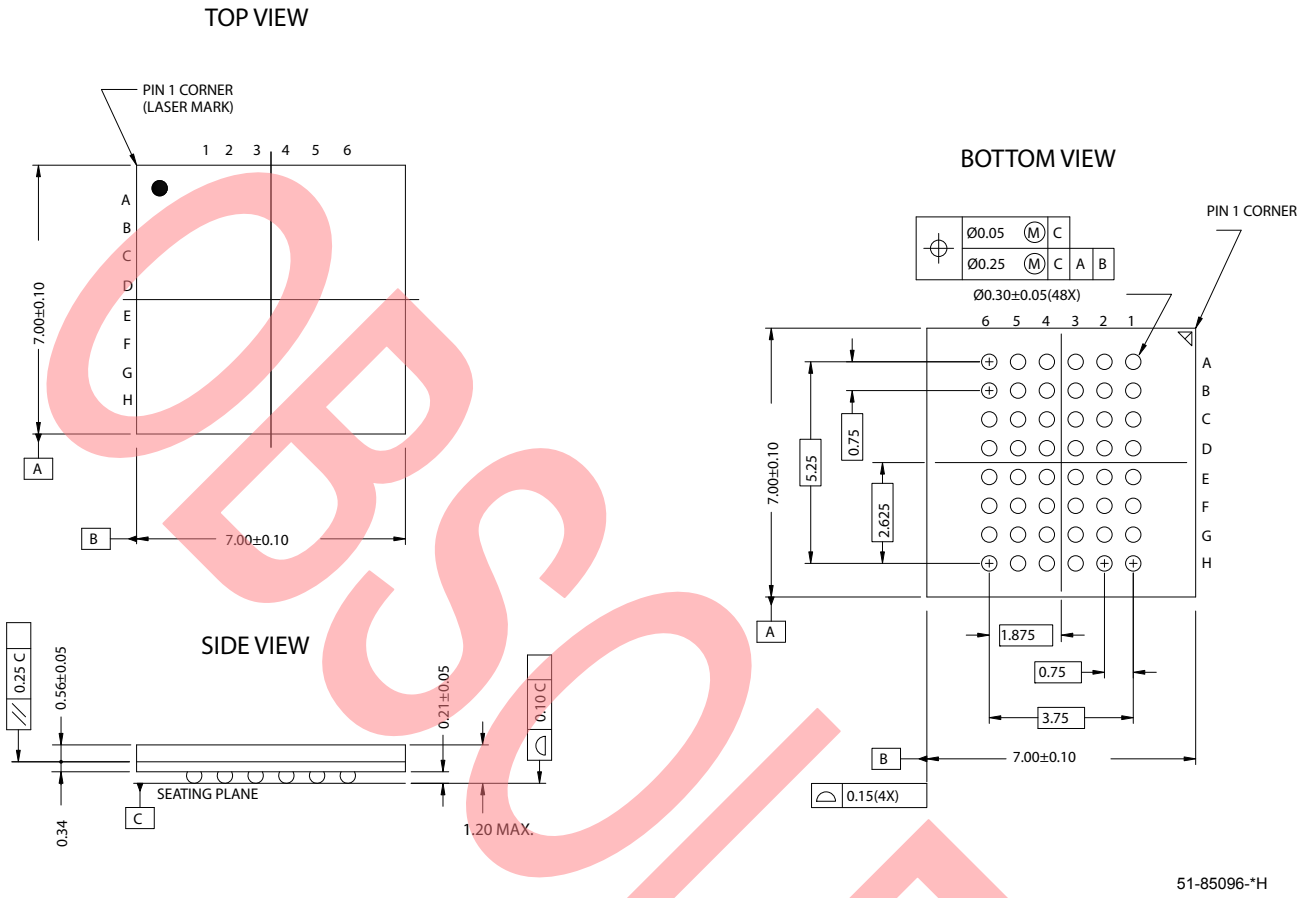


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48-Ball (7.00 mm x 7.00 mm) FBGA (51-85096)



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Document History Page

Document Title: CY62136VN MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 001-06510				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	426503	See ECN	RXU	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table
*B	2897932	03/23/2010	VKN	Removed Automotive-E information Updated ordering Information table Updated TSOPII and FBGA package outline diagram
*C	3094203	11/24/2010	RAME	The specified parts in the ordering information table is being pruned. Obsolete datasheet.

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