

128K x 8 HIGH-SPEED CMOS STATIC RAM

MARCH 2018

FEATURES

HIGH SPEED: (IS63/64WV1288DALL/DBLL)

- High-speed access time: 8, 10, 12, 20 ns
- Low Active Power: 135 mW (typical)
- Low Standby Power: 12 μ W (typical)
CMOS standby

LOW POWER: (IS63/64WV1288DALS/DBLS)

- High-speed access time: 25, 35 ns
- Low Active Power: 55 mW (typical)
- Low Standby Power: 12 μ W (typical)
CMOS standby
- Single power supply
 - V_{DD} 1.65V to 2.2V (IS63WV1288DAxx)
 - V_{DD} 2.4V to 3.6V (IS63/64WV1288DBxx)
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- $\overline{\text{CE}}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Lead-free available

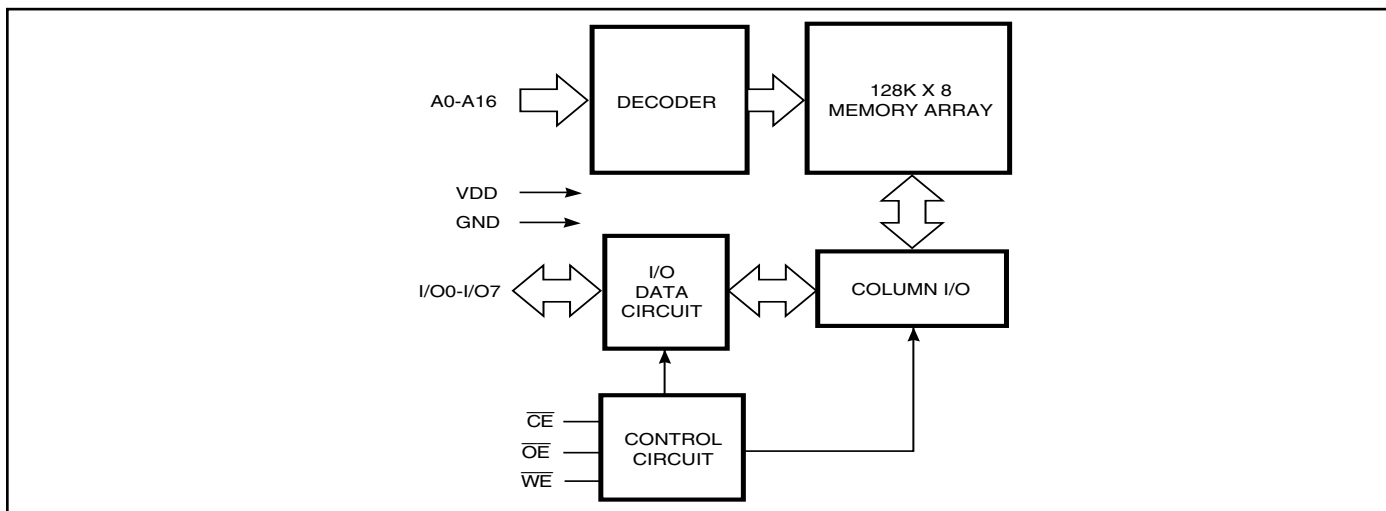
DESCRIPTION

The *ISSI* IS63/64WV1288Dxxx is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM. The IS63/64WV1288DBLL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 25 μ W (typical) with CMOS input levels.

The IS63/64WV1288DBLL operates from a single V_{DD} power supply. The IS63/64WV1288Dxxx is available in 32-pin TSOP (Type II), 32-pin sTSOP (Type I), 48-Ball miniBGA (6mm x 8mm), 32-pin SOJ (400-mil) and 32-pin SOJ (300-mil) packages.

FUNCTIONAL BLOCK DIAGRAM



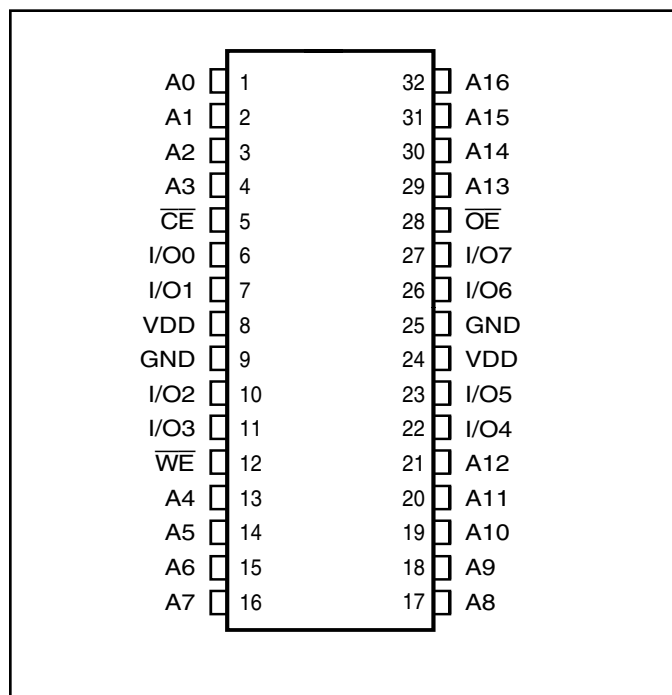
Copyright © 2018 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATION

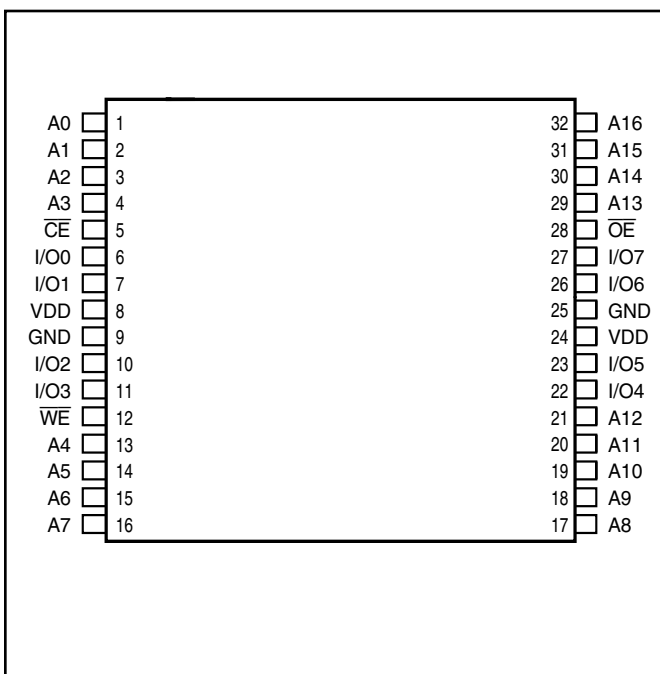
32-Pin SOJ



PIN CONFIGURATION

32-Pin TSOP (Type II) (T)

32-Pin sTSOP (Type I) (H)

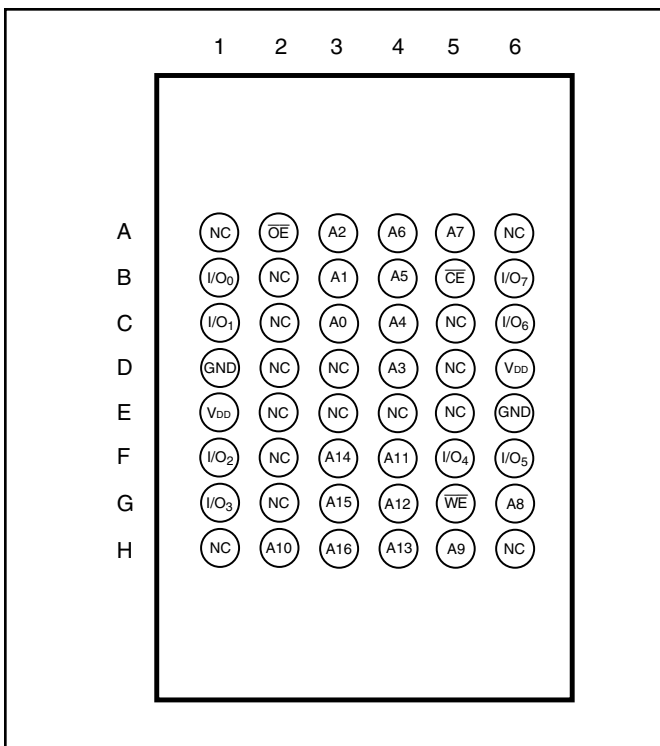


PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
VDD	Power
GND	Ground

PIN CONFIGURATION

48-mini BGA (B) (6 mm x 8 mm)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V _{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{cc1} , I _{cc2}
Read	H	L	L	D _{OUT}	I _{cc1} , I _{cc2}
Write	L	L	X	D _{IN}	I _{cc1} , I _{cc2}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{DD} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.5	W
V _{DD}	V _{DD} Related to GND	-0.2 to +3.9	V

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V $\pm$ 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD} / 2$	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 (Ω)	1909	317	13500
R2 (Ω)	1105	351	10800
V_{TM} (V)	3.0V	3.3V	1.8V

AC TEST LOADS

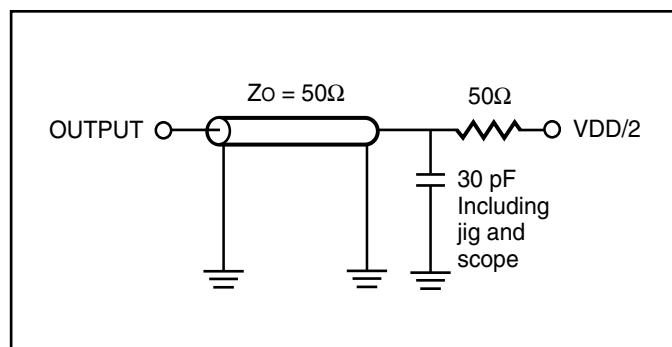


Figure 1.

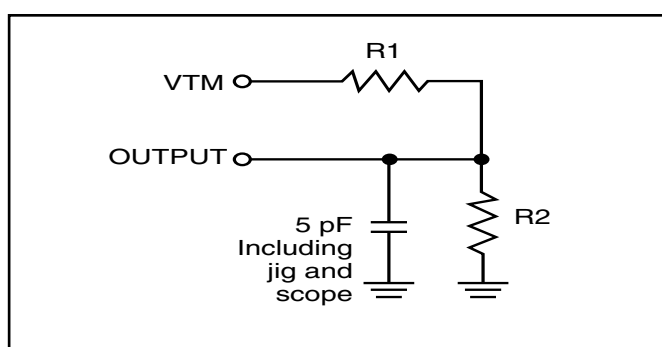


Figure 2.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	-1	1	μA

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -1.0 mA	1.8	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 1.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	-1	1	μA

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V _{DD}	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V _{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V _{DD} + 0.2	V
V _{IL} ⁽¹⁾	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}		-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled		-1	1	μA

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

HIGH SPEED (IS63WV1288DALL/DBLL)

OPERATING RANGE (V_{DD}) (IS63WV1288DALL)

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	-40°C to +85°C	1.65V-2.2V	20ns
Automotive	-40°C to +125°C	1.65V-2.2V	20ns

OPERATING RANGE (V_{DD}) (IS63WV1288DBLL)⁽¹⁾

Range	Ambient Temperature	V _{DD} (8 ns) ¹	V _{DD} (10 ns) ¹
Commercial	0°C to +70°C	3.3V ± 5%	2.4V-3.6V
Industrial	-40°C to +85°C	3.3V ± 5%	2.4V-3.6V

Note:

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV1288DBLL)⁽²⁾

Range	Ambient Temperature	V _{DD} (8 ns) ²	V _{DD} (10 ns) ²
Automotive	-40°C to +125°C	3.3V ± 5%	2.4V-3.6V

Note:

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-8		-10		-12		-20		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max.,	Com.	—	65	—	50	—	45	—	40	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	70	—	55	—	50	—	45	
		CE = V _{IL}	Auto. ⁽³⁾	—	—	—	65	—	55	—	50	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V	typ. ⁽²⁾			45		45				
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	40	—	40	—	40	—	40	μA
		CE ≥ V _{DD} - 0.2V,	Ind.	—	55	—	55	—	55	—	55	
		V _{IN} ≥ V _{DD} - 0.2V, or	Auto.	—	—	—	90	—	90	—	90	
		V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾			4		4				

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.
- For Automotive grade at 15ns, typ. I_{CC} = 38mA, not 100% tested.

LOW POWER (IS63WV1288DALS/DBLS)

OPERATING RANGE (V_{DD}) (IS63WV1288DALS)

Range	Ambient Temperature	V_{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	-40°C to +85°C	1.65V-2.2V	45ns
Automotive	-40°C to +125°C	1.65V-2.2V	55ns

OPERATING RANGE (V_{DD}) (IS63WV1288DBLS)

Range	Ambient Temperature	V_{DD} (35 ns)
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	-40°C to +85°C	2.4V-3.6V

OPERATING RANGE (V_{DD}) (IS64WV1288DBLS)

Range	Ambient Temperature	V_{DD} (35 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-25		-35		-45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max.,	Com.	—	15	—	15	—	12	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	20	—	20	—	18	
		$\overline{CE}$ = V _{IL}	Auto.	—	30	—	30	—	25	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V	typ. ⁽²⁾		18					
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	40	—	40	—	40	μA
		$\overline{CE}$ ≥ V _{DD} - 0.2V,	Ind.	—	50	—	50	—	50	
		V _{IN} ≥ V _{DD} - 0.2V, or	Auto.	—	75	—	75	—	75	
		V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾		4					

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t _{AA}	Address Access Time	—	8	—	10	—	12	ns
t _{OHA}	Output Hold Time	2	—	2	—	2	—	ns
t _{ACE}	$\overline{\text{CE}}$ Access Time	—	8	—	10	—	12	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	4	—	5	—	6	ns
t _{LZOE} ⁽²⁾	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	0	—	ns
t _{HZOE} ⁽²⁾	$\overline{\text{OE}}$ to High-Z Output	0	4	0	5	0	6	ns
t _{LZCE} ⁽²⁾	$\overline{\text{CE}}$ to Low-Z Output	3	—	3	—	3	—	ns
t _{HZCE} ⁽²⁾	$\overline{\text{CE}}$ to High-Z Output	0	4	0	5	0	6	ns
t _{PU}	$\overline{\text{CE}}$ to Power Up Time	0	—	0	—	0	—	ns
t _{PD}	$\overline{\text{CE}}$ to Power Down Time	—	8	—	10	—	12	ns

Notes:

- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V loading specified in Figure 1.
- Tested with the loading specified in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

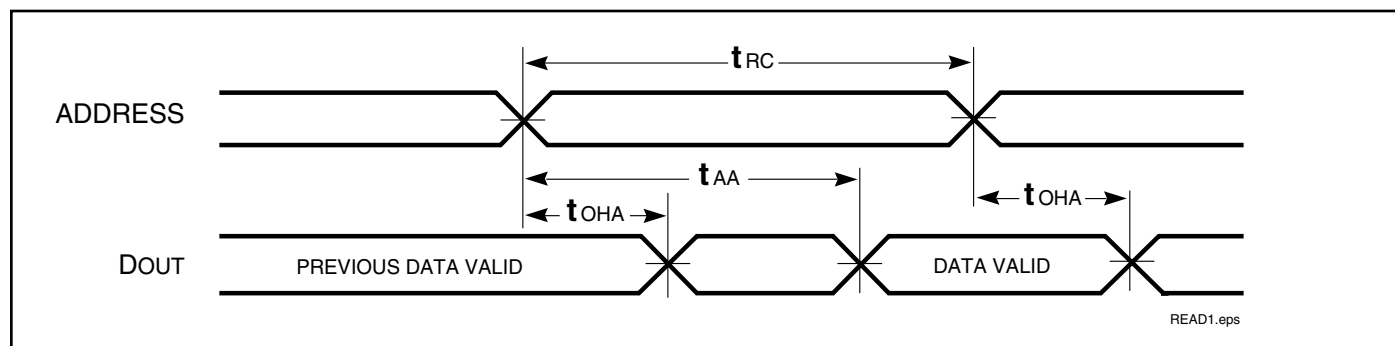
Symbol	Parameter	-20 ns		-25 ns		-35 ns		-45 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t _{OHA}	Output Hold Time	2.5	—	6	—	8	—	10	—	ns
t _{ACE}	$\overline{\text{CE}}$ Access Time	—	20	—	25	—	35	—	45	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	8	—	12	—	15	—	20	ns
t _{HZOE} ⁽²⁾	$\overline{\text{OE}}$ to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZOE} ⁽²⁾	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t _{HZCE} ⁽²⁾	$\overline{\text{CE}}$ to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZCE} ⁽²⁾	$\overline{\text{CE}}$ to Low-Z Output	3	—	10	—	10	—	10	—	ns

Notes:

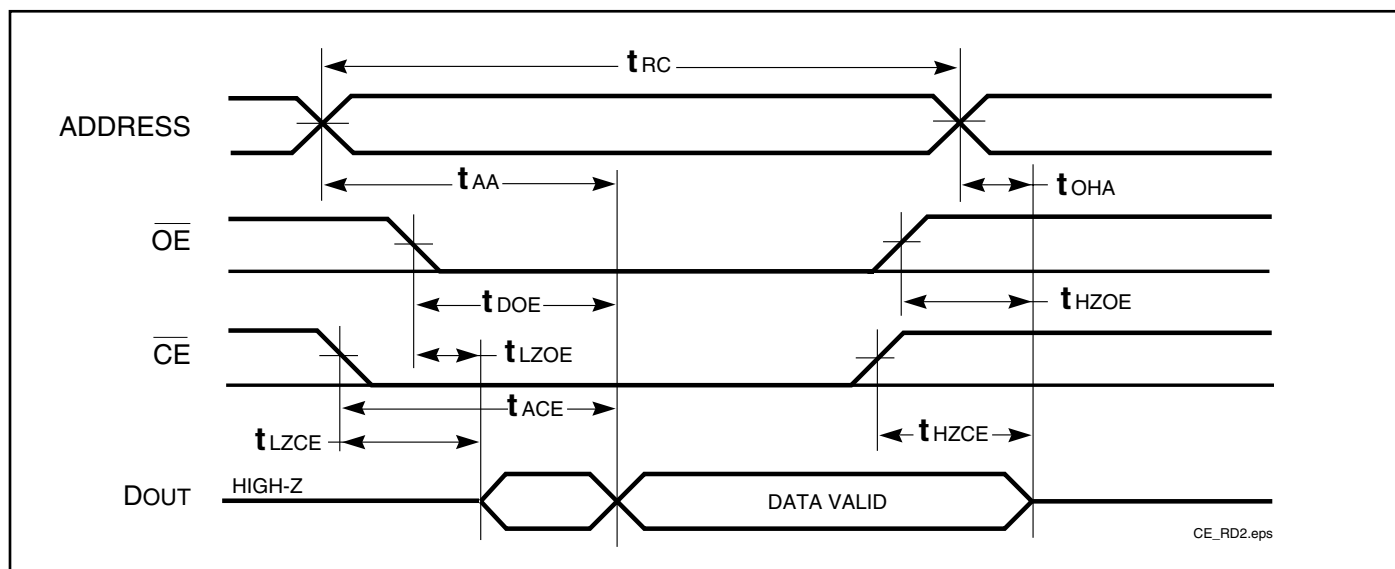
- Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
- Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
- Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t _{SCE}	CE to Write End	7	—	7	—	8	—	ns
t _{AW}	Address Setup Time to Write End	8	—	8	—	8	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWE₁} ⁽¹⁾	WE Pulse Width (OE High)	7	—	7	—	8	—	ns
t _{PWE₂} ⁽²⁾	WE Pulse Width (OE Low)	8	—	10	—	12	—	ns
t _{SD}	Data Setup to Write End	5	—	5	—	6	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	WE LOW to High-Z Output	—	4	—	5	—	6	ns
t _{LZWE} ⁽²⁾	WE HIGH to Low-Z Output	3	—	3	—	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

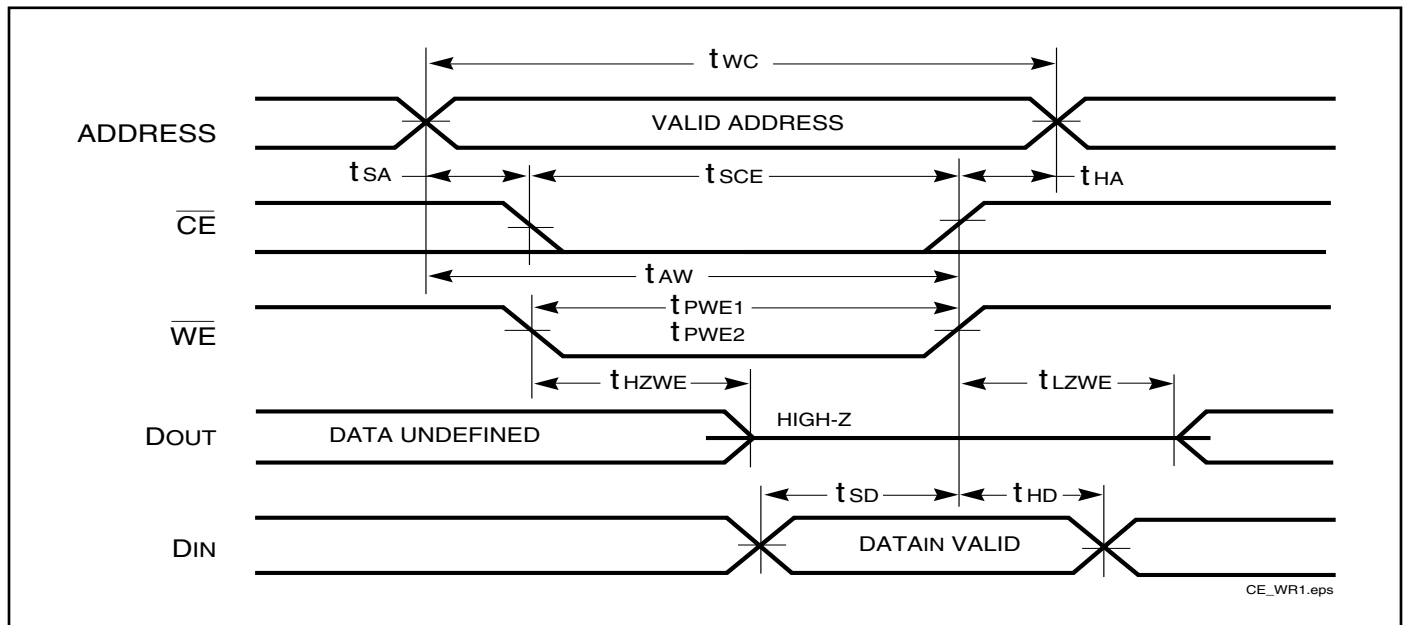
Symbol	Parameter	-20 ns		-25 ns		-35 ns		-45ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t _{SCE}	CE to Write End	12	—	18	—	25	—	35	—	ns
t _{AW}	Address Setup Time to Write End	12	—	15	—	25	—	35	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWE1}	WE Pulse Width (OE = HIGH)	12	—	18	—	30	—	35	—	ns
t _{PWE2}	WE Pulse Width (OE = LOW)	17	—	20	—	30	—	35	—	ns
t _{SD}	Data Setup to Write End	9	—	12	—	15	—	20	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE} ⁽³⁾	WE LOW to High-Z Output	—	9	—	12	—	20	—	20	ns
t _{LZWE} ⁽³⁾	WE HIGH to Low-Z Output	3	—	5	—	5	—	5	—	ns

Notes:

1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and UB or LB, and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

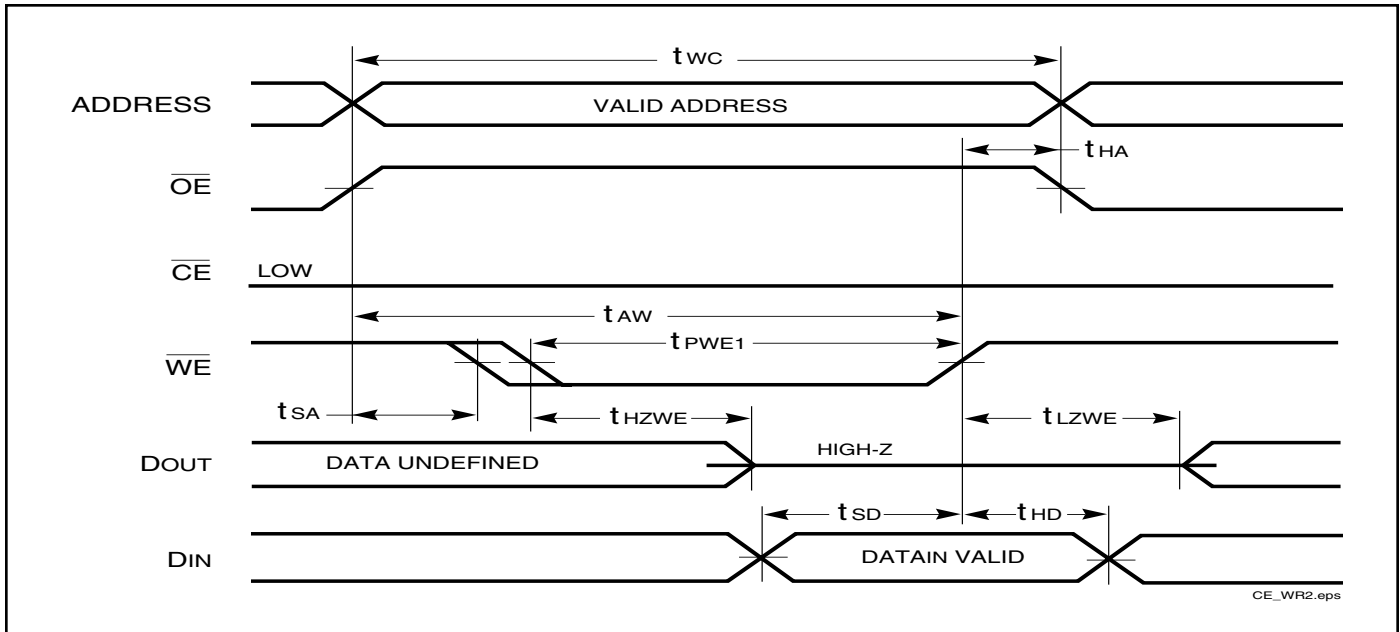
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

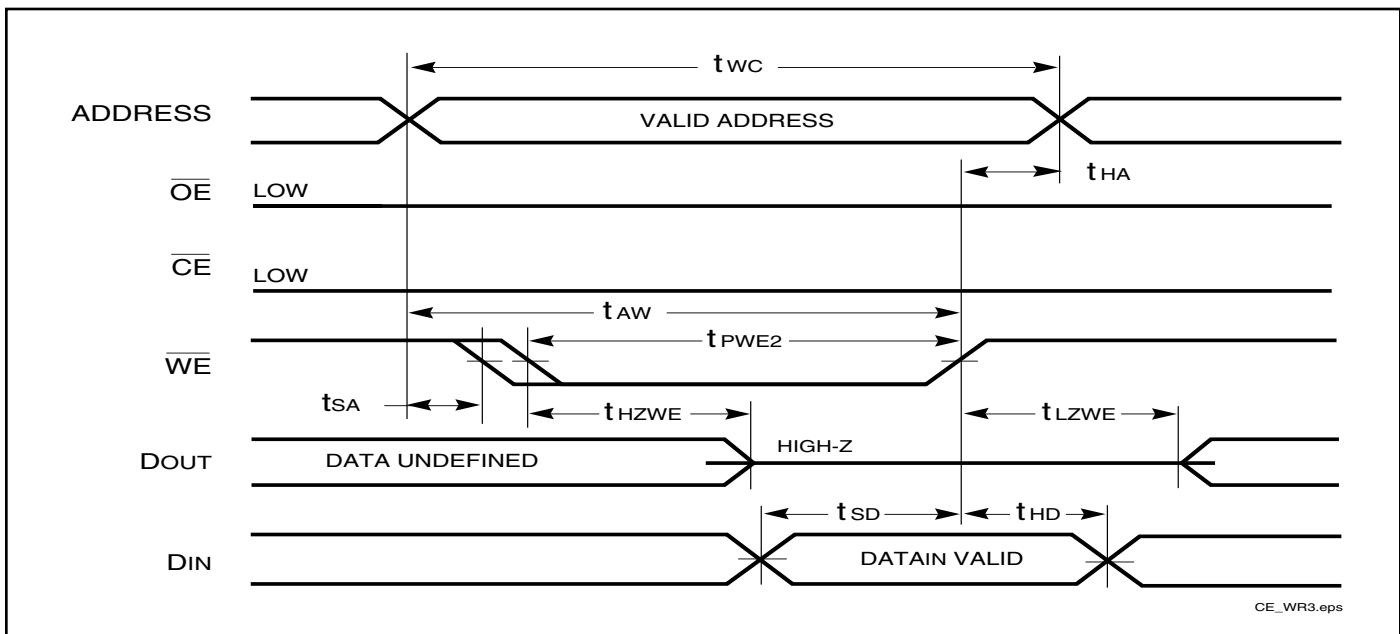


AC WAVEFORMS

WRITE CYCLE NO. 2⁽¹⁾ ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

HIGH SPEED (IS63/4WV1288DALL/DBLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	4 — —	40 55 90	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

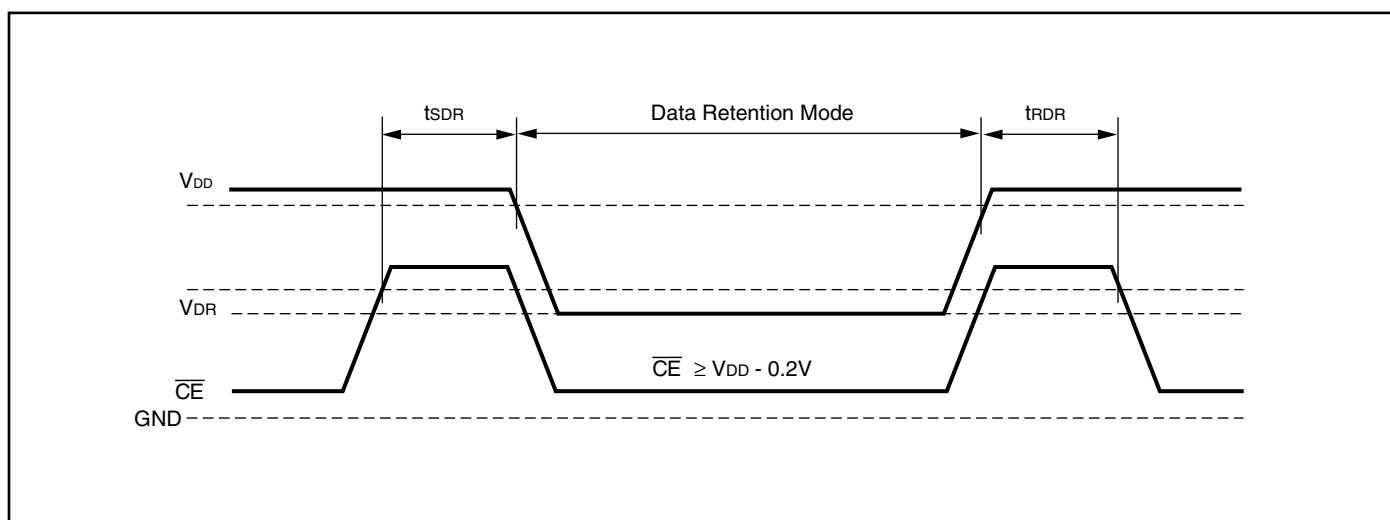
Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	4 — —	40 55 90	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



LOW POWER (IS63/4WV1288DALS/DBLS)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	4 — —	40 50 75	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

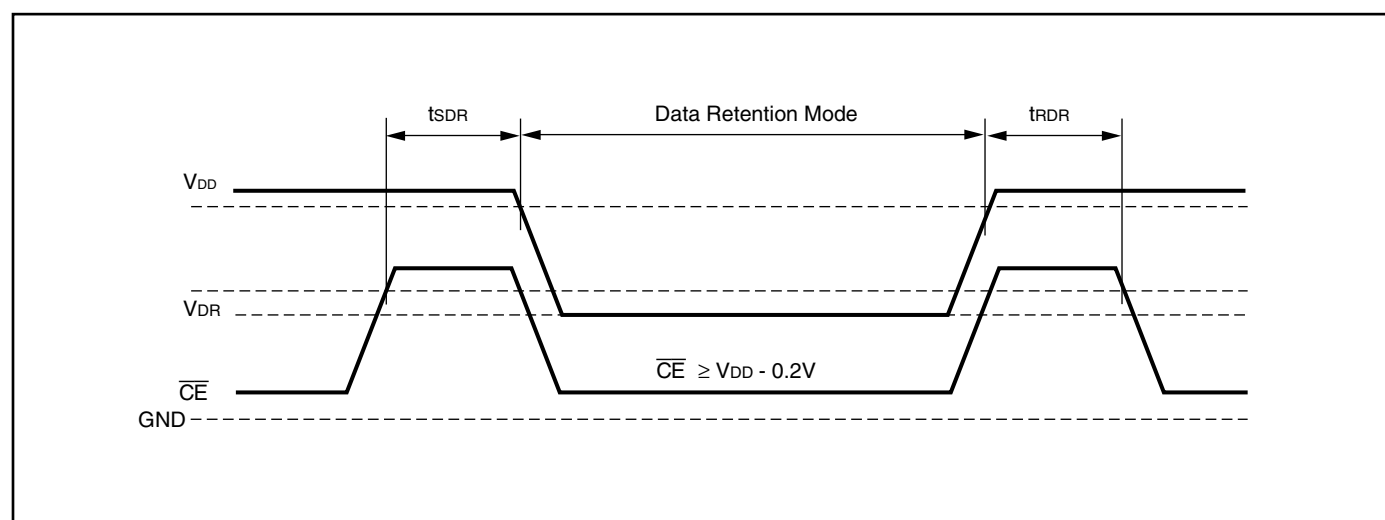
Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	4 — —	40 50 75	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Industrial Range: –40°C to +85°C

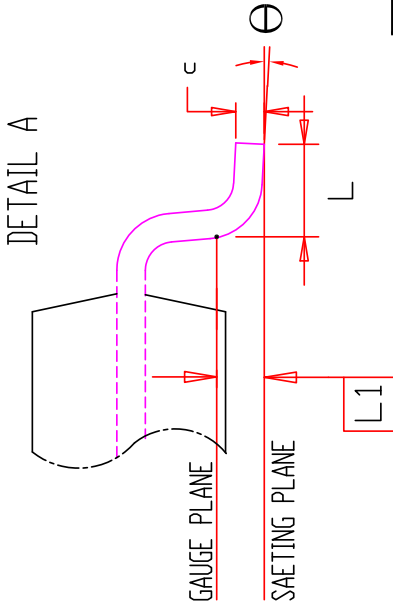
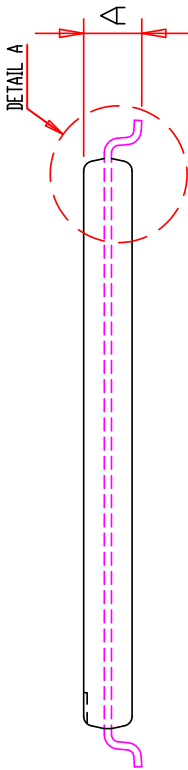
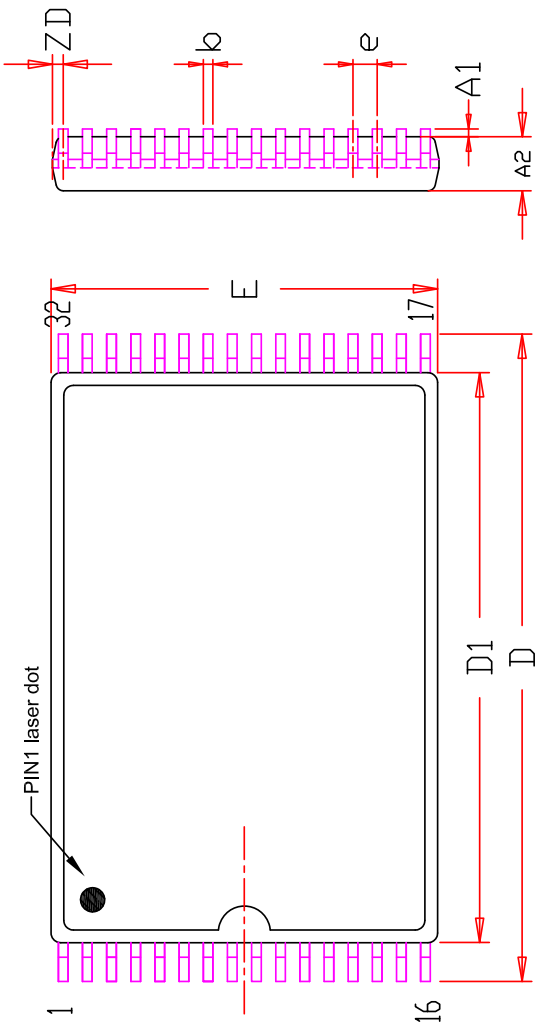
Speed (ns)	Order Part No.	Package
8	IS63WV1288DBLL-8TLI	32-pin TSOP (Type II), Lead-free
	IS63WV1288DBLL-8HLI	sTSOP (Type I) (8mm x13.4mm), Lead-free
	IS63WV1288DBLL-8JLI	32-pin SOJ (300-mil), Lead-free
10	IS63WV1288DBLL-10TLI	32-pin TSOP (Type II), Lead-free
	IS63WV1288DBLL-10HLI	sTSOP (Type I) (8mm x13.4mm), Lead-free
	IS63WV1288DBLL-10JLI	32-pin SOJ (300-mil), Lead-free
	IS63WV1288DBLL-10KLI	32-pin SOJ (400-mil), Lead-free

Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
10(8*)	IS64WV1288DBLL-10CTLA3	32-pin TSOP (Type II), Copper Lead frame, Lead-free
	IS64WV1288DBLL-10HLA3	sTSOP (Type I) (8mm x13.4mm), Lead-free

Note:

1. Speed = 8ns for V_{DD} = 3.3V + 5%. Speed = 10ns for V_{DD} = 2.4V-3.6V.



NOTE :

- 1. Controlling Dimension : mm
- 2. Dimension D1 and E do not include mold protrusion.
- 3. Dimension b does not include dambar protrusion/intrusion.
- 4. Reference Document : JEDEC MO-183
- 5. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°
c	0.10		0.21	0.004		0.008

CASE 1



TITLE

32L 8x13.4mm TSOP-1
Package Outline

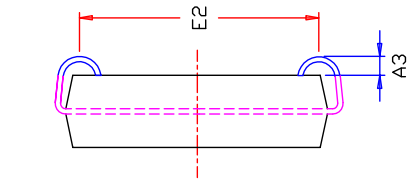
REV.

F

DATE

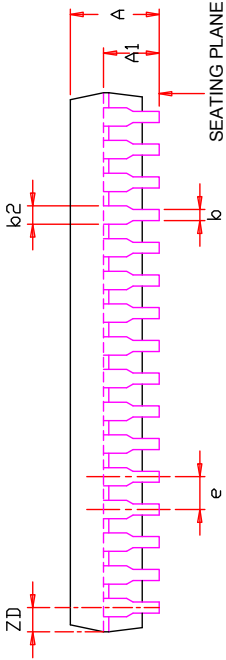
06/21/2017

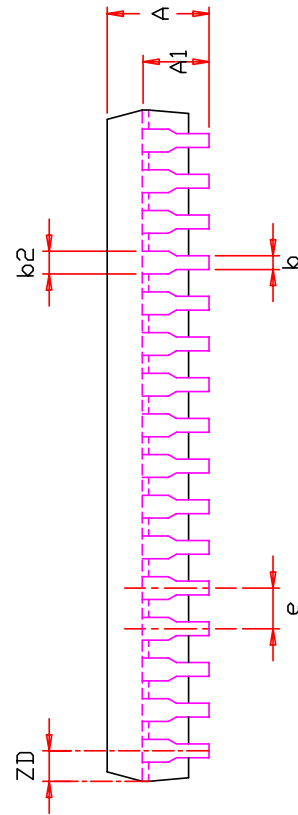
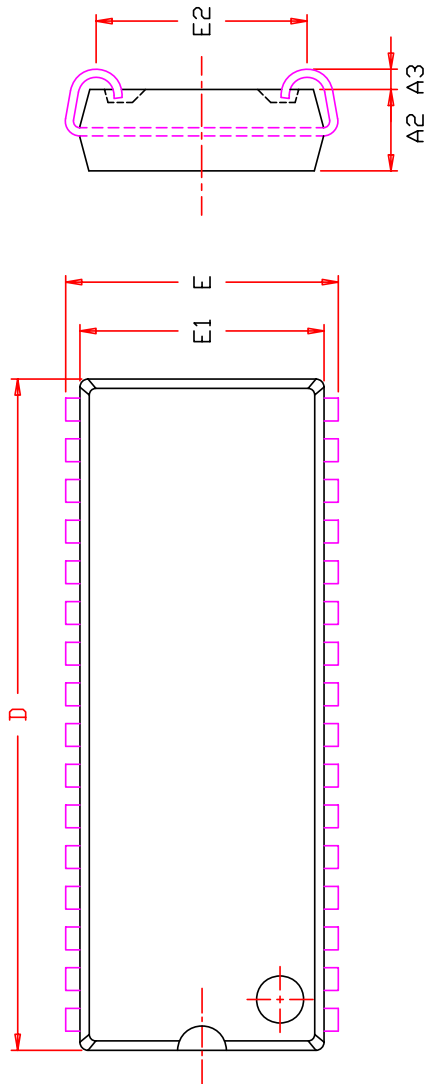
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MTN.	NDM.	MAX.	MTN.	NDM.	MAX.
A	3.25		3.76	0.128		0.148
A1	2.08			0.082		
A3	0.635			0.025		
b	0.38		0.51	0.015		0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40	BSC		0.370	BSC	
e	1.27	BSC		0.050	BSC	
ZD	0.95	REF		0.037	REF	



NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027 .





NOTE :

- 1. CONTROLLING DIMENSION : MM
- 2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.05		3.76		0.120	0.148
A1	2.08		2.41		0.082	0.095
A2	2.41	2.54	2.67	0.095	0.100	0.105
A3	0.64		1.09	0.025		0.043
b	0.41		0.51	0.016		0.020
b2	0.66		0.81	0.026		0.032
D	20.82		21.09	0.820		0.830
E	8.38	8.51	8.64	0.330	0.335	0.340
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.48		6.99	0.255		0.275
e		1.27 BSC.		0.050 BSC.		
ZD		0.95 REF.		0.037 REF.		



32L 300mil SOJ
Package Outline

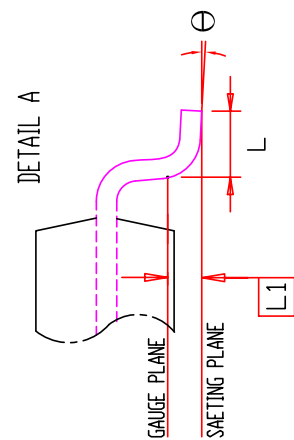
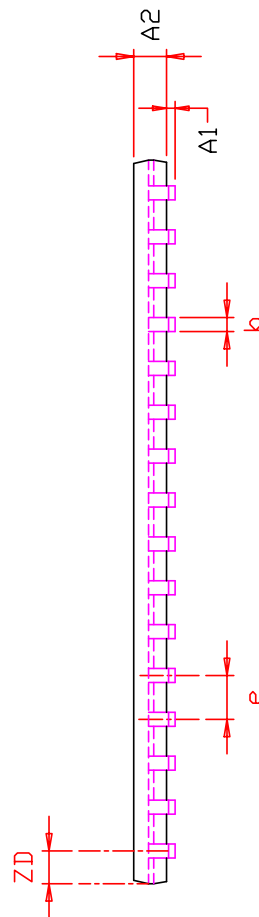
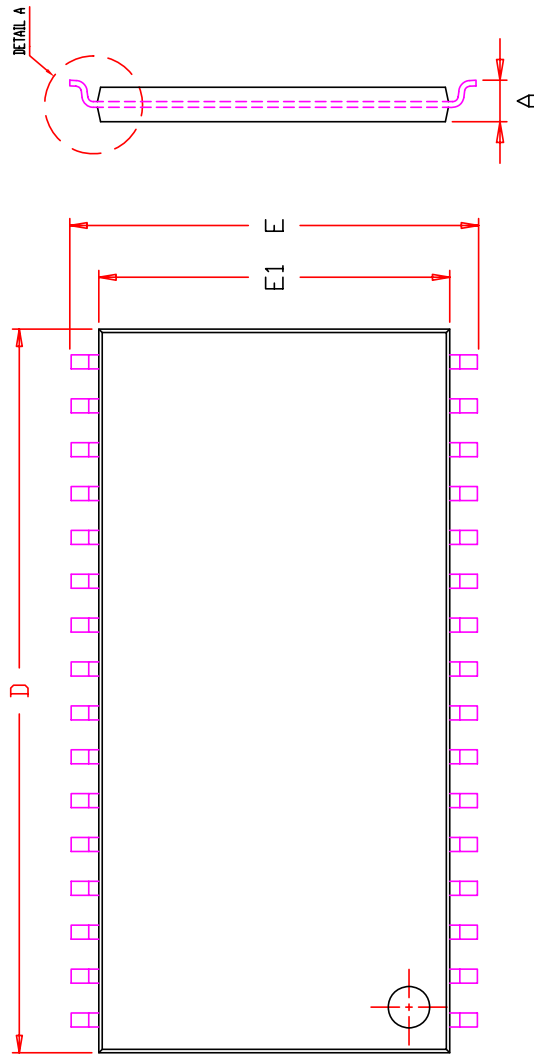
TITLE

REV.

C

DATE

08/14/2009



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.52	0.012		0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		1.27	BSC.		0.050	BSC.
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.25	BSC.		0.010	BSC.
ZD		0.95	REF.		0.037	REF.
theta	0		8°	0		8°



TITLE
32L 400mil TSOP-2
Package Outline

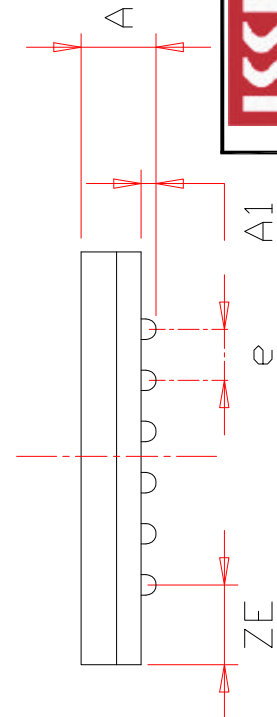
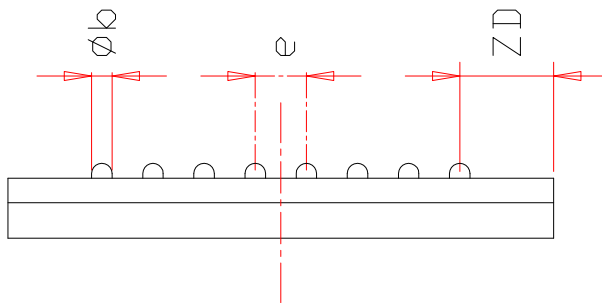
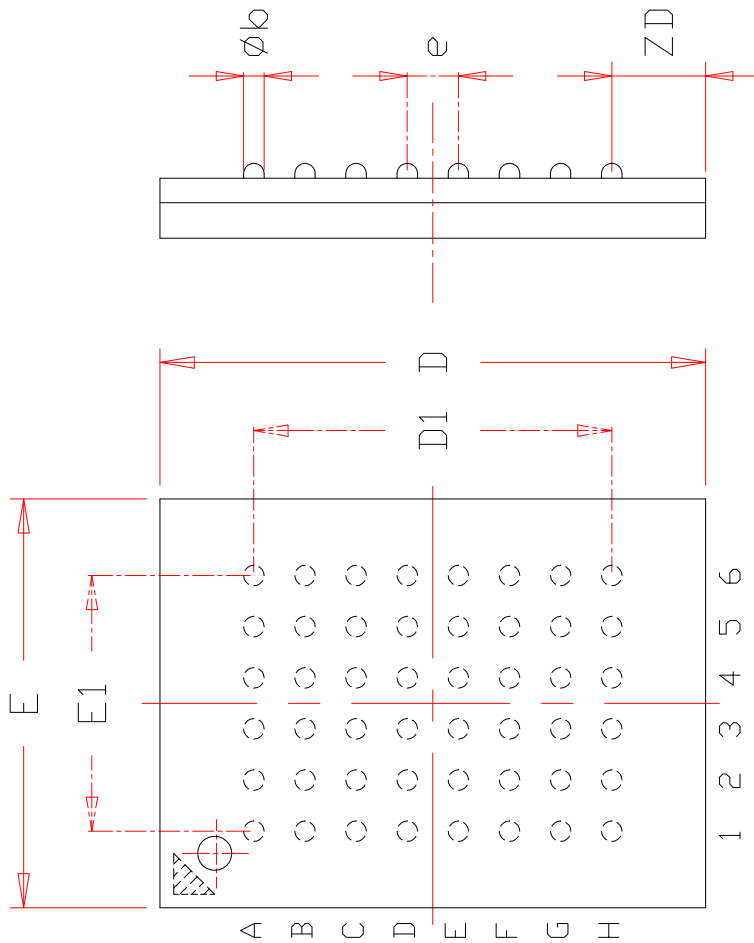
REV.

E

DATE

06/23/2009

TOP VIEW



NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC.			0.030 BSC.		
ZD	1.375 REF.			0.054 REF.		
ZE	1.125 REF.			0.044 REF.		



TITLE

48L 6x8mm TF-BGA
Package Outline

REV.

C

DATE

08/12/2008