

Evaluation Board User's Manual for NB4L16M

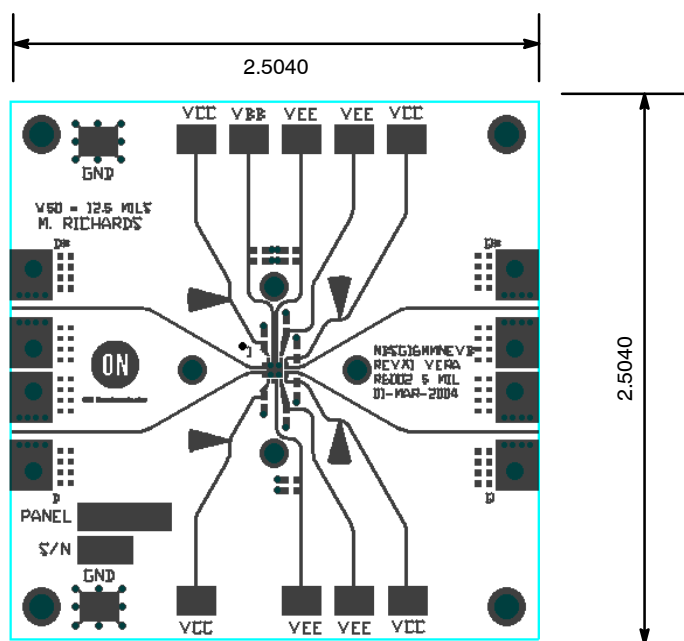


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EVAL BOARD USER'S MANUAL

The board is implemented in two layers and provides a high bandwidth 50 Ω controlled impedance environment for higher performance. The first layer or primary trace layer is 5 mils thick Rogers RO6002 material, which is engineered

- Jitter
- Output Skew
- Gain/Return Loss
- Eye Pattern Generation
- Frequency Performance
- Output Rise and Fall Time
- V_{CMR} (Input High Common Mode Range)



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NB4L16MMNEVB

SETUP FOR TIME DOMAIN MEASUREMENTS

Table 1. BASIC EQUIPMENT

Description	Example Equipment (Note 1)	Qty.
Power Supply with 4 outputs	HP6624A	1
Oscilloscope	TDS8000 with 80E01 Sampling Head (Note 2)	1
Differential Signal Generator	HP 8133A, Advantest D3186	1
Matched High Speed Cables with SMA Connectors	Storm, Semflex	4
Power Supply Cables with Clips		8

- Equipment used to generate example measurements within this document.
- 50 GHz sampling head used (for effective rise, fall and jitter performance measurement)

Setup

Step 1: Connect Power

1a: Two power levels must be provided to the board for V_{CC} and V_{EE} via the surface mount clips.

Table 2. NB4L16M Power Supply Connections

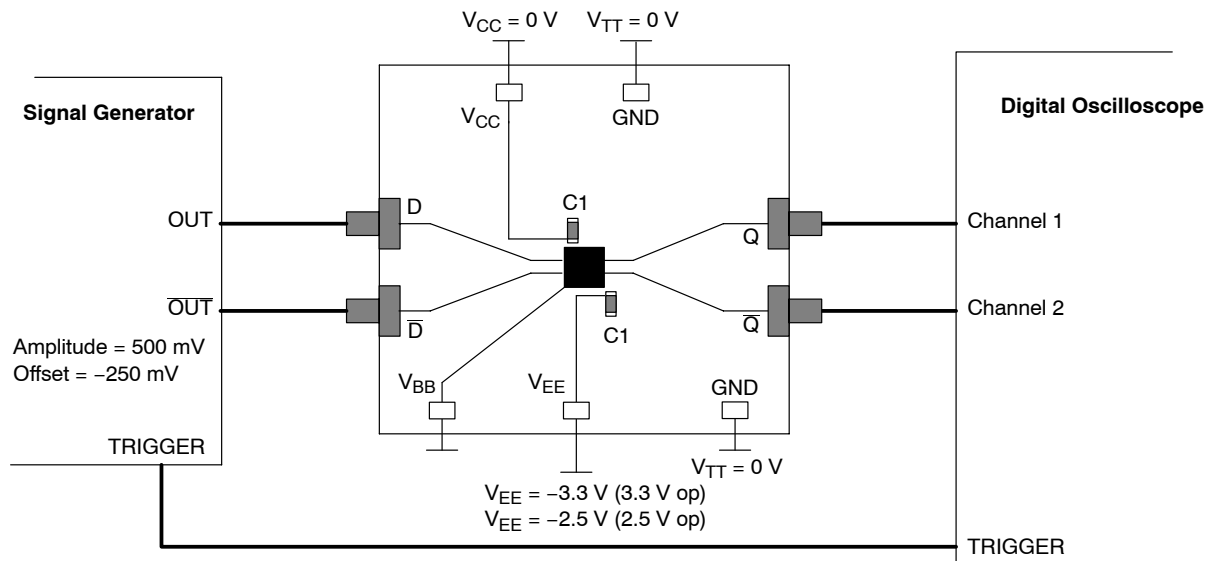
3.3 V Setup	2.5 V Setup
$V_{CC} = 0 \text{ V} = \text{GND}$	$V_{CC} = 0 \text{ V} = \text{GND}$
$V_{TT} = V_{CC} = 0 \text{ V} = \text{GND}$	$V_{TT} = V_{CC} = 0 \text{ V} = \text{GND}$
$V_{EE} = -3.3 \text{ V}$	$V_{EE} = -2.5 \text{ V}$

Step 2: Connect Inputs

For Differential Mode (3.3 V and 2.5 V operation)

2a: Connect the differential output of the generator to the differential input of the device (D and $\bar{D}$).

NOTE: Device may oscillate when the input is not driven.



NOTE: All differential cable pairs must be matched.

Figure 2. NB4L16M Board Setup – Time Domain (Differential Mode)

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Step 3: Setup Input Signals

3a: Set the signal generator amplitude to 500 mV.

NOTE: The signal generator amplitude can vary from 75 mV to 900 mV to produce a 400 mV DUT output.

3b: Set the signal generator offset to -250 mV.

NOTE: The V_{IHCMR} (Input High Voltage Common Mode Range) allows the signal generator offset to vary as long as V_{IH} is within the V_{IHCMR} range. Refer to the device data sheet for further information.

3c: Set the generator output for a PRBS data signal, or for a square wave clock signal with a 50% duty cycle.

Step 4: Connect Output Signals

4a: Connect the outputs of the device (Q , $\bar{Q}$) to the oscilloscope. The oscilloscope sampling head must have internal 50 Ω termination to ground.

NOTE: Where a single output is being used, the unconnected output for the pair ***must be*** terminated to V_{TT} through a 50 Ω resistor for best operation. Unused pairs may be left unconnected. Since $V_{TT} = 0$ V, a standard 50 Ω SMA termination is recommended.

SETUP FOR FREQUENCY DOMAIN MEASUREMENTS

Table 3. BASIC EQUIPMENT

Description	Example Equipment (Note 3)	Qty
Power Supply with 4 outputs	HP 6624A	1
Vector Network Analyzer (VNA)	R&S ZVK (10 MHz to 40 GHz)	1
180° Hybrid Coupler	Krytar Model #4010180	1
Bias Tee with 50 Ω Resistor Termination	Picosecond Model #5542-219	1
Matched High Speed Cables with SMA Connectors	Storm, Semflex	3
Power Supply Cables with Clips		8

3. Equipment used to generate example measurements within this document.

Setup

Step 1: Connect Power

1a: Two power levels must be provided to the board for V_{CC} and V_{EE} via the surface mount clips.

Table 4. NB4L16M Power Supply Connections

3.3 V Setup
$V_{CC} = 0$ V = GND
$V_{TT} = V_{CC} = 0$ V = GND
$V_{EE} = -3.3$ V

Setup Test Configurations for Differential Operation

Small Signal Setup

Step 2: Input Setup

2a: Calibrate VNA from 1.0 GHz to 12 GHz.

2b: Set input level to -35 dBm at the output of the 180° Hybrid coupler (input of the DUT).

Step 3: Output Setup

3a: Set display to measure S21 and record data.

Large Signal Setup

Step 2: Input Setup

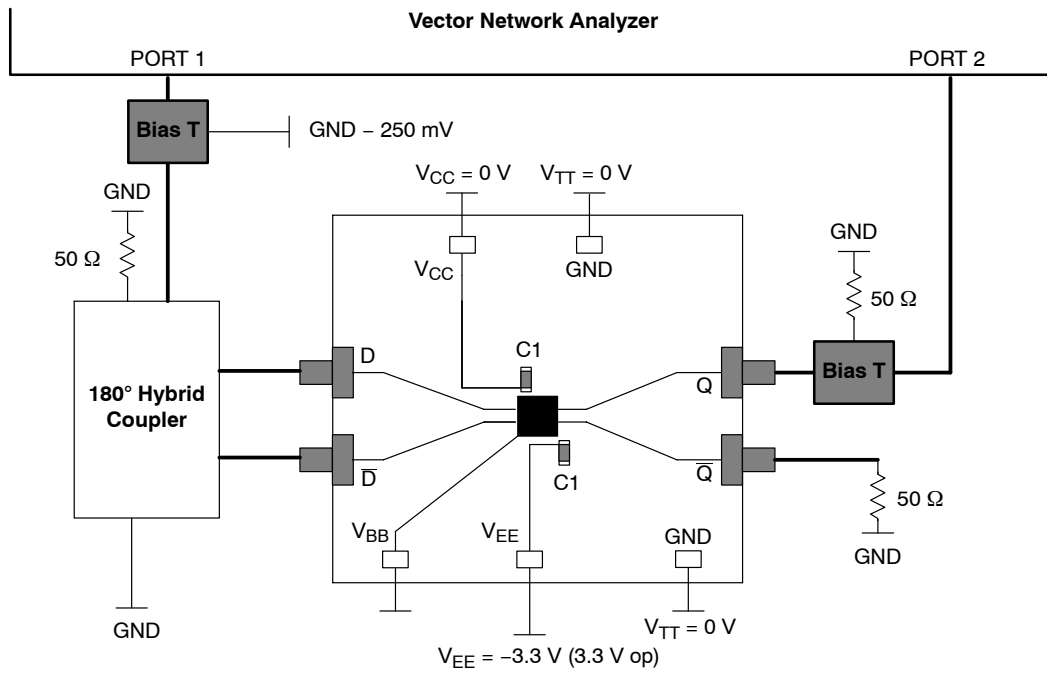
2a: Calibrate VNA from 1.0 GHz to 12 GHz.

2b: Set input levels to -2.0 dBm (500 mV) at the input of DUT.

Step 3: Output Setup

3a: Set display to measure S21 and record data.

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MORE INFORMATION ABOUT EVALUATION BOARD

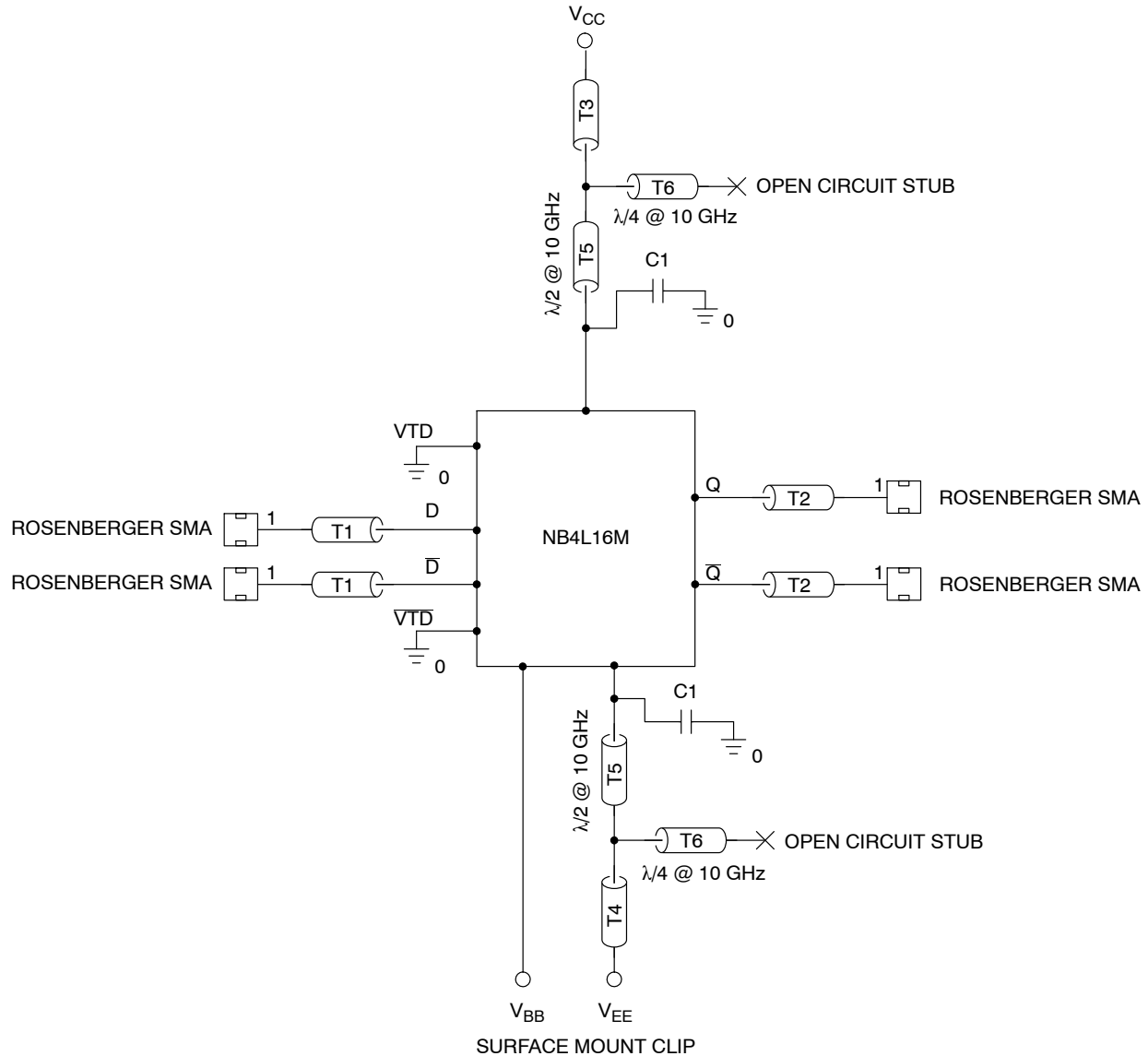
Design Considerations for >10 GHz operation

While the NB4L16M is specified to operate at 12 GHz, this evaluation board is designed to support operating frequencies up to 20 GHz.

The following considerations played a key role to ensure this evaluation board achieves high-end microwave performance:

- Optimal SMA connector launch
- Minimal insertion loss and signal dispersion
- Accurate Transmission line matching (50 ohms)
- Distributed effects while bypassing and noise filtering

SURFACE MOUNT CLIP



NOTE: C1, C2* = Decoupling cap
Tx = 50 Ω Transmission line

Figure 4. Evaluation Board Schematic

NB4L16MMNEVB

Table 5. PARTS LIST

Part No	Qty	Description	Manufacturer	WEB address
NB4L16MMN	1	2.5 V/3.3 V, 5 Gb/s Multi Level Clock/Data Input to CML Receiver/Driver/ Translator with Internal Termination	ON Semiconductor	http://www.onsemi.com
32K243-40ME3	4	Gold Plated Connector	Rosenberger	http://www.rosenberger.de
CO6BLBB2X5CO6 03CL04K6RAC	9	2 MHz – 30 GHz Capacitor 0603 0.1 μ F $\pm$ 10%	Dielectric Laboratories Kemet	http://www.dilabs.com http://www.newark.com/
SO16	9	Test Point-Anvil	Keystone	http://www.newark.com http://www.digikey.com

Table 6. BOARD MATERIAL

Material	Thickness
Rogers 6002	5 mil
Copper Plating	32 mil

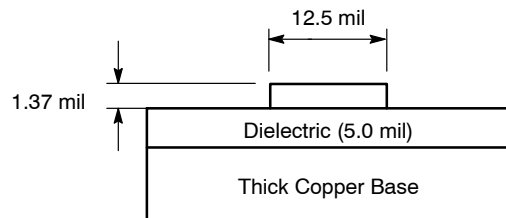


Figure 5. Board Stack-up

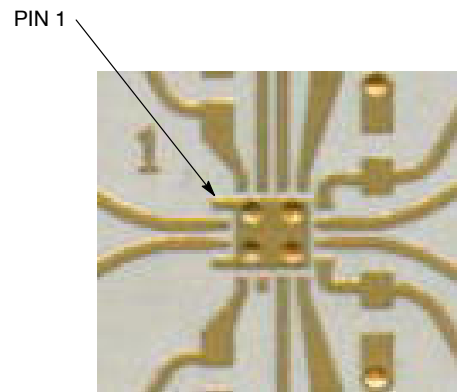
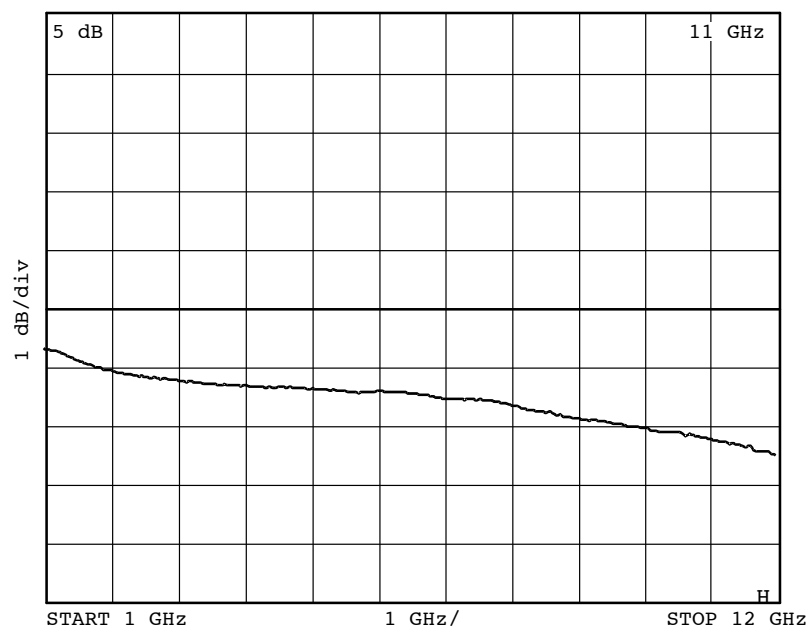


Figure 6. Layout Mask for NB4L16M



NOTE: The insertion loss curve can be used to calibrate out board loss if testing under small signal conditions.

Figure 7. Insertion Loss

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ADDITIONAL EVALUATION BOARD INFORMATION

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In all cases, the most up-to-date information can be found on our website.

- Sample orders for devices and boards
- New Product updates
- Literature download/order
- IBIS and Spice models

References

NB4L16M/D, Data Sheet, 2.5V/3.3V, 5 Gb/s Multi Level Clock/Data Input to CML Driver / Receiver / Buffer / Translator with Internal Termination

AND8077/D, Application Note, GigaComm™ (SiGe) SPICE Modeling Kit.

AND8075/D, Application Note, Board Mounting Considerations for the FCBGA Packages.

ORDERING INFORMATION

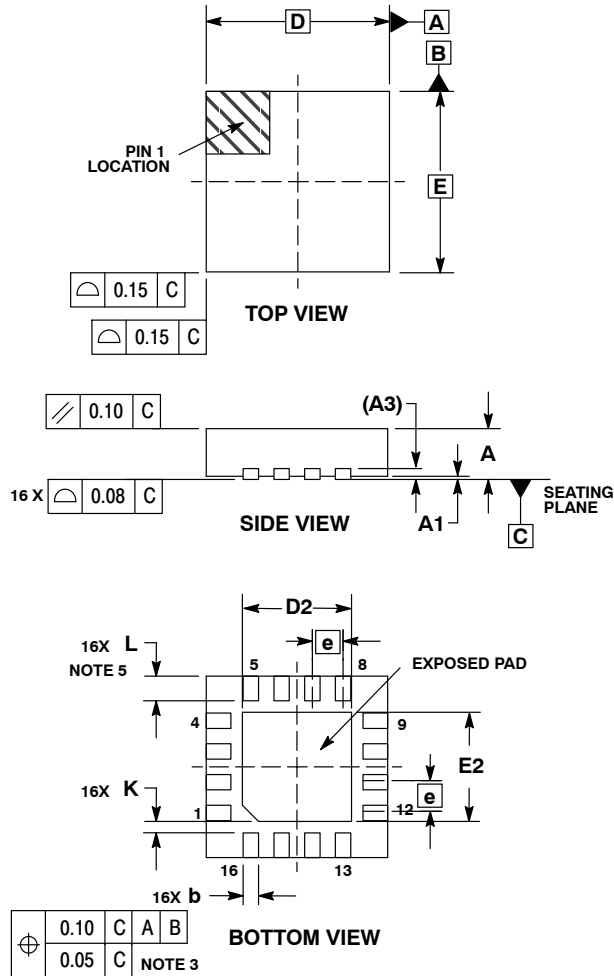
Part No	Description	Package	Shipping
NB4L16MMN	2.5V/3.3V, 5 Gb/s Multi Level Clock/Data Input to CML Driver / Receiver / Buffer / Translator with Internal Termination	3X3 mm QFN-16	123 Units/Tray
NB4L16MMNG	2.5V/3.3V, 5 Gb/s Multi Level Clock/Data Input to CML Driver / Receiver / Buffer / Translator with Internal Termination	3X3 mm QFN-16 (Pb-Free)	123 Units/Tray
NB4L16MMNR2	2.5V/3.3V, 5 Gb/s Multi Level Clock/Data Input to CML Driver / Receiver / Buffer / Translator with Internal Termination	3X3 mm QFN-16	3000 / Tape & Reel
NB4L16MMNEVB	NB4L16MN Evaluation Board		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB4L16MMNEVB

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.20	---
L	0.30	0.50

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