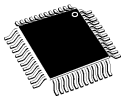
STM32C542xx

Datasheet

Arm® Cortex®-M33 32-bit MCU with FPU, 144 MHz, 593 CoreMark®, 256-Kbyte dual-bank flash memory, 64-Kbyte RAM, I3C, cryptography



LQFP32 (7 x 7 mm)
LQFP48 (7 x 7 mm)
LQFP64 (10 x 10 mm)
TSSOP20 (6.5 x 4.4 mm)

UFQFPN32 (5 x 5 mm)
UFQFPN48 (7 x 7 mm)
UFQFPN24 (4 x 4 mm)
UFQFPN20 (3 x 3 mm)

Product summary	
STM32C542xx	STM32C542CC STM32C542EC STM32C542FC STM32C542KC STM32C542RC

Features

Includes ST state-of-the-art patented technology.

Core

- 32-bit Arm® Cortex®-M33 CPU with FPU, frequency up to 144 MHz, MPU, and DSP instructions

Benchmarks

- 593 CoreMark® (4.12 CoreMark®/MHz)

ART Accelerator

- 8-Kbyte instruction cache allowing 0-wait-state execution from flash and up to CPU maximum speed

Memories

- 256-Kbyte flash memory with ECC, 2 banks read-while-write
- 64-Kbyte SRAM including 32 Kbytes with ECC
- 64-Kbyte user data flash memory, 2 banks
- 4.5-Kbyte OTP (one-time programmable)

Clock, reset, and supply management

- 2.7 V to 3.6 V application supply and I/O
- POR, PDR, and PVD
- Embedded regulator (LDO)
- Internal oscillators:
  - 144 MHz HSI
    (with ± 1% accuracy over temperature range [-20°C : 130°C])
  - 160/144/100 MHz PSI
  - 32 kHz LSI
- External oscillators:
  - 4 to 50 MHz HSE
  - 32.768 kHz LSE
- Low-power modes: Sleep, Stop, and Standby

DMA controller to offload the CPU

- 2 x LPDMA with 8 channels (4 + 4)

Analog

- 1 × 12-bit ADC (12 external channels and 2 internal), up to 2.25 MSPS
- 2 × 12-bit DACs
- 2 × comparators
- 1 × Operational amplifier

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Up to 10 timers

- 6 × 16-bit (including 2 × 16-bit advanced motor controls, 1 × low-power 16-bit timer available in Stop mode) and 1 × 32-bit timers
- 2 × watchdogs
- 1 × SysTick timer
- RTC with hardware calendar, alarms, and calibration

Communication interfaces

- Up to 1 × I2C FM+ interface (SMBus/PMBus)
- Up to 1 × I3C
- Up to 2 × USARTs (ISO7816 interface, LIN, IrDA, modem control), 2 × UARTs, and 1 × LPUART
- Up to 2 × SPIs with muxed with full-duplex I2S for audio class accuracy via external clock and up to 2 × additional SPIs from 2 × USARTs when configured in synchronous mode
- 2 × FDCANs
- 1 × USB 2.0 full-speed host and device

Low-power modes

- Sleep, Stop, and Standby modes

Up to 52 I/O ports with interrupt capability

Security

- AES coprocessor
- HASH hardware accelerator (SHA-1, SHA-224, SHA-256, HMAC)
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- Flexible life-cycle scheme with RDP and password-protected regression

Mathematical coprocessor

- CORDIC for trigonometric functions acceleration

Bootloader support on USART, FDCAN, USB, and SPI interfaces

All packages are ECOPACK2 compliant.

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1 Introduction

This document provides information on STM32C542xx devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

For information on the Arm® Cortex®-M33 core, refer to the *Arm® Cortex®-M33 Processor Technical Reference Manual*, available from the www.arm.com website.

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2 Description

The STM32C542xx devices are general purpose microcontrollers family (STM32C5 series) based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 144 MHz.

The Cortex®-M33 core features a single-precision floating-point unit (FPU) that supports all the Arm® single-precision data-processing instructions and all the data types.

The Cortex®-M33 core also implements a full set of digital signal processing (DSP) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (up to 256-Kbyte flash memory and 64-Kbyte SRAM), and an extensive range of enhanced I/Os, peripherals connected to three APB buses, three AHB buses, and a 32-bit multi-AHB bus matrix.

The devices feature several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, and hide protection areas.

The devices embed several peripherals reinforcing security:

- HASH hardware accelerator
- True random number generator
- AES coprocessor

The devices offer one 12-bit ADC, two DAC channels, two comparators, one operational amplifier, a low-power RTC, one 32-bit general-purpose timer, two 16-bit PWM timers dedicated to motor control, two 16-bit general-purpose timers, two 16-bit basic timers, and one 16-bit low-power timer.

The devices also feature standard and advanced communication interfaces such as:

- One I^2C
- One I^3C
- Two SPIs with muxed full-duplex I2S
- Two USARTs, two UARTs, and one low-power UART
- Two FDCANs
- One USB full-speed

The devices operate in the -40 to +125 °C (+140 °C junction) temperature ranges from a 2.7 to 3.6 V power supply.

A comprehensive set of power-saving modes allows the design of low-power applications.

The devices offer multiple packages from 20 to 64 pins.

See Table 1 for the list of peripherals available for each part number.

Table 1. Device features and peripheral counts

Peripherals		STM32C542FCP	STM32C542FCU	STM32C542ECU	STM32C542KCT	STM32C542KCU	STM32C542CCT STM32C542CCU	STM32C542RCT
Number of pins		20	20	24	32	32	48	64
Flash memory (Kbytes)		256						
SRAM (Kbytes)		64 (including 32 with ECC)						
ICACHE (Kbytes)		8						
Data flash memory (Kbytes)		64						
One-time-programmable (Kbytes)		4.5						
Timers	General purpose	1 (32-bit) and 2 (16-bit)						
	Advanced-control	2						
	Basic	2						

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Peripherals		STM32C542FCP	STM32C542FCU	STM32C542ECU	STM32C542KCT	STM32C542KCU	STM32C542CCT STM32C542CCU	STM32C542RCT
Timers	Low-power	1						
	SysTick	1						
	Watchdog	2						
Communication interfaces	SPI (with I2S)	2						
	I2C	1						
	I3C	1						
	USART	2						
	UART	1			2			
	LPUART	1						
	USB	1						
	FDCAN	2						
	TRACE	No						Yes
CORDIC		Yes						
RTC		Yes (without LSE)					Yes	
Tamper pins		1		2			3	
True random number generator (RNG)		Yes						
HASH		Yes						
AES		Yes						
GPIOs		14		16	25	27	38	52
Wake-up pins		1		3			4	
12-bit ADC channels		4 external + 2 internal		5 external + 2 internal	8 external + 2 internal			12 external + 2 internal
12-bit DAC channels		2						
Analog comparator		2						
Operational amplifier		1						
Maximum CPU frequency (MHz)		144						
Operating voltage		2.7 V - 3.6 V						
Operating temperature		Junction temperature range: -40 to +140°C						
Packages		TSSOP20	UFQFPN20	UFQFPN24	LQFP32	UFQFPN32	LQFP48 UFQFPN48	LQFP64

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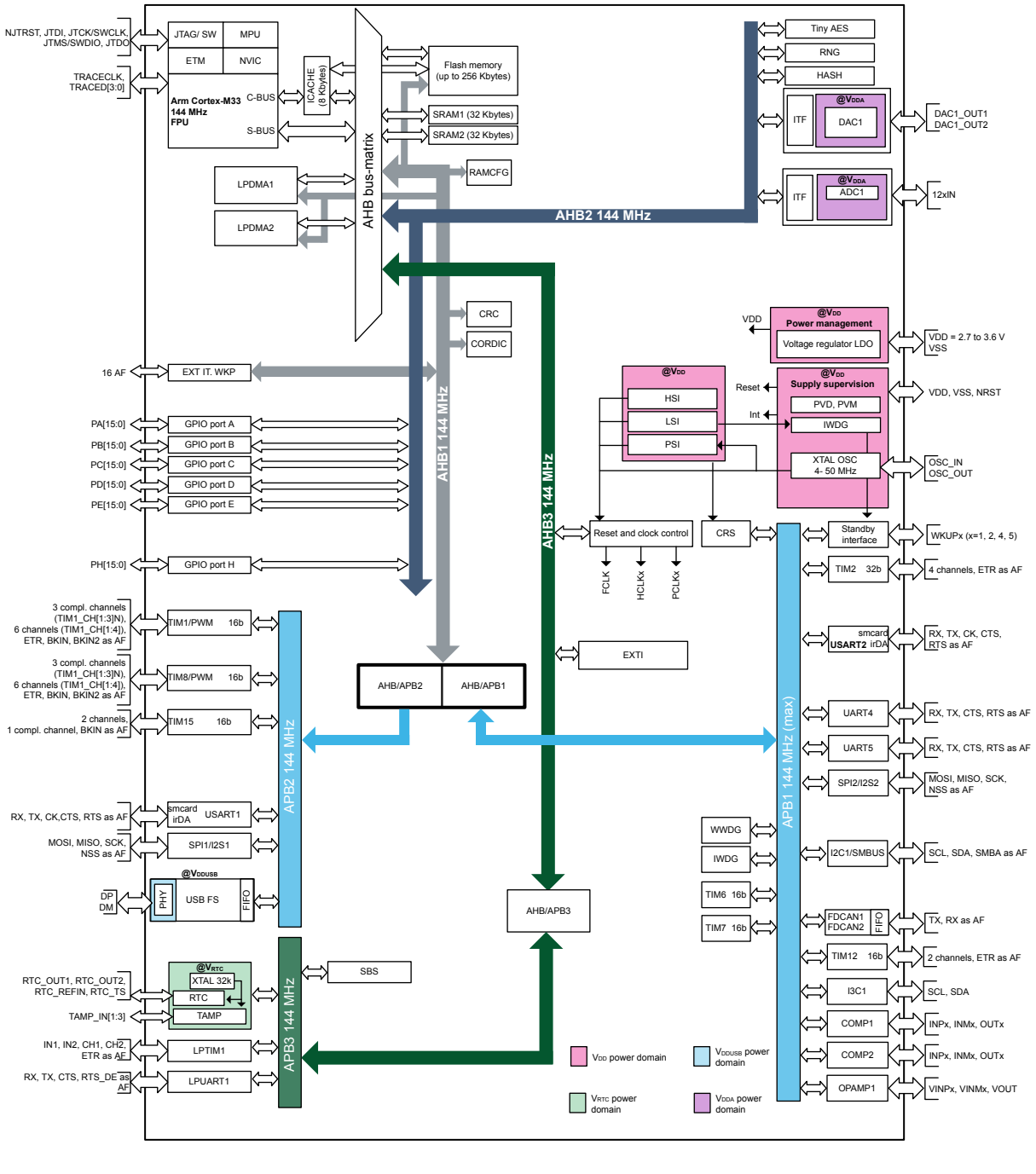
Figure 1 shows the general block diagram of the device family.

Figure 1. STM32C542xx block diagram



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3 Functional overview

3.1 Arm® Cortex®-M33 with FPU

The Cortex®-M33 is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex® processor delivers a high-computational performance with low-power consumption and an advanced response to interrupts.

It features:

- Memory protection units (MPUs) supporting eight regions
- Floating-point arithmetic functionality with support for single-precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex®-M33 processor features:

- System AHB bus:
  The system AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus:
  The code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Refer to Figure 1. STM32C542xx block diagram for more details.

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3.2 Instruction cache (ICACHE)

The instruction cache (ICACHE) is introduced on the C-AHB code bus of the Cortex®-M33 processor to improve performance when fetching instructions and data from internal memories. Some specific features, like hit-under-miss and critical-word-first refill policy, allow close to zero-wait-state performance in most use cases.

The ICACHE main features are:

- Bus interface:
  - One 32-bit AHB slave port, the execution port (input from Cortex®-M33 C-AHB code interface)
  - One 128-bit AHB master port: master1 port (output to Fast bus of the main AHB bus matrix)
  - One 32-bit AHB slave port for control (input from AHB peripherals interconnect, for ICACHE registers access)
- Cache access:
  - Zero wait-state on hits
  - Hit-under-miss capability: ability to serve processor requests (access to cached data) during an ongoing line refill due to a previous cache miss
  - Optimal cache line refill thanks to WRAPw bursts of the size of the cache line (32-bit word size, w, aligned on cache line size)
  - n-way set-associative default configuration with the possibility to configure as 1-way, meaning direct-mapped cache, for applications needing a very-low-power consumption profile
- Replacement and refill:
  - pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with the best complexity/performance balance
  - Critical-word-first refill policy, minimizing processor stalls
  - Possibility to configure burst type of AHB memory transaction for remapped regions: INCRw or WRAPw (size w aligned on cache line size)
- Performance counters:
  The ICACHE implements two performance counters:
  - Hit monitor counter (32-bit)
  - Miss monitor counter (16-bit)
- Error management:
  - Possibility to detect an unexpected cacheable write access, to flag an error, and optionally to raise an interrupt
- Maintenance operation:
  - Cache invalidate: full cache invalidation, fast command, noninterruptible

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory. It also prevents one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to eight protected areas.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. An RTOS (real-time operating system) usually manages the MPU.

If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

3.4 Memories

3.4.1 Embedded flash memory

The devices feature up to 256-Kbyte embedded flash memory that is available for storing programs and data.

The flash memory interface features:

- Dual-bank operating modes
- Read-while-write (RWW)

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This allows a read operation to be performed from one bank while an erase or program operation is performed to the other bank. Each bank contains 16 pages of 8 Kbytes.

The flash memory embeds 4.5-Kbyte OTP (one-time programmable) for user data.

Enhanced flash memory protection mechanisms are available. These mechanisms can be activated by option bytes:

- RDP states for protecting memory content from debug access
- Page group write-protection (WRPG)
- One hide protection area (HDP) per bank that provides temporal isolation for startup code

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.4.1.1 *User data flash memory*

The device features 64 Kbytes of user data flash memory split in two banks of 16 × 2-Kbyte sectors offering perfect space for storing EEPROM emulation data.

3.4.2 Embedded SRAMs

Two SRAMs are embedded in the STM32C542xx devices.

These SRAMs are made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 32 Kbytes
- SRAM2: 32 Kbytes with optional ECC

3.5 Boot modes

At startup, the BOOT0 pin allows the system to boot either from the user Flash or from the bootloader.

When boot from user Flash is selected, BOOTADD defines the boot address. This address can be locked thanks to BOOT_LOCK.

The embedded bootloader is located in the system memory, programmed by STMicroelectronics during production. It is used to reprogram the flash memory by using USART, SPI, FDCAN, or USB in device mode through the device firmware upgrade (DFU).

Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

3.6 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (VCORE)
  - VDD domain
  - RTC domain
  - Analog domain (VDDA)
- System supply voltage regulation
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - PVD monitor
- Power management
  - Low-power modes
- Privileged protection

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3.6.1 Power supply schemes

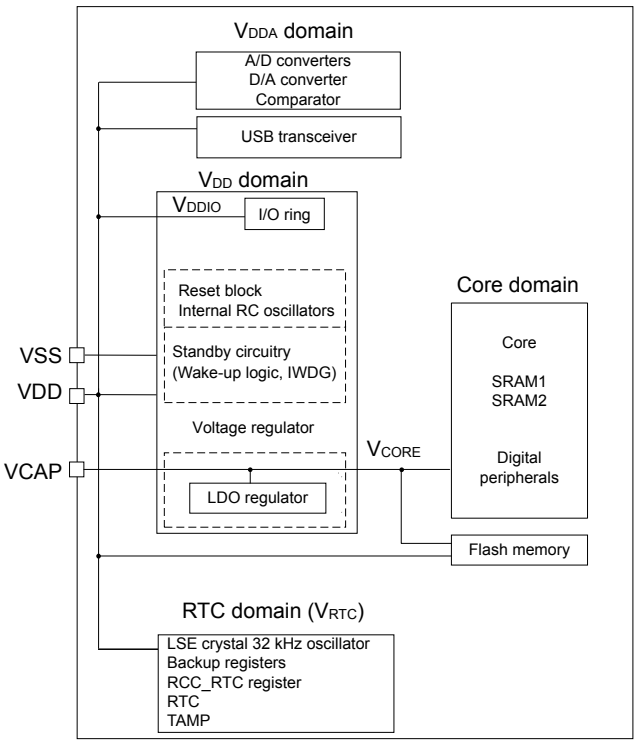
The devices require a 2.7 V to 3.6 V operating voltage supply V_{DD}.

- V_{DD} = 2.7 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator, and the system analog such as reset, power management, and internal clocks. It is provided externally through the VDD pins.
- $V_{DDA} = V_{DD}$
  V_{DDA} is the analog power supply for ADCs, DACs, and comparator.
- V_{REF-}, V_{REF+}
  V_{REF+} is the input reference voltage for ADCs and DAC.
  V_{REF+} can be grounded when ADCs and DAC are not active.
  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.

The STM32C542xx devices embed a LDO regulator to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, and embedded flash memory. The LDO generates this voltage on VCAP pin connected to an external capacitor of 2.2 µF typical.

The LDO regulator can operate in Stop modes where it may provide two different voltages (voltage scaling).

Figure 2. STM32C542xx power supply overview



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3.6.2 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors the V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors the V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.
- Programmable voltage detector (PVD)
  The PVD monitors the V_{DD} power supply by comparing it with a threshold fixed by hardware.
  An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the device into a safe state. The software enables the PVD.

3.6.3 Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode
  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PSI, the HSI, and the HSE crystal oscillators are disabled. The LSE or LSI is still running.
  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).
  The system clock is HSI 144 MHz when exiting stop mode.
  Stop 0 mode maintains the regulator output at a nominal voltage of 1.2 V.
  Stop 1 mode reduces power consumption by lowering V_{CORE} to 0.95 V, which results in a longer wake-up time and fewer wake-up sources compared to Stop 0 mode.
- **Standby** mode
  The Standby mode is used to achieve the lowest power consumption with BOR.
  The PSI, the HSI, and the HSE crystal oscillators are also switched off.
  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).
  The state of each I/O during Standby mode can be retained.
  After entering Standby mode, SRAMs and register contents are lost except for registers in the RTC domain and Standby circuitry.
  The device exits Standby mode in the following cases:
  - An external reset with NRST pin
  - An IWDG reset
  - A WKUP pin event (configurable rising or falling edge)
  - An RTC event occurs (alarm, periodic wake-up, timestamp), or in a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  The system clock after wake-up is HSI 144 MHz.

3.6.4 Reset mode

To improve the consumption under reset, the I/O state under and after reset is “analog state” (the I/O Schmitt trigger is disabled).

3.7 Peripheral interconnect matrix

Several peripherals have direct connections between them. These connections allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run and Sleep modes.

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3.8 Reset and clock controller (RCC)

The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness.

It features:

- **Clock prescaler:** in order to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** in order to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 50 MHz high-speed external crystal or ceramic resonator (HSE). The HSE can also be configured in bypass mode for an external clock.
  - 144 MHz or 48 MHz on high-speed internal RC oscillator (HSI), trimmable by software
  - 144 MHz programmable-speed internal oscillator (PSI)
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
- **Peripheral clock sources:** several peripherals have their own independent clock whatever the system clock. Two dividers, each with a large scale of configurable division factors, can generate independent clocks for the ADCs, USARTx, UARTx, SPIx, I2Cx, I3C1, and FDCAN.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 144 MHz clock (HSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock automatically switches to HSI and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- **Clock-out capability:**
  - MCO (microcontroller clock output): it outputs one of the internal clocks for external use by the application.
  - LSCO (low-speed clock output): it outputs LSI or LSE in all low-power modes.

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 144 MHz.

3.9 Clock recovery system (CRS)

The devices embed a special block that allows automatic trimming of the internal 144 MHz oscillator to guarantee its optimal accuracy over the whole device-operational range. This automatic trimming is based on the external synchronization signal. This signal is either derived from USB_SOF signalization, from an LSE oscillator, from an external signal on the CRS_SYNC pin or generated by user software. For faster lock-in during startup, automatic-trimming and manual-trimming action can be combined.

3.10 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in Analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.11 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, LPDMA1, LPDMA2) and the slave peripherals (flash memory, SRAMs, AHB, and APB). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

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3.12 Low-power direct memory access controller (LPDMA)

The low-power direct memory access (LPDMA) controller is a bus master and system peripheral. The LPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, under the control of an off-loaded CPU.

The LPDMA main features are:

- Single bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral to memory
  - Memory to peripheral
  - Memory to memory
  - Peripheral to peripheral
- Transfers arbitration based on a 4-grade programmed priority at the channel level:
  - One high-priority traffic class for time-sensitive channels (queue 3)
  - Three low-priority traffic classes with a weighted round-robin allocation for non-time-sensitive channels (queues 0, 1, 2)
- Per channel event generation on any of the following events: transfer complete, half transfer complete, data transfer error, user setting error, link transfer error, completed suspension, and trigger overrun
- 8 concurrent LPDMA channels (4-channel LPDMA1, 4-channel LPDMA2):
  - Intrachannel LPDMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intrachannel and interchannel LPDMA transfers chaining via programmable LPDMA input triggers connection to LPDMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based padding or truncation, sign extension, and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Programmable LPDMA request and trigger selection
  - Programmable LPDMA half-transfer and transfer-complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the LPDMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting and event flags
- Privileged/unprivileged support:
  - Support for privileged and unprivileged LPDMA transfers, independently at the channel level
  - Privileged-aware AHB slave port

Table 2. LPDMA1 and LPDMA2 channels implementation and usage

Channel x	Hardware parameters		Features
	dma_fifo_size[x]	dma_addressing[x]	
x = 0 to 4	0	0	Channel x (x = 0 to 4) is implemented with: • no FIFO. Only a single source transfer cell is internally registered. • fixed/contiguously incremented addressing

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Table 3. **LPDMA1 and LPDMA2 autonomous mode and wake-up in low-power modes**

Feature	Low-power modes
Wake-up	LPDMA1/2 in Sleep mode

3.13 Interrupts and events

3.13.1 Nested vectored interrupt controller (NVIC)

- 88 maskable interrupt channels (not including the 16 Cortex®-M33 with FPU interrupt lines)
- 16 programmable priority levels (4 bits of interrupt priority used)
- Low-latency exception and interrupt handling
- Power management control
- Implementation of system control registers

The NVIC and the processor core interface are closely coupled, enabling low-latency interrupt processing and efficient processing of late-arriving interrupts. All interrupts, including the core exceptions, are managed by the NVIC.

3.13.2 Extended interrupt and event controller (EXTI)

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable and direct event inputs. It provides wake-up requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to wake up from Stop modes.

The interrupt request and event request generation can also be used in Run modes.

The EXTI also includes the EXTI mux I/O port selection.

The EXTI main features are the following:

- 37 input events are supported.
- All event inputs allow the possibility to wake up the system.
- Events that do not have an associated wake-up flag in the peripheral have a flag in the EXTI and generate an interrupt to the CPU from the EXTI.
- Events can be used to generate a CPU wake-up event.

The asynchronous event inputs are classified into two groups:

- Configurable events (signals from I/Os or peripherals able to generate a pulse), with the following features:
  - Selectable active trigger edge
  - Interrupt pending status register bits independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt, and event generation
  - Software trigger possibility
  - EXTI I/O port selection
- Direct events (interrupt and wake-up sources from peripherals having an associated flag which requires to be cleared in the peripheral), with the following features:
  - Fixed rising edge active trigger
  - No interrupt pending status register bit in the EXTI (the interrupt pending status flag is provided by the peripheral generating the event)
  - Individual interrupt and event generation mask, used to condition the CPU wake-up and event generation
  - No software trigger possibility

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3.14 Cyclic redundancy check calculation unit (CRC)

The cyclic redundancy check calculation unit (CRC) calculation unit is used to get a CRC code from 8-, 16-, or 32-bit data word and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.15 Analog-to-digital converter (ADC)

The devices embed one analog-to-digital converter (ADC).

Each ADC consists of one 12-bit successive approximation analog-to-digital converter. Each ADC has up to 14 multiplexed channels. A/D conversion of the various channels can be performed in single, continuous, scan, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned (default configuration) 32-bit data register.

The ADCs are mapped on the AHB bus to allow fast data handling. The analog watchdog features allow the application to detect if the input voltage goes outside the user-defined high or low thresholds.

A built-in hardware oversampler improves analog performance while off-loading the related computational burden from the CPU. An efficient low-power mode is implemented to allow very low consumption at low frequency.

The ADC main features are:

- High-performance features:
  - ADC1 connected to 12 external channels and two internal channels
  - 12, 10, 8, or 6-bit configurable resolution
  - ADC conversion time independent from the AHB bus clock frequency
  - Faster conversion time by lowering resolution
  - AHB slave bus interface to allow fast data handling
  - Channel-wise programmable sampling time
  - Flexible sampling time control
  - Fixed latency for a trigger to start of sampling
  - Up to four injected channels (analog inputs assignment to regular or injected channels is fully configurable)
  - Data alignment with in-built data coherency
  - Data can be managed by DMA for regular channel conversions
  - Four dedicated data registers for the injected channels
- Low-power features:
  - Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency
  - Allows slow bus frequency application while keeping optimum ADC performance
  - Provides automatic control to avoid ADC overrun in low AHB bus clock frequency application (autodelayed mode)
- Oversampler:
  - 32-bit data register
  - Oversampling ratio adjustable from 2 to 1024
  - Programmable data right and left shifts
- Data preconditioning:
  - Gain compensation
  - Offset compensation
- Analog input channels:
  - External analog inputs (per ADC): up to 14 GPIO pads
  - One channel for the internal reference voltage (V_{REFINT})
  - One channel for the internal temperature sensor (V_{SENSE})

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- Start-of-conversion can be initiated:
  - By software for both regular and injected conversions
  - By hardware triggers with configurable polarity (internal timer events or GPIO input events) for both regular and injected conversions
- Conversion modes:
  - Each ADC can convert a single channel or can scan a sequence of channels
  - Single mode converts selected inputs once per trigger
  - Continuous mode converts selected inputs continuously
  - Discontinuous mode
- Interrupt generation at ADC ready, the end of sampling, the end of conversion (regular or injected), end of sequence conversion (regular or injected), analog watchdog 1, 2, or 3, or overrun events
- Three analog watchdogs per ADC
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{REF+}$

Table 4. ADC features

ADC modes/features	ADC1
Resolution	12 bits
Maximum sampling-speed	2.25 Msps
Hardware-offset calibration	X
Single-ended inputs	X
Injected channel conversion	X
Oversampling	up to x1024
Data register	32 bits
DMA support	X
Offset compensation	X
Gain compensation	X
Number of analog watchdogs	3

3.15.1 Analog temperature sensor

The STM32C542xx embed an analog temperature sensor that generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by STMicroelectronics. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

3.15.2 Internal voltage reference (V_{REFINT})

The V_{REFINT} provides a stable (bandgap) voltage output for the ADC and the comparator. It is internally connected to ADC input channel.

The precise voltage of V_{REFINT} is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

3.16 Digital to analog converter (DAC)

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode and can be used in conjunction with the DMA controller. In 12-bit mode, the data may be left-aligned or right-aligned.

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An input reference pin, VREF+ (shared with others analog peripherals) is available for better resolution.

The DAC_OUTx pin can be used as general-purpose input/output (GPIO) when the DAC output is disconnected from the output pad and connected to the on chip peripheral. The DAC output buffer can be optionally enabled to allow a high drive output current. An individual calibration can be applied DAC output channel. The DAC output channels support a low-power mode, the sample and hold mode.

The DAC main features are::

- One DAC interface, two output channels
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave and triangular-wave generation
- DMA capability for each channel including DMA underrun error detection
- Double-data DMA capability to reduce the bus activity
- External triggers for conversion
- DAC output-channel buffered/unbuffered modes
- Buffer offset calibration
- DAC output can be disconnected from the DAC_OUTx output pin
- DAC output connection to on chip peripherals
- Sample and hold mode for low-power operation in Stop mode
- Voltage reference input from VREF+ pin

3.17 Ultralow-power comparator (COMP)

The device embeds two ultralow-power comparators (COMP). It can be used for a variety of functions including:

- Wake-up from low-power mode triggered by an analog signal
- Analog signal conditioning
- Cycle-by-cycle current control loop when combined with a PWM output from a timer

The COMP main features are:

- Selectable inverting analog inputs:
  - I/O pins
  - DAC channel output
  - Internal reference voltage and three submultiple values (1/4, 1/2, 3/4) provided by the scaler (buffered voltage divider)
- I/O pins selectable as noninverting analog inputs
- Programmable hysteresis
- Programmable speed/consumption
- Mapping of outputs to I/Os
- Redirection of outputs to timer inputs for triggering:
  - Capture events
  - OCREF_CLR events (for cycle-by-cycle current control)
  - Break events for fast PWM shutdowns
- Blanking of comparator outputs
- Interrupt generation capability with wake-up from Sleep and Stop modes (through the EXTI controller)
- Direct interrupt output to the CPU

3.18 Operational amplifier (OPAMP)

The devices embed one operational amplifier instance, OPAMP1.

OPAMP contains an operational amplifier, an internal resistor divider, and multiplexers to set the OPAMP peripheral into a specific operating mode. In one of these modes, the operational amplifier inputs (INP and INM) and the output (OUT) are connected to external pins, which allows the use of OPAMP as a standalone operational amplifier device. The other OPAMP configurations allow operation as a follower and as a noninverting or inverting operational amplifier with programmable gain (with or without external filtering and/or biasing).

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The programmable gain and the operating mode can be controlled through primary and secondary control register sets that can be activated in a time-multiplexed manner by the timer.

The operational amplifier output can be connected, through a multiplexer, to the OPAMP_VOUT pin or internally to a COMP input channel.

The INP input of OPAMP1 can be connected to an output of the internal DAC.

The operational amplifier operates at normal and high speed (slew rate). Its input offset is compensated through factory trimming, which can be modified by the user if needed.

When OPAMP is not required, it can be disabled to save power.

OPAMP main features are:

- Rail-to-rail input voltage range
- Low input bias current
- Low input offset voltage (factory compensated)
- High frequency bandwidth
- Normal and high speed (slew rate)
- Timer-controlled operation

3.19 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG).

The RNG can be certified NIST SP800-90B. It has also been tested using the German BSI statistical tests of AIS-31 (T0 to T8).

The RNG main features are the following:

- The RNG delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage.
- It can be used as the entropy source to construct a nondeterministic random bit generator (NDRBG).
- It embeds startup and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management.
- It can be disabled to reduce power consumption, or enabled with an automatic low power mode (default configuration).
- It has an AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored).

3.20 AES hardware accelerator (AES)

The AES hardware accelerator (AES) encrypts or decrypts data in compliance with the advanced encryption standard (AES) defined by NIST.

AES supports ECB, CBC, CTR, GCM, GMAC, and CCM chaining modes for key sizes of 128 or 256 bits.

The peripheral supports DMA single transfers for incoming and outgoing data (two DMA channels are required).

The AES main features are:

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- Compliant with NIST FIPS publication 197 “Advanced encryption standard (AES)” (November 2001)
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 128-bit data block processing, supporting cipher key lengths of 128-bit and 256-bit
  - 51 or 75 clock cycle latency in ECB mode for processing one 128-bit block with, respectively, 128-bit or 256-bit key
- Integrated key scheduler to compute the last round key for ECB/CBC decryption
- 256-bit write-only registers for storing cryptographic keys (eight 32-bit registers)
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- 32-bit buffer for data input and output
- Automatic data flow control supporting two direct memory access (DMA) channels, one for incoming data, one for processed data. Only single transfers are supported.
- Data-swapping logic to support 1-, 8-, 16-, or 32-bit data
- AMBA AHB slave peripheral, accessible through 32-bit word single accesses only. Other access types generate an AHB error, and other than 32-bit writes may corrupt the register content.
- Software (in CPU mode only, not in DMA mode) can suspend a message if AES needs to process another message with a higher priority, then resume the original message.

Table 5. AES features

Modes or features[1]	AES
ECB, CBC chaining	X
CTR, CCM, GCM chaining	X
AES 128-bit ECB encryption in cycles	51
DHUK and BHK key selection	-
Resistant to side-channel attacks	-
Shared key between SAES and AES	X
Key sizes in bits	128/256

1. *X = supported.*

3.21 HASH processor (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The hash processor computes FIPS (Federal Information Processing Standards) approved digests of lengths of 160, 224, and 256 bits for messages of any length less than 2 × 64 bits (for SHA-1, SHA-224, and SHA-256).

The HASH main features are:

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- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, Secure Hash Standard (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, Digital Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, HMAC: Keyed-Hashing for Message Authentication and Federal Information Processing Standards Publication FIPS PUB 198-1, The Keyed-Hash Message Authentication Code (HMAC)
- Support for HMAC mode with all supported algorithms
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message.
  - Automatic 32-bit word swapping to comply with the internal little-endian representation of the input bit-string
  - Supported word swapping format: bits, bytes, half-words, and 32-bit words
- Single 32-bit, write-only, input register associated with an internal input FIFO, corresponding to a 64-byte block size (16 × 32 bits)
- Automatic padding to complete the input bit string to fit the digest minimum block size
- AHB slave peripheral, accessible by 32-bit words only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H15) for output message digest
- Automatic data flow control supporting direct memory access (DMA) using one channel
- Support for both single and fixed DMA burst transfers of four words
- Interruptible message digest computation, on a per-block basis
  - Reloadable digest registers
  - Hashing computation suspend/resume mechanism, including DMA

3.22 Timers and watchdogs

The devices include two advanced control timers, up to three general-purpose timers, two basic timers, one low-power timer, two watchdog timers, and one SysTick timer.

The table below compares the features of the advanced control, general-purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture / compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16 bits	Up, down, Up/ down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TIM2	32 bits	Up, down, Up/ down	Any integer between 1 and 65536	Yes	4	No
	TIM12,	16 bits	Up			2	
	TIM15	16 bits	Up, down, Up/ down			2	
Basic	TIM6, TIM7	16 bits	Up	Any integer between 1 and 65536	Yes	0	No

3.22.1 Advanced-control timers (TIM1/TIM8)

The advanced-control timers (TIM1/TIM8) consist of a 16-bit autoreload counter driven by a programmable prescaler.

They may be used for various purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

TIM1/TIM8 timer features include:

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- 16-bit up, down, up/down autoreload counter
- 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency by any factor from 1 to 65536
- Seven independent channels for:
  - Input capture (except channels 5, 6, and 7)
  - Output compare
  - PWM generation (edge- and center-aligned mode)
  - One-pulse mode output
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Two break inputs to put the timer’s output signals in a safe user-selectable configuration
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization, or count by internal/external trigger)
  - Input capture
  - Output compare
- Incremental encoders, quadrature encoders, and hall-sensors support
- Trigger input for external clock or cycle-by-cycle current management
- ADC synchronization for jitter-free sampling points

3.22.2 General-purpose timers (TIM2/TIM12/TIM15)

The general-purpose timers (TIMx) consist of a 16-bit or 32-bit autoreload counter driven by a programmable prescaler.

They can be used for various purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare and PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

General-purpose TIMx timer features include:

- 16-bit or 32-bit up, down, up/down autoreload counter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- Up to four independent channels for:
  - Input capture
  - Output compare
  - PWM generation (edge- and center-aligned modes)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization, or count by internal/external trigger)
  - Input capture
  - Output compare
- Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- ADC synchronization for jitter-free sampling points

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3.22.3 Basic timers (TIM6/TIM7)

The basic timers (TIM6/TIM7) consist of a 16-bit autoreload counter driven by a programmable prescaler.

They can be used as generic timers for time-base generation.

The basic timer can also be used for triggering the digital-to-analog converter. This is done with the trigger output of the timer.

The timers are completely independent and do not share any resources.

Basic timer (TIM6/TIM7) features include:

- 16-bit autoreload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- Synchronization circuit to trigger the DAC
- Interrupt/DMA generation on the update event: counter overflow
- ADC synchronization for jitter-free sampling points

3.22.4 Low-power timers (LPTIM1)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to its diversity of clock sources, the LPTIM can keep running in all power modes except for Standby mode. Given its capability to run even with no internal clock source, the LPTIM can be used as a pulse counter, which can be useful in some applications. The LPTIM capability to wake up the system from low-power modes makes it suitable to realize timeout functions with extremely low-power consumption.

The low-power timer supports the following features:

- 16-bit up counter with 16-bit auto reload register
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI, or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
- 16-bit ARR auto reload register
- 16-bit capture/compare register
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.22.5 Independent watchdog (IWDG)

The independent watchdog (IWDG) peripheral offers a high safety level due to its capability to detect malfunctions caused by software or hardware failures.

The IWDG is clocked by an independent clock and remains active even if the main clock fails.

Additionally, the watchdog function is performed in the VDD voltage domain, allowing the IWDG to remain functional even in low-power modes.

The IWDG main features are:

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- 12-bit down-counter
- Dual voltage domain, thus enabling operation in low-power modes
- Independent clock
- Early wake-up interrupt generation
- Reset generation:
  - In case of timeout
  - In case of refresh outside the expected window

3.22.6 Window watchdog (WWDG)

The system window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interference or unforeseen logical conditions, which causes the application program to abandon its normal sequence.

The watchdog circuit generates a reset on the expiry of a programmed time period unless the program refreshes the contents of the down-counter before the T6 bit is cleared. A reset is also generated if the 7-bit down-counter value (in the control register) is refreshed before the down-counter reaches the window register value. This implies that the counter must be refreshed in a limited window.

The WWDG clock is prescaled from the APB clock and has a configurable time window that can be programmed to detect abnormally late or early application behavior.

The WWDG is best suited for applications requiring the watchdog to react within an accurate timing window.

The WWDG main features are:

- Programmable free-running down-counter
- Conditional reset:
  - Reset (if watchdog activated) when the down-counter value becomes lower than 0x40
  - Reset (if watchdog activated) if the down-counter is reloaded outside the window
- Early wake-up interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40

3.22.7 SysTick timer

The Cortex®-M33 embeds one SysTick timer.

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

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3.23 Real-time clock (RTC), tamper and backup registers

3.23.1 Real-time clock (RTC)

The real-time clock (RTC) supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a controller clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event.
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- Privilege protection support:
  - Alarm A, alarm B, wake-up timer, and timestamp individual privileged protection

The RTC is functional in all low-power modes when it is clocked by the LSE.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.23.2 Tamper and backup registers (TAMP)

The antitamper detection circuit is used to protect sensitive data from external attacks. Thirty-two 32-bit backup registers are retained in all low-power modes. The backup registers, as well as other secrets in the device, are protected by this antitamper detection circuit with three tamper pins and six internal tampers. The external tamper pins can be configured for edge detection or level detection with or without filtering.

The TAMP main features are:

- A tamper detection can optionally erase the backup registers, SRAM2, ICACHE, and cryptographic peripherals. The device resources protected by tamper are named “device secrets”.
- 32 × 32-bit backup registers
- Up to three tamper pins for three external tamper detection events:
  - Passive tampers: Ultralow-power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- Six internal tamper events to protect against transient attacks
- Each tamper can be configured in two modes:
  - Confirmed mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Potential mode: most of the secrets erase following a tamper detection are launched by software
- Any tamper detection can generate an RTC timestamp event
- Tamper configuration and backup registers privilege protection

3.24 Inter-integrated circuit interface (I2C)

The device embeds one I2C interface. Refer to Table 7 for feature implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration, and timing.

It supports Standard-mode (Sm), Fast-mode (Fm), and Fast-mode Plus (Fm+).

The I2C peripheral is also system management bus (SMBus) and power management bus (PMBus®) compatible.

It can use DMA to reduce the CPU load.

The I²C peripheral supports:

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- I²C-bus specification rev03 compatibility:
  - Controller and target modes
  - Multicontroller capability
  - Standard-mode (up to 100 kHz)
  - Fast-mode (up to 400 kHz)
  - Fast-mode Plus (up to 1 MHz)
  - 7-bit and 10-bit addressing mode
  - Multiple 7-bit target addresses (2 addresses, 1 with configurable mask)
  - All 7-bit addresses acknowledge mode
  - General call
  - Programmable setup and hold times
  - Easy-to-use event management
  - Clock stretching (optional)
- 1-byte buffer with DMA capability
- Programmable analog and digital noise filters
- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and device support – SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock
- Wake-up from Stop mode on address match

Table 7. I2C implementation

Features[1]	I2C1
Standard-mode (up to 100 Kbit/s)	X
Fast mode (up to 400 Kbit/s)	X
Fast mode plus (Fm+) with 20 mA output drive I/Os (up to 1 Mbit/s)	X
Programmable analog and digital noise filters	X
SMBus/PMBus hardware support	X
Independent clock	X
Wake-up capability	X

1. *X = supported.*

3.25 Improved inter-integrated circuit interface (I3C)

The I3C interface handles communication between this device and others, such as sensors and the host processor, connected on an I3C bus.

An I3C bus is a two-wire, serial single-ended, multidrop bus, intended to improve a legacy I^2C bus.

The I3C SDR-only peripheral implements all the features required by the MIPI® I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as a controller (formerly known as master) or as a target (formerly known as slave). When acting as a controller, the I3C peripheral improves the features of the I2C interface while preserving some backward compatibility: it allows an I^2C target to operate on an I3C bus in legacy I^2C fast mode (Fm) or legacy I^2C fast mode plus (Fm+), provided that the latter does not perform clock stretching. The I3C peripheral can be used with DMA to offload the CPU.

The I3C peripheral supports:

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- MIPI® I3C specification v1.1, as:
  - I3C SDR-only primary controller
  - I3C SDR-only secondary controller
  - I3C SDR-only target
- I3C SCL bus clock frequency up to 12.5 MHz
- Registers configuration from the host application via the APB target port
- Queued data transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on the I3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Queued control/status transfers, when controller:
  - Control FIFO (C-FIFO) for control words to be sent on the I3C bus
  - Optional status FIFO (S-FIFO) for status words as received on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Messages:
  - Legacy I²C read/write messages to legacy I^2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header generation on the I3C bus
  - HDR exit pattern generation on the I3C bus for error recovery
- Programmable bus timing, when controller:
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time
  - Bus available/idle condition time
  - Clock stall time
- Target-initiated requests management:
  - Simultaneous support up to four targets, when controller
  - In-band interrupts, with programmable IBI payload (up to four bytes), with pending read notification support
  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
- HDR exit pattern detection, when target
- Bus error management:
  - CEx with x = 0, 1, 2, 3 when controller
  - TEx with x = 0, 1, ... , 6 when target
  - Bus control switch error and recovery
  - Target reset
- Individual programmable event-based management:
  - Per-event identification with flag reporting and clear control
  - Host application notification via flag polling, and/or via interrupt with a per-event programmable enable
  - Error type identification

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- Wake-up from Stop mode(s), as controller:
  - On an in-band interrupt without payload
  - On a hot-join request
  - On a controller-role request
- Wake-up from Stop mode(s), as target:
  - On a reset pattern
  - On a missed start
- Multiclock domain management:
  - Separate APB clock and kernel clock, driven from independently programmed clock sources via the RCC, in addition to SCL clock
  - Minimum operating frequency for the kernel clock and the APB clock vs. the application-driven SCL clock

Table 8. I3C peripheral controller/target features versus MIPI® v1.1

Features(1)	MIPI® I3C v1.1	I3C peripheral when controller	I3C peripheral when target	Comments
I3CSDR message	X	X	X	-
Legacy I^2C message (Fm/Fm+)	X	X	-	Mandatory when controller and the I3C bus is mixed with (external) legacy I^2C target(s). Optional in MIPI v1.1 when target.
HDR DDR message	X	-	-	Optional in MIPI v1.1
HDR-TSL/TSP, HDR-BT	X	-	-	
Dynamic address assignment	X	X	X	-
Static address	X	X	-	No (intended) support of I3C peripheral as a target on an I^2C bus.
Grouped addressing	X	X	-	Optional in MIPI v1.1
CCCs	X	X	X	Mandatory CCCs and some optional CCCs are supported.
Error detection and recovery	X	X	X	-
In-band interrupt (with MDB)	X	X	X	-
Secondary controller	X	X	X	-
Hot-join mechanism	X	X	X	-
Target reset	X	X	X	-
Synchronous timing control	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 0	X	X	-	
Asynchronous timing control 1, 2, 3	X	-	-	
Device-to-device tunneling	X	X	-	
Multilane data transfer	X	X	-	
Monitoring device early termination	X	-	-	

1. *X = supported.*

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3.26 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have two embedded universal synchronous receiver transmitters (USART1/2), two universal asynchronous receiver transmitters (UART4/5), and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 9. USART, UART, and LPUART features

Features[1]	USART1/2	UART4/5	LPUART1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode (controller/target)	X	-	-
Smartcard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain and wake-up from Stop mode	X[2]	X[2]	X[2]
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Autobaud rate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8, and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size	8 bytes		

1. *X = supported.*
2. *Wake-up supported from Stop mode.*

3.26.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications are possible by using the DMA (direct memory access) for multibuffer configuration.

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The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
- Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (one or two stop bits)
- Synchronous controller/target mode and clock output/input for synchronous communications
- SPI controller transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop capability
- LIN controller synchronous break send capability and LIN target break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.26.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART is a UART, which enables bidirectional UART communications with a limited power consumption. Only a 32.768 kHz LSE clock is required to enable UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock.

Even when the microcontroller is in low-power mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.

It supports half-duplex single-wire communications and modem operations (CTS/RTS).

It also supports multiprocessor communications. The direct memory access (DMA) can be used for data transmission/reception.

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The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 bauds to 9600 bauds using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data
  Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (one or two stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop mode

3.27 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

The devices embed two serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex, and simplex synchronous, serial communication with external devices.

Table 10. SPI features

SPI feature	SPI2S1, SPI2S2 (full feature set instances)
Data size	Configurable from 4 to 32-bit
CRC computation	CRC polynomial length configurable from 5 to 32-bit
Size of FIFOs	16 × 8-bit
Number of transferred data	Unlimited, expandable
I2S feature	Yes

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The serial peripheral interface (SPI) can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex, and simplex synchronous, serial communication with external devices. The interface can be configured as master or slave and can operate in multimaster or multislave configurations. The device configured as master provides a communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to set up communication with a specific slave and to ensure it handles the data flow properly. The Motorola® data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- From 4-bit up to 32-bit data size selection
- Multimaster or multislave mode capability
- Dual clock domain, the peripheral kernel clock is independent from the APB bus clock
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO × MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI format support
- Hardware CRC can verify the integrity of the communication at the end of a transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun, mode fault, and frame error, depending on the operating mode
- Two 8-bit width embedded Rx and Tx FIFOs (FIFO size depends on instance)
- Configurable FIFO thresholds (data packing)
- Capability to handle data streams by system DMA controller
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Optional status pin RDY signaling that the slave device is ready to handle the data flow

The I2S main features are:

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- Full duplex communication
- Simplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler
- Data length can be 16, 24, or 32 bits
- Channel length can be 16 or 32 in master, any value in slave
- Programmable clock polarity
- Error flags signaling for improved reliability: Underrun, overrun, and frame errors
- Embedded Rx and Tx FIFOs
- Supported I2S protocols:
  - I2S Philips standard
  - MSB-justified standard (left-justified)
  - LSB-justified standard (right-justified)
  - PCM standard (with short and long frame synchronization)
- Data ordering programmable (LSB or MSB first)
- DMA capability for transmission and reception
- Master clock can be output to drive an external audio component:
  - FMCK = 256 × FWS for all I2S modes
  - FMCK = 128 × FWS for all PCM modes

3.28 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory, and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs, and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- Two receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO/queue of three payloads (up to 64 bytes per payload)
- Configurable transmit event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.29 Universal serial bus full-speed host/device interface (USB)

The USB peripheral implements an interface between a full-speed USB 2.0 bus and the APB2 bus. USB suspend and resume are supported, which permits stopping the device clocks for low-power consumption.

The USB main features are:

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- USB specification version 2.0 full-speed compliant
- Supports both host and device modes
- Configurable number of endpoints from 1 to 8
- Dedicated packet buffer memory (SRAM) of 2048 bytes
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding, and bit-stuffing
- Isochronous transfers support
- Double-buffered bulk/isochronous endpoint/channel support
- USB suspend and resume operations
- Frame-locked clock pulse generation
- USB 2.0 link power management support (device mode only)
- Battery charging specification revision 1.2 support (device mode only)
- USB connect/disconnect capability (controllable embedded pull-up resistor on USB_DP line)

3.30 Development support

3.30.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be reused as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.30.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell™ (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The ETM operates with third party debugger software tools.

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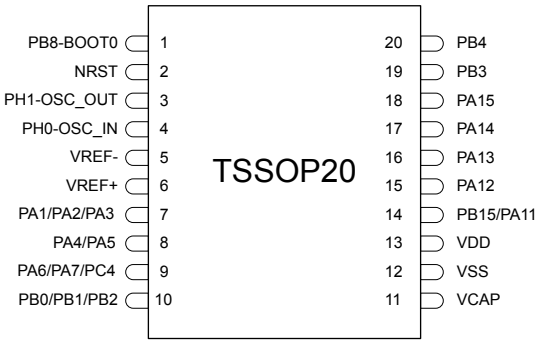
4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 3. TSSOP20 pinout

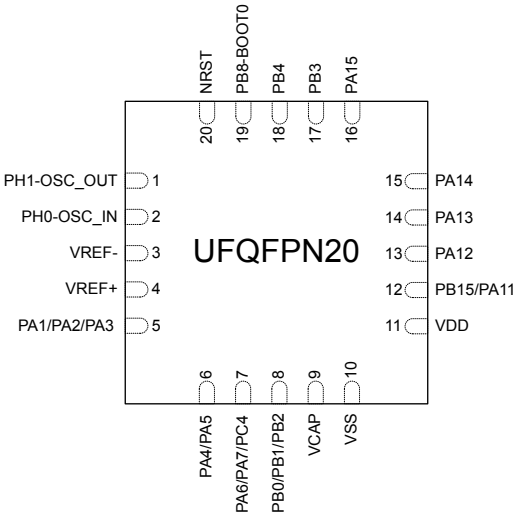
Package top view



DT76162V1

Figure 4. UFQFPN20 pinout

Package top view



DT76163V1

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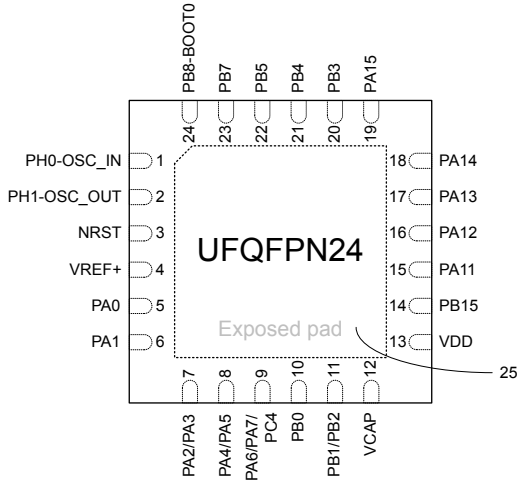
Figure 5. UFQFPN24 pinout

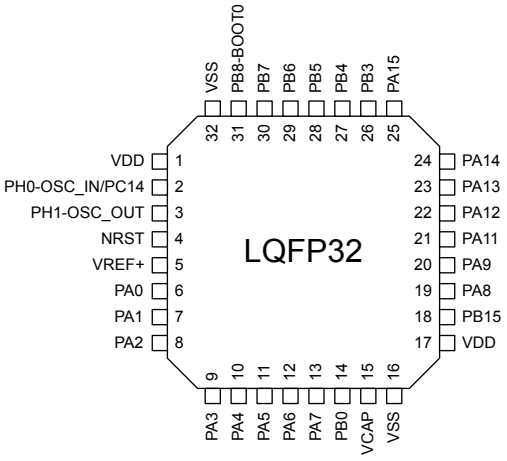
Package top view



DT76164V1

Figure 6. LQFP32 pinout

Package top view



DT74257V2

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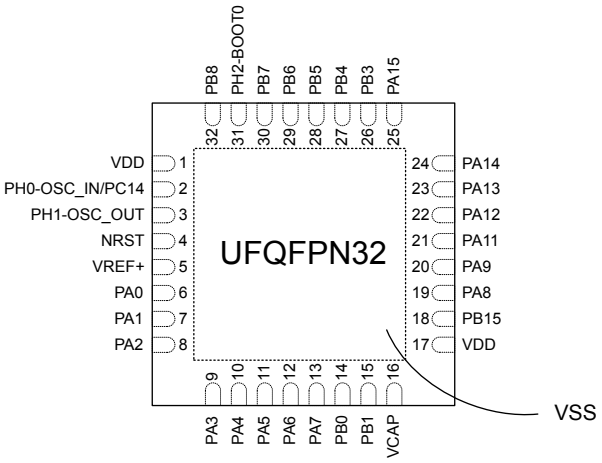
Figure 7. UFQFPN32 pinout

Package top view

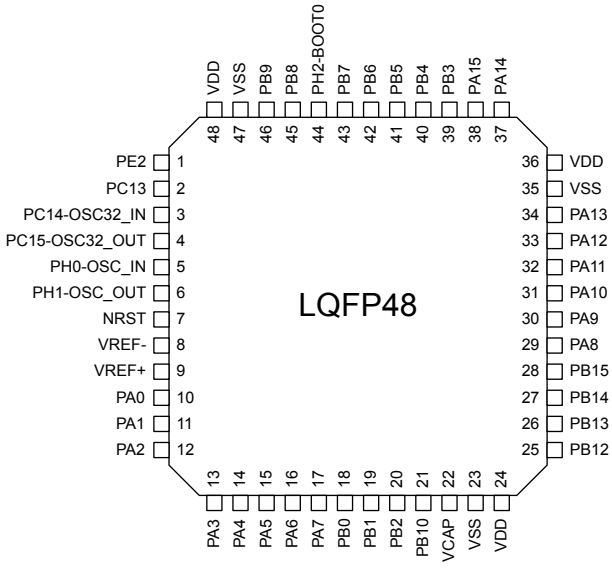


DT74256V2

Note: There is an exposed die pad on the underside of the UFQFPN package. This backside pad must be connected and soldered to PCB ground.

Figure 8. LQFP48 pinout

Package top view



DT74258V1

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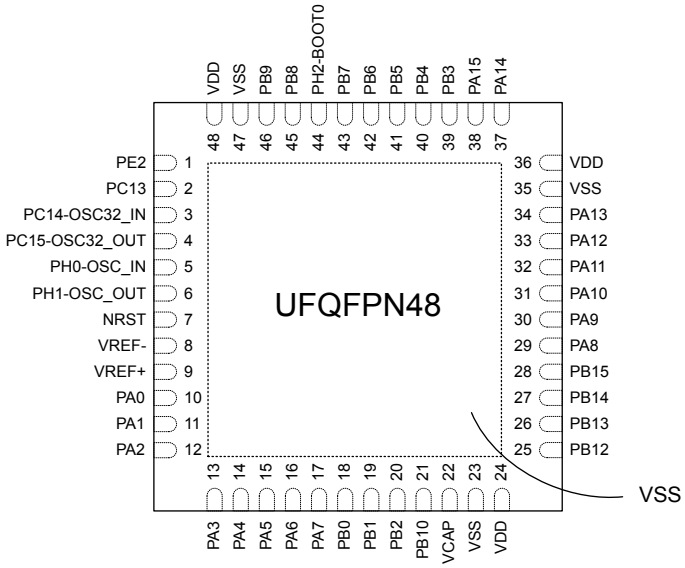
Figure 9. UFQFPN48 pinout

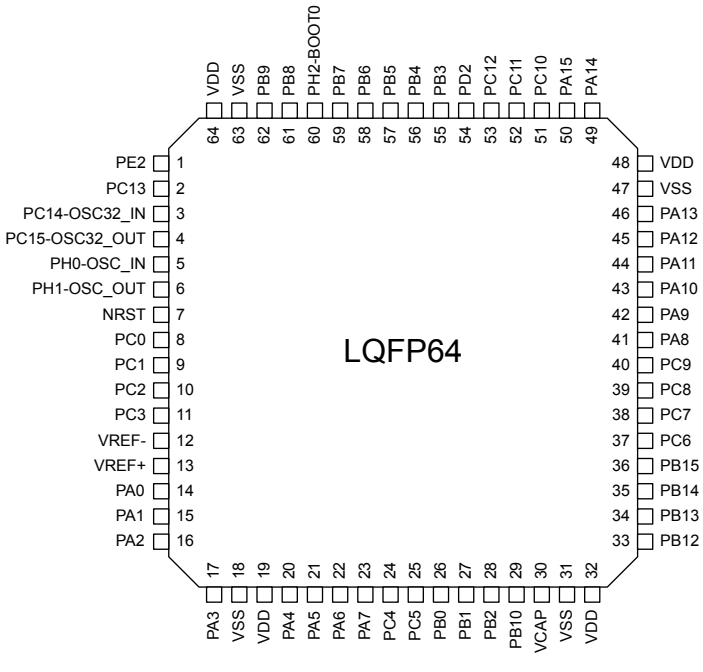
Package top view



Note: There is an exposed die pad on the underside of the UFQFPN package. This backside pad must be connected and soldered to PCB ground.

Figure 10. LQFP64 pinout

Package top view



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4.2 Pin description

Table 11. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name.	
Pin type		I	Input-only pin
		I/O	Input/output pin
		S	Supply pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT and FT I/Os[(1)]	
		_a	I/O with analog switch function supplied by V_{DDA}
		_t	Tamper I/O
		_f	I/O fm+ capable
		_u	I/O with USB function
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. *The related I/O structures in the table below are a concatenation of various options. Examples: FT, TT_a.*

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Table 12. STM32C542xx pin/ball definition

Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
-	-	-	-	-	1	1	1	PE2	I/O	FT	-	TRACECLK, LPTIM1_IN2, EVENTOUT	-
-	-	-	-	-	2	2	2	PC13	I/O	FT_t	(1)(2)	FDCAN1_TX, EVENTOUT	TAMP_IN1, RTC_OUT1/ RTC_TS, WKUP4
-	-	-	2	2	3	3	3	PC14-OSC32_IN (OSC32_IN)	I/O	FT	(1)	TIM12_CH1, FDCAN1_RX, EVENTOUT	OSC32_IN
-	-	-	-	-	4	4	4	PC15-OSC32_OUT (OSC32_OUT)	I/O	FT	(1)	TIM12_CH2, EVENTOUT	OSC32_OUT
4	2	1	2	2	5	5	5	PH0-OSC_IN (PH0)	I/O	FT_f	-	I2C1_SDA, EVENTOUT	OSC_IN
3	1	2	3	3	6	6	6	PH1-OSC_OUT (PH1)	I/O	FT_f	-	I2C1_SCL, EVENTOUT	OSC_OUT
2	20	3	4	4	7	7	7	NRST	I/O	RST	-	-	-
-	-	-	-	-	-	-	8	PC0	I/O	FT_a	-	SPI2_RDY, EVENTOUT	ADC1_IN8, COMP2_INP
-	-	-	-	-	-	-	9	PC1	I/O	FT_a	-	TRACED0, SPI2_MOSI/ I2S2_SDO, EVENTOUT	ADC1_IN9, COMP2_INM, TAMP_IN2
-	-	-	-	-	-	-	10	PC2	I/O	FT_a	-	PWR_CSLEEP, SPI2_MISO/ I2S2_SDI, EVENTOUT	ADC1_IN10
-	-	-	-	-	-	-	11	PC3	I/O	FT_a	-	PWR_CSTOP, LPUART1_TX, SPI2_MOSI/I2S2_SDO, EVENTOUT	ADC1_IN11
5	3	-	-	-	8	8	12	VREF-	S	-	-	-	-
6	4	4	5	5	9	9	13	VREF+	S	-	-	-	-
-	-	5	6	6	10	10	14	PA0	I/O	FT_a	-	TIM2_CH1, TIM8_ETR, TIM15_BKIN, SPI2_RDY, SPI1_RDY, USART2_CTS/ USART2_NSS, UART4_TX, SPI2_NSS/I2S2_WS, TIM2_ETR, EVENTOUT	ADC1_IN0, COMP1_INP, TAMP_IN2, WKUP1

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Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
7	5	6	7	7	11	11	15	PA1	I/O	TT_a	-	TIM2_CH2, TIM8_BKIN, TIM15_CH1N, LPTIM1_IN1, USART2_RTS, UART4_RX, EVENTOUT	ADC1_IN1, OPAMP1_VINP0, TAMP_IN3
7	5	7	8	8	12	12	16	PA2	I/O	TT_a	-	TIM2_CH3, LPUART1_RX, TIM15_CH1, LPTIM1_IN2, USART2_TX, COMP2_OUT, EVENTOUT	ADC1_IN2, COMP2_INM, OPAMP1_VINM0, TAMP_IN3, WKUP2
7	5	7	9	9	13	13	17	PA3	I/O	FT_a	-	TIM2_CH4, LPUART1_TX, TIM15_CH2, SPI2_NSS/ I2S2_WS, SPI2_MOSI/ I2S2_SDO, USART2_RX, COMP1_OUT, EVENTOUT	ADC1_IN3, COMP2_INP
-	-	-	-	-	-	-	18	VSS	S	-	-	-	-
-	-	-	-	-	-	-	19	VDD	S	-	-	-	-
8	6	8	10	10	14	14	20	PA4	I/O	TT_a	-	TIM1_BKIN2, SPI1_MOSI/ I2S1_SDO, SPI1_NSS/ I2S1_WS, SPI2_NSS/I2S2_WS, USART2_CK, EVENTOUT	ADC1_IN4, DAC1_OUT1
8	6	8	11	11	15	15	21	PA5	I/O	TT_a	-	TIM2_CH1, TIM1_CH3, TIM8_CH1N, SPI1_SCK/ I2S1_CK, SPI2_SCK/I2S2_CK, USART1_CTS/USART1_NSS, TIM2_ETR, EVENTOUT	ADC1_IN5, DAC2_OUT1, COMP1_INM
9	7	9	12	12	16	16	22	PA6	I/O	TT_a	-	TIM1_BKIN, TIM8_BKIN, SPI1_MISO/I2S1_SDI, USART1_TX, LPUART1_RTS, EVENTOUT	ADC1_IN6, OPAMP1_VOUT
9	7	9	13	13	17	17	23	PA7	I/O	FT_a	-	TIM1_CH1N, TIM8_CH1N, TIM15_CH1, SPI1_MOSI/ I2S1_SDO, SPI2_MISO/ I2S2_SDI, USART1_RX, LPUART1_CTS, COMP2_OUT, EVENTOUT	ADC1_IN7
9	7	9	-	-	-	-	24	PC4	I/O	FT_a	-	TIM2_CH4, TIM8_BKIN, I2S1_MCK, USART2_RX, EVENTOUT	ADC1_IN2, COMP1_INM
-	-	-	-	-	-	-	25	PC5	I/O	FT_a	-	TIM1_CH4N, TIM8_BKIN2, COMP1_OUT, EVENTOUT	ADC1_IN5, COMP2_INM

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Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
10	8	10	14	14	18	18	26	PB0	I/O	TT_a	-	TIM1_CH2N, TIM8_CH2N, SPI1_MISO/I2S1_SDI, USART2_TX, UART4_CTS, EVENTOUT	ADC1_IN6, COMP1_INP, OPAMP1_VINP1
10	8	11	15	-	19	19	27	PB1	I/O	TT_a	-	TIM1_CH3N, TIM8_CH3N, SPI2_NSS/I2S2_WS, USART2_RX, COMP1_OUT, EVENTOUT	ADC1_IN7, COMP1_INM, OPAMP1_VINM1
10	8	11	-	-	20	20	28	PB2	I/O	FT_a	-	RTC_OUT2, TIM8_CH4N, SPI1_RDY, LPTIM1_CH1, SPI2_SCK/I2S2_CK, SPI2_MOSI/I2S2_SDO, EVENTOUT	COMP1_INP, LSCO
-	-	-	-	-	21	21	29	PB10	I/O	FT_f	-	TIM2_CH3, TIM8_CH1, LPTIM1_IN1, I2C1_SCL, SPI2_SCK/I2S2_CK, USART2_TX, EVENTOUT	-
11	9	12	16	15	22	22	30	VCAP	S	-	-	-	-
12	10	-	-	16	23	23	31	VSS	S	-	-	-	-
13	11	13	17	17	24	24	32	VDD	S	-	-	-	-
-	-	-	-	-	25	25	33	PB12	I/O	FT_f	-	TIM1_BKIN, TIM8_CH3, I2C1_SDA, SPI2_NSS/ I2S2_WS, USART2_CK, FDCAN2_RX, UART5_RX, EVENTOUT	-
-	-	-	-	-	26	26	34	PB13	I/O	FT	-	TIM1_CH1N, TIM8_CH2, LPTIM1_CH1, I2C1_SMBA, SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, LPUART1_RX, FDCAN2_TX, UART5_TX, EVENTOUT	-
-	-	-	-	-	27	27	35	PB14	I/O	FT	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, USART2_RTS, UART4_RTS, EVENTOUT	-

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Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
14	12	14	18	18	28	28	36	PB15	I/O	TT	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/ I2S2_SDO, SPI1_MOSI/ I2S1_SDO, UART4_CTS, UART5_RX, EVENTOUT	COMP2_INP, OPAMP1_VINP2
-	-	-	-	-	-	-	37	PC6	I/O	FT	-	TIM12_CH1, TIM8_CH1, I2S2_MCK, EVENTOUT	-
-	-	-	-	-	-	-	38	PC7	I/O	FT	-	TIM8_CH2, I2S1_MCK, EVENTOUT	-
-	-	-	-	-	-	-	39	PC8	I/O	FT	-	TRACED1, TIM8_CH3, UART5_RTS, EVENTOUT	-
-	-	-	-	-	-	-	40	PC9	I/O	FT_f	-	MCO2, TIM12_CH2, TIM8_CH4, AUDIOCLK, UART5_CTS, I2C1_SDA, EVENTOUT	-
-	-	-	19	19	29	29	41	PA8	I/O	FT_f	-	MCO1, TIM1_CH1, I3C1_SDA, TIM8_BKIN2, TIM15_CH2, SPI1_RDY, SPI2_MOSI/ I2S2_SDO, USART1_CK, I2C1_SCL, USB_SOF, TIM2_CH4, EVENTOUT	-
-	-	-	20	20	30	30	42	PA9	I/O	FT	-	MCO2, TIM1_CH2, I3C1_SCL, LPUART1_TX, TIM15_CH1N, SPI2_SCK/I2S2_CK, USART1_TX, I2C1_SMBA, TIM8_CH2N, EVENTOUT	-
-	-	-	-	-	31	31	43	PA10	I/O	FT	-	TIM1_CH3, LPUART1_RX, USART1_RX, FDCAN2_TX, EVENTOUT	-
14	12	15	21	21	32	32	44	PA11	I/O	FT_fu	-	TIM1_CH4, LPUART1_CTS, USART2_TX, SPI2_NSS/ I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, I2C1_SCL, FDCAN1_RX, EVENTOUT	USB_DM

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Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
15	13	16	22	22	33	33	45	PA12	I/O	FT_fu	-	TIM1_ETR, LPUART1_RTS, USART2_RX, SPI2_SCK/ I2S2_CK, UART4_TX, USART1_RTS, I2C1_SDA, FDCAN1_TX, COMP2_OUT, EVENTOUT	USB_DP
16	14	17	23	23	34	34	46	PA13 (JTMS/ SWDIO)	I/O	FT	(3)	JTMS/SWDIO, COMP1_OUT, EVENTOUT	-
-	-	-	-	-	35	35	47	VSS	S	-	-	-	-
-	-	-	-	-	36	36	48	VDD	S	-	-	-	-
17	15	18	24	24	37	37	49	PA14 (JTCK/ SWCLK)	I/O	FT	(3)	JTCK/SWCLK, EVENTOUT	-
18	16	19	25	25	38	38	50	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM1_CH2N, LPTIM1_ETR, I2C1_SMBA, SPI1_NSS/I2S1_WS, SPI2_NSS/I2S2_WS, USART2_CK, UART4_RTS, USART1_TX, TIM8_CH4N, TIM2_ETR, EVENTOUT	-
-	-	-	-	-	-	-	51	PC10	I/O	FT	-	TIM8_CH1N, I3C1_SCL, SPI2_SCK/I2S2_CK, USART2_TX, UART4_TX, EVENTOUT	-
-	-	-	-	-	-	-	52	PC11	I/O	FT	-	TIM8_CH2N, I3C1_SDA, SPI2_MISO/I2S2_SDI, USART2_RX, UART4_RX, EVENTOUT	-
-	-	-	-	-	-	-	53	PC12	I/O	FT	-	TRACED3, TIM15_CH1, TIM8_CH3N, SPI2_MOSI/ I2S2_SDO, USART2_CK, UART5_TX, EVENTOUT	-
-	-	-	-	-	-	-	54	PD2	I/O	FT	-	TRACED2, TIM15_BKIN, UART5_RX, EVENTOUT	-

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Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
19	17	20	26	26	39	39	55	PB3 (JTDO/ TRACESWO)	I/O	FT_f	-	JTDO/TRACESWO, TIM2_CH2, I3C1_SDA, I2C1_SDA, SPI1_SCK/I2S1_CK, FDCAN2_RX, USART1_CK, LPUART1_TX, I2C1_SCL, CRS_SYNC, USART1_TX, TIM8_CH1, UART5_RTS, EVENTOUT	-
20	18	21	27	27	40	40	56	PB4 (NJTRST)	I/O	FT_f	-	NJTRST, TIM15_CH1, I3C1_SCL, LPTIM1_CH2, SPI1_MISO/I2S1_SDI, FDCAN2_TX, SPI2_NSS/ I2S2_WS, LPUART1_CTS, I2C1_SDA, USART1_RX, TIM8_CH2, UART5_CTS, EVENTOUT	-
-	-	22	28	28	41	41	57	PB5	I/O	FT	-	I3C1_SDA, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, LPUART1_RTS, FDCAN2_RX, USART1_CK, TIM8_CH3, UART5_RX, EVENTOUT	-
-	-	-	29	29	42	42	58	PB6	I/O	FT_f	-	I3C1_SCL, I2C1_SCL, SPI1_MISO/I2S1_SDI, USART1_TX, LPUART1_TX, FDCAN2_TX, USART1_CTS/ USART1_NSS, TIM8_CH4, UART5_TX, EVENTOUT	-
-	-	23	30	30	43	43	59	PB7	I/O	FT_f	-	I3C1_SDA, I2C1_SDA, SPI1_SCK/I2S1_CK, USART1_RX, LPUART1_RX, FDCAN1_TX, USART1_RTS, EVENTOUT	WKUP5
-	-	-	31	-	44	44	60	PH2-BOOT0	I/O	FT	-	MCO1, LPTIM1_IN2, FDCAN1_RX, EVENTOUT	-
1	19	24	-	31	-	-	-	PB8-BOOT0	I/O	FT_f	-	TIM1_CH1, I3C1_SCL, I2C1_SCL, SPI1_NSS/ I2S1_WS, UART4_RX, FDCAN1_RX, EVENTOUT	-

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Pin number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TSSOP20	UFQFPN20	UFQFPN24	UFQFPN32	LQFP32	LQFP48	UFQFPN48	LQFP64						
-	-	-	32	-	45	45	61	PB8	I/O	FT_f	-	TIM1_CH1, I3C1_SCL, I2C1_SCL, SPI1_NSS/ I2S1_WS, UART4_RX, FDCAN1_RX, EVENTOUT	-
-	-	-	-	-	46	46	62	PB9	I/O	FT_f	-	I3C1_SDA, I2C1_SDA, SPI2_NSS/I2S2_WS, SPI1_SCK/I2S1_CK, UART4_TX, FDCAN1_TX, EVENTOUT	-
-	-	-	-	32	47	47	63	VSS	S	-	-	-	-
-	-	-	1	1	48	48	64	VDD	S	-	-	-	-

1. *After a RTC domain reset, PC13, PC14, and PC15 operate as GPIOs. Their function depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the backup domain and RTC register descriptions in the product reference manual.*
2. *Toggling the PC13 port can disturb the low-speed crystal connected to the LSE on PC14 and PC15. Refer to product errata sheet for more details.*
3. *After reset, this pin is configured for JTAG or SWD alternate function. The internal pull-up on the PA15, PA13, and PB4 pins, and the internal pull-down on the PA14 pin, are activated.*

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4.3 Alternate functions

Table 13. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2	I3C1/ TIM1/8/12/15	I3C1/LPTIM1/ LPUART1/ TIM8	I2C1/2/I3C1/ LPTIM1/SPI1/ I2S1/TIM15/ USART1/2	I3C1/LPTIM1/ SPI1/I2S1/ SPI2/ I2S2/SYS	FDCAN2/ SPI1/ I2S1/SPI2/ I2S2/UART4	SPI2/I2S2/ USART1/2	I2C1/ LPUART1/ UART4/5	FDCAN1/2/ I2C1/ SPI2/I2S2	CRS	USART1	-	TIM8/USB_	COMP1/2/ TIM2/UART5	SYS
Port A	PA0	-	TIM2_CH1	-	TIM8_ETR	TIM15_BKIN	SPI2_RDY	SPI1_RDY	USART2_CTS / USART2_NSS	UART4_TX	SPI2_NSS/ I2S2_WS	-	-	-	-	TIM2_ETR	EVENTOUT
	PA1	-	TIM2_CH2	-	TIM8_BKIN	TIM15_CH1N	LPTIM1_IN1	-	USART2_RTS	UART4_RX	-	-	-	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	-	LPUART1_RX	TIM15_CH1	LPTIM1_IN2	-	USART2_TX	-	-	-	-	-	-	COMP2_OUT	EVENTOUT
	PA3	-	TIM2_CH4	-	LPUART1_TX	TIM15_CH2	SPI2_NSS/ I2S2_WS	SPI2_MOSI/ I2S2_SDO	USART2_RX	-	-	-	-	-	-	COMP1_OUT	EVENTOUT
	PA4	-	TIM1_BKIN2	-	-	SPI1_MOSI/ I2S1_SDO	SPI1_NSS/ I2S1_WS	SPI2_NSS/ I2S2_WS	USART2_CK	-	-	-	-	-	-	-	EVENTOUT
	PA5	-	TIM2_CH1	TIM1_CH3	TIM8_CH1N	-	SPI1_SCK/ I2S1_CK	SPI2_SCK/ I2S2_CK	USART1_CTS / USART1_NSS	-	-	-	-	-	-	TIM2_ETR	EVENTOUT
	PA6	-	TIM1_BKIN	-	TIM8_BKIN	-	SPI1_MISO/ I2S1_SDI	-	USART1_TX	LPUART1_RTS	-	-	-	-	-	-	EVENTOUT
	PA7	-	TIM1_CH1N	-	TIM8_CH1N	TIM15_CH1	SPI1_MOSI/ I2S1_SDO	SPI2_MISO/ I2S2_SDI	USART1_RX	LPUART1_CTS	-	-	-	-	-	COMP2_OUT	EVENTOUT
	PA8	MCO1	TIM1_CH1	I3C1_SDA	TIM8_BKIN2	TIM15_CH2	SPI1_RDY	SPI2_MOSI/ I2S2_SDO	USART1_CK	-	I2C1_SCL	-	-	-	USB_SOF	TIM2_CH4	EVENTOUT
	PA9	MCO2	TIM1_CH2	I3C1_SCL	LPUART1_TX	TIM15_CH1N	SPI2_SCK/ I2S2_CK	-	USART1_TX	-	I2C1_SMBA	-	-	-	TIM8_CH2N	-	EVENTOUT
	PA10	-	TIM1_CH3	-	LPUART1_RX	-	-	-	USART1_RX	-	FDCAN2_TX	-	-	-	-	-	EVENTOUT
	PA11	-	TIM1_CH4	-	LPUART1_CTS	USART2_TX	SPI2_NSS/ I2S2_WS	UART4_RX	USART1_CTS / USART1_NSS	I2C1_SCL	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	LPUART1_RTS	USART2_RX	SPI2_SCK/ I2S2_CK	UART4_TX	USART1_RTS	I2C1_SDA	FDCAN1_TX	-	-	-	-	COMP2_OUT	EVENTOUT
	PA13	JTMS/SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	COMP1_OUT	EVENTOUT
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1	TIM1_CH2N	LPTIM1_ETR	I2C1_SMBA	SPI1_NSS/ I2S1_WS	SPI2_NSS/ I2S2_WS	USART2_CK	UART4_RTS	-	-	USART1_TX	-	TIM8_CH4N	TIM2_ETR	EVENTOUT
Port B	PB0	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI1_MISO/ I2S1_SDI	-	USART2_TX	UART4_CTS	-	-	-	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_NSS/ I2S2_WS	-	USART2_RX	-	-	-	-	-	-	COMP1_OUT	EVENTOUT
	PB2	RTC_OUT2	-	-	TIM8_CH4N	SPI1_RDY	LPTIM1_CH1	SPI2_SCK/ I2S2_CK	SPI2_MOSI/ I2S2_SDO	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	I3C1_SDA	I2C1_SDA	SPI1_SCK/ I2S1_CK	FDCAN2_RX	USART1_CK	LPUART1_TX	I2C1_SCL	CRS_SYNC	USART1_TX	-	TIM8_CH1	UART5_RTS	EVENTOUT
	PB4	NJTRST	-	TIM15_CH1	I3C1_SCL	LPTIM1_CH2	SPI1_MISO/ I2S1_SDI	FDCAN2_TX	SPI2_NSS/ I2S2_WS	LPUART1_CTS	I2C1_SDA	-	USART1_RX	-	TIM8_CH2	UART5_CTS	EVENTOUT
	PB5	-	-	-	I3C1_SDA	I2C1_SMBA	SPI1_MOSI/ I2S1_SDO	-	-	LPUART1_RTS	FDCAN2_RX	-	USART1_CK	-	TIM8_CH3	UART5_RX	EVENTOUT
	PB6	-	-	-	I3C1_SCL	I2C1_SCL	-	SPI1_MISO/ I2S1_SDI	USART1_TX	LPUART1_TX	FDCAN2_TX	-	USART1_CTS / USART1_NSS	-	TIM8_CH4	UART5_TX	EVENTOUT

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2	I3C1/ TIM1/8/12/15	I3C1/LPTIM1/ LPUART1/ TIM8	I2C1/2/I3C1/ LPTIM1/SPI1/ I2S1/TIM15/ USART1/2	I3C1/LPTIM1/ SPI1/I2S1/ SPI2/ I2S2/SYS	FDCAN2/ SPI1/ I2S1/SPI2/ I2S2/UART4	SPI2/I2S2/ USART1/2	I2C1/ LPUART1/ UART4/5	FDCAN1/2/ I2C1/ SPI2/I2S2	CRS	USART1	-	TIM8/USB_	COMP1/2/ TIM2/UART5	SYS
Port B	PB7	-	-	-	I3C1_SDA	I2C1_SDA	-	SPI1_SCK/ I2S1_CK	USART1_RX	LPUART1_RX	FDCAN1_TX	-	USART1_RTS	-	-	-	EVENTOUT
	PB8	-	TIM1_CH1	-	I3C1_SCL	I2C1_SCL	-	SPI1_NSS/ I2S1_WS	-	UART4_RX	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PB9	-	-	-	I3C1_SDA	I2C1_SDA	SPI2_NSS/ I2S2_WS	SPI1_SCK/ I2S1_CK	-	UART4_TX	FDCAN1_TX	-	-	-	-	-	EVENTOUT
	PB10	-	TIM2_CH3	TIM8_CH1	LPTIM1_IN1	I2C1_SCL	SPI2_SCK/ I2S2_CK	-	USART2_TX	-	-	-	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	TIM8_CH3	-	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	USART2_CK	-	FDCAN2_RX	-	-	-	-	UART5_RX	EVENTOUT
	PB13	-	TIM1_CH1N	TIM8_CH2	LPTIM1_CH1	I2C1_SMBA	SPI2_SCK/ I2S2_CK	-	USART2_CTS / USART2_NSS	LPUART1_RX	FDCAN2_TX	-	-	-	-	UART5_TX	EVENTOUT
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/ I2S2_SDI	-	USART2_RTS	UART4_RTS	-	-	-	-	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/ I2S2_SDO	SPI1_MOSI/ I2S1_SDO	-	UART4_CTS	-	-	-	-	-	UART5_RX	EVENTOUT
Port C	PC0	-	-	-	-	-	-	-	SPI2_RDY	-	-	-	-	-	-	-	EVENTOUT
	PC1	TRACED0	-	-	-	-	SPI2_MOSI/ I2S2_SDO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	PWR_CSLEEP	-	-	-	-	SPI2_MISO/ I2S2_SDI	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC3	PWR_CSTOP	-	-	LPUART1_TX	-	SPI2_MOSI/ I2S2_SDO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC4	-	TIM2_CH4	-	TIM8_BKIN	-	I2S1_MCK	-	USART2_RX	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	TIM1_CH4N	-	TIM8_BKIN2	-	-	-	-	-	-	-	-	-	-	COMP1_OUT	EVENTOUT
	PC6	-	-	TIM12_CH1	TIM8_CH1	-	I2S2_MCK	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC7	-	-	-	TIM8_CH2	-	-	I2S1_MCK	-	-	-	-	-	-	-	-	EVENTOUT
	PC8	TRACED1	-	-	TIM8_CH3	-	-	-	-	UART5_RTS	-	-	-	-	-	-	EVENTOUT
	PC9	MCO2	-	TIM12_CH2	TIM8_CH4	-	AUDIOCLK	-	-	UART5_CTS	I2C1_SDA	-	-	-	-	-	EVENTOUT
	PC10	-	-	-	TIM8_CH1N	I3C1_SCL	-	SPI2_SCK/ I2S2_CK	USART2_TX	UART4_TX	-	-	-	-	-	-	EVENTOUT
	PC11	-	-	-	TIM8_CH2N	I3C1_SDA	-	SPI2_MISO/ I2S2_SDI	USART2_RX	UART4_RX	-	-	-	-	-	-	EVENTOUT
	PC12	TRACED3	-	TIM15_CH1	TIM8_CH3N	-	-	SPI2_MOSI/ I2S2_SDO	USART2_CK	UART5_TX	-	-	-	-	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	FDCAN1_TX	-	-	-	-	-	EVENTOUT
	PC14	-	-	TIM12_CH1	-	-	-	-	-	-	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PC15	-	-	TIM12_CH2	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port D	PD2	TRACED2	-	-	-	TIM15_BKIN	-	-	-	UART5_RX	-	-	-	-	-	-	EVENTOUT
Port E	PE2	TRACECLK	LPTIM1_IN2	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	I2C1_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	I2C1_SCL	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	MCO1	-	-	LPTIM1_IN2	-	-	-	-	-	FDCAN1_RX	-	-	-	-	-	EVENTOUT

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.62 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 11.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 12.

Figure 11. Pin loading conditions

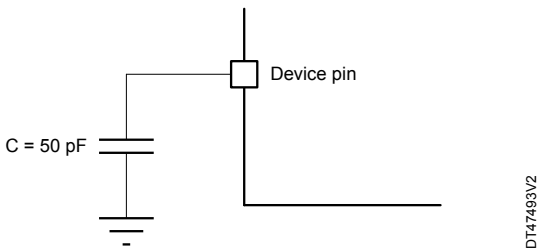
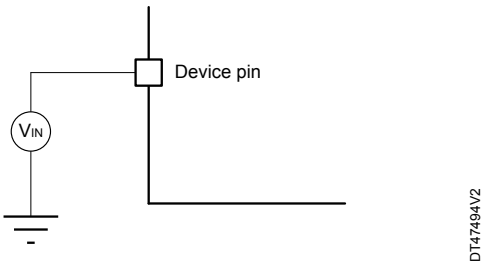


Figure 12. Pin input voltage



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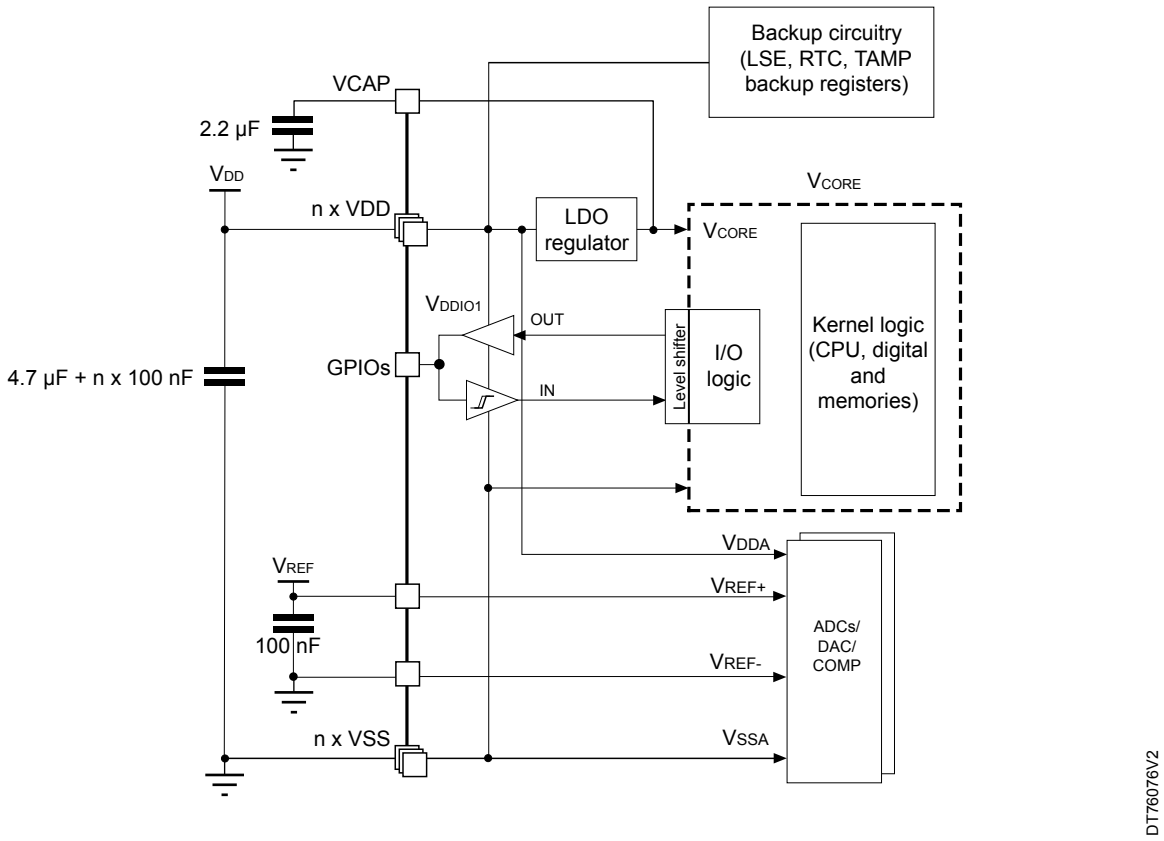
5.1.6 Power supply scheme

Each power supply pair must be decoupled with filtering ceramic capacitors as shown in the following figures. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the proper functionality of the device.

Figure 13. STM32C542xx power supply scheme



The external capacitor on VCAP pin requires the following characteristics:

- COUT = 2.2 µF
- COUT ESR < 20 mΩ at 3 MHz
- COUT rated voltage ≥ 10 V

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5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 14, Table 15, and Table 16 may damage permanently the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard. Extended mission profiles are available on demand.

Table 14. Voltage characteristics

All main power (VDD) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.
The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA} and V_{REF+})	−0.3	4.0	V
V_{IN}[1]	Input voltage on FT_xxx pins	VSS−0.3	MIN (V_{DD} + 4.0V , 6.0 V)[2]	V
	Input voltage on TT_xx pins	VSS−0.3	4.0	V
V_{REF+}-V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V
$\|\Delta V_{DDX}\|$	Variations between different VDDX power pins of the same domain	-	50.0	mV
|VSSx-VSS|	Variations between all the different ground pins	-	50.0	mV

1. *V_{IN} maximum must always be respected. Refer to Table 15 for the maximum allowed injected current values.*
2. *When the analog option is selected by enabling analog peripheral or the pull-up/pull-down resistors are enabled on a given pin, V_{IN} must not exceed 4 V.*

Table 15. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)[1]	200	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)[1]	200	
IV_{DD}	Maximum current into each VDD power pin (source)[1]	100	
IV_{SS}	Maximum current out of each VSS ground pin (sink)[1]	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins[2]	140	
	Total output current sourced by sum of all I/Os and control pins[2]	140	
$I_{INJ(PIN)}$[3][4]	Injected current on FT_xx, TT_xx, RST pins	-5/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)[5]	±25	

1. *All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supplies, in the permitted range.*
2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins, referring to high pin count QFP packages.*
3. *A negative injection is induced by V_{IN} < V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer also to Table 14 for the minimum allowed input voltage values.*
4. *Positive injection (when V_{IN} > V_{DDIOx}) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*
5. *When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the negative injected currents (instantaneous values).*

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Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}/V_{DDA}	Standard operating voltage	-	2.7[1]	-	3.6	V
V_{IN}	I/O Input voltage	All I/O except TT_xx	V_{SS}−0.3	-	MIN (V_{DD} + 3.6V , 5.5 V)[2]	
		TT_xx I/O	V_{SS}−0.3	-	V_{DD} + 0.3	
V_{CAP}	Internal regulator ON	RUN, SLEEP, STOP0 Modes	1.15	1.20	1.26	
		STOP1 Mode	0.9	0.95	1.0	
f_{HCLK}	AHB clock frequency	-	-	-	144	MHz
f_{PCLK}	APB clock frequency	-	-	-	144	
P_D	Power dissipation at T_A = 85 °C for suffix 6[3]	-	See Section 6.10: Package thermal characteristics for application appropriate thermal resistance and package. Power dissipation is then calculated according ambient temperature (T_A) and maximum junction temperature (T_J) and selected thermal resistance.			mW
	Power dissipation at T_A = 125 °C for suffix 3[3]					
T_A	Ambient temperature for suffix 3 version	-	-40	-	125	°C
	Ambient temperature for suffix 6 version	-	-40	-	85	
T_J	Junction temperature range for suffix 3 version	-	-40	-	140	°C
	Junction temperature range for suffix 6 version.	-	-40	-	105	

1. *When RESET is released, the functionality is guaranteed down to PDR minimum voltage.*
2. *For operation with voltage higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled. The minimum and maximum input voltage (Vin) must comply with the selected peripheral enabled on the given GPIOs. Refer to the respective peripheral characteristics for details.*
3. *If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see Section 6.10: Package thermal characteristics).*

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5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in Table 17.

Table 18. Operating conditions at power-up/power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise-time rate	0	∞	µs/V
	V_{DD} fall-time rate	0	∞	ms/V

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature conditions summarized in Table 17.

Table 19. Embedded reset and power control block characteristics

The values in this table are evaluated by characterization - Not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[(1)(2)]	Reset temporization after POR released	V_{DD} rising	-	-	463	µs
$V_{POR/PDR}$	Power-on/power-down reset threshold (BORH_EN =0)	Rising edge	2.56	2.61	2.64	V
		Falling edge	2.53	2.58	2.61	
V_{PVD}	Programmable Voltage Detector threshold	Rising edge	3.00	3.04	3.08	
		Falling edge	2.89	2.93	2.96	
$V_{hyst_POR_PDR}$	Hysteresis for power-on/power-down reset	-	-	30	-	mV
V_{hyst_PVD}	Hysteresis voltage of PVD	-	-	110	-	
I_{DD_PVD}[(2)]	PVD consumption from VDD	-	-	-	0.63	µA

1. *Specified by design - Not tested in production.*
2. *From POR threshold crossing to NRST pull-up resistor activation.*

5.3.4 Inrush current and inrush electric charge characteristics

The parameters provided in the following table are specified by design simulation and are not tested in production.

Table 20. Embedded internal voltage reference

The typical values are provided for V_{DD} = 3.3V and for a typical decoupling capacitor value .
The product consumption on V_{DDCORE} is not included in the inrush current and inrush electric charge

Symbol	Parameter	Typ	Unit
I_{RUSH}	Inrush current during voltage regulator power-on (POR) or wake-up from standby	35	mA
Q_{RUSH}	Inrush electric charge during voltage regulator power-on (POR) or wake-up from standby.	2.8	µC

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5.3.5 Embedded voltage reference

The parameters provided in Table 21. Embedded internal voltage reference are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 5.3.1.

Table 21. Embedded internal voltage reference

The values in this table are specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40°C < T_J < 140 °C	1.180	1.217	1.250	V
$t_{S_vrefint}$ (1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
$t_{start_vrefint}$ (2)	Start time of reference voltage buffer when ADC is enable	-	-	-	4.4	µs
I_{refbuf} (2)	Reference Buffer consumption for ADC	V_{DDA} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT} (2)	Internal reference voltage spread over the temperature range	-40 °C < T_J < 140 °C	-	5	15	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	19	67	ppm/°C
$V_{DDcoeff}$	Average Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V

1. *The shortest sampling time for the application can be determined by multiple iterations.*
2. *Specified by design - Not tested in production.*

Table 22. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	0x08FFF810 - 0x08FFF812

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Current consumption measurement.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the tables *Number of wait states according to CPU clock (HCLK) frequency* available in the product reference manual).
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

The parameters given in the tables below are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 5.3.1: General operating conditions. If not specified otherwise, typical data are measured with a V_{DD} supply of 3.0 V, and maximum data are measured at 3.6 V.

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5.3.6.1 Current consumption in Run mode

Table 23. Typical and maximum current consumption in Run mode

Evaluated by characterization - not tested in production, unless otherwise stated.
Clocked by HSI at 144 MHz or HSIDIV3 at 48MHz if not otherwise specified.

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max LDO					Unit
					T_J = 30°C	T_J = 90°C	T_J = 110°C	T_J = 130°C	T_J = 140°C	
$I_{DD(Run)}$[1]	Supply current in Run mode with all peripheral clocks disabled	Code in Flash, ICACHE 2-way	144	10.0	10.50	12.00	13.50	15.00	16.50	mA
			48	3.7	3.85	5.10	6.50	8.15	9.90	
		Code in Flash, ICACHE OFF	144	9.6	9.85	11.00	12.50	14.00	15.50	
			48	3.9	4.20	5.40	6.80	8.45	10.00	
		Code in SRAM2, ICACHE OFF, FLASH ON	144	9.1	9.35	10.50	12.00	13.50	15.00	
			48	3.3	3.40	4.65	6.00	7.70	9.45	
	Supply current in Run mode with all peripheral clocks enabled	Code in flash, ICACHE 2-way	144[2]	19.5	20.0	21.0	22.5	24.0	26.5	
		Code in flash, ICACHE OFF	144[2]	19.0	19.0	20.0	21.75	23.5	25.5	

1. *Measurements done with prefetch enabled.*
2. *Clocked by PSI at 144 MHz with HSE at 16 MHz in bypass mode.*

Table 24. Typical current consumption in Run mode with CoreMark running from flash memory and SRAM

Evaluated by characterization - not tested in production, unless otherwise stated.

Symbol	Parameter	Conditions	SYSCLK source	f_{HCLK} (MHz)	Typ	Unit	Typ	Unit
		Peripheral						
$I_{DD(Run)}$	Supply current in Run mode	Code in flash, ICACHE 2-way, prefetch ON	PSI [1]	144	10.50	mA	72.50	µA/ MHz
		Code in flash, ICACHE 1-way, prefetch ON			9.15		63.50	
		Code in flash, ICACHE OFF, prefetch ON			9.95		69.00	
		Code in flash, ICACHE OFF, prefetch OFF			8.70		60.50	
		SRAM2, ICACHE 2-way			10.00		69.50	
		Code in SRAM2, ICACHE 1-way			8.75		61.00	
		Code in ICACHE OFF			9.30		64.50	

1. *Clocked by PSI 144 MHz with HSE at 16 MHz on bypass mode.*

5.3.6.2 Current consumption in Sleep mode

Table 25. Typical and maximum current consumption in Sleep mode

Evaluated by characterization - Not tested in production.
Clocked by HSI at 144MHz of HSIDIV3 at 48MHz.

Symbol	Parameter	Conditions	(MHz)	Typ	Max					Unit
					T_J = 30°C	T_J = 90°C	T_J = 110°C	T_J = 130°C	T_J = 140°C	
$I_{DD(SLEEP)}$	Supply current in Sleep mode	All peripheral clocks disabled	144	2.00	2.15	3.40	4.95	6.45	8.15	mA
			48	0.90	1.05	2.35	3.85	5.35	7.10	
		All peripheral clocks enabled	144	12.50	11.00	12.00	13.50	15.00	16.50	
			48	4.50	4.00	5.25	6.80	8.30	10.00	

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5.3.6.3 Current consumption in Stop mode

Table 26. Typical and maximum current consumption in Stop mode

Evaluated by characterization - not tested in production, unless otherwise stated.

Symbol	Parameter	Conditions		Typ	Max					Unit
					T_J = 30°C	T_J = 90°C	T_J = 110°C	T_J = 130°C	T_J = 140°C	
$I_{DD(STOP)}$	FLASH ON	SRAM1/2 ON	STOP0	0.17	0.31	1.40	2.75	4.05	5.55	mA
			STOP1	0.06	0.13	0.80	1.65	2.50	3.50	
	FLASH IN LOW POWER	SRAM1/2 ON	STOP0	0.16	0.29	1.40	2.75	4.05	5.45	
			STOP1	0.04	0.12	0.78	1.65	2.50	3.50	
		SRAM1/2 powered down	STOP0	0.16	0.29	1.40	2.70	4.00	5.45	
			STOP1	0.04	0.12	0.78	1.65	2.50	3.50	

Table 27. Typical and maximum HSIKERON current consumption in Stop mode

Evaluated by characterization - not tested in production, unless otherwise stated.

Symbol	Parameter	Conditions		Typ	Max					Unit
					T_J = 30°C	T_J = 90°C	T_J = 110°C	T_J = 130°C	T_J = 140°C	
$I_{DD(Stop)}$	FLASH IN LOW POWER	HSIKERON, STOP0	HSI144	0.42	0.55	1.65	2.95	4.25	5.50	mA
			HSI48	0.35	0.48	1.60	2.90	4.20	5.50	

5.3.6.4 Current consumption in Standby mode

Table 28. Typical and maximum current consumption in Standby mode

Evaluated by characterization - not tested in production, unless otherwise stated.

Symbol	Parameter	RTC and LSE [1]	Typ			Max					Unit
			2.7 V	3 V	3.3 V	T_J = 30°C	T_J = 90°C	T_J = 110°C	T_J = 130°C	T_J = 140°C	
$I_{DD(Standby)}$	Supply current in Standby mode, IWDG OFF	OFF	2.60	2.75	2.85	3.85	7.70	14.00	27.00	42.50	µA
		ON	2.95	3.10	3.25	-	-	-	-	-	
	Supply current in Standby mode, IWDG ON	OFF	2.60	2.75	2.85	5.50	7.65	13.50	26.50	42.00	
		ON	2.9	3.05	3.25	-	-	-	-	-	

1. *LSE is in bypass mode at 32.768 kHz.*

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5.3.6.5 *Current consumption from peripherals*

Table 29. Peripheral current consumption measured in Sleep mode

Bus	Peripheral	IDD(Typ)	Unit
AHB1	SRAM1	0.28	µA/MHz
	RAMCFG	0.82	
	ICACHE	0.57	
	CRC	0.94	
	FLASH	7.11	
	LPDMA1	1.20	
	LPDMA2	1.37	
	SRAM2	0.33	
AHB2	RNG	0.76	µA/MHz
	AES	1.36	
	HASH	0.65	
	DAC1	1.00	
	ADC1	2.84	
	GPIOA	0.09	
	GPIOB	0.01	
	GPIOC	0.02	
	GPIOD	0.01	
	GPIOE	0.00	
	GPIOH	0.10	
APB1	FDCAN	2.64	µA/MHz
	CRS	0.23	
	I2C1	1.90	
	I3C1	0.41	
	UART5	3.27	
	UART4	3.30	
	USART2	3.73	
	COMP	0.03	
	SPI2/I2S2	1.56	
	OPAMP1	0.55	
	WWDG	0.19	
	TIM2	0.35	
	TIM6	0.26	
	TIM7	0.30	
	TIM12	0.32	
APB2	USB	1.95	µA/MHz
	USART1	3.34	
	SPI1/I2S1	1.41	
	TIM1	0.47	

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Bus	Peripheral	IDD(Typ)	Unit
APB2	TIM8	0.41	µA/MHz
	TIM15	0.44	
APB3	RTC	3.28	µA/MHz
	LPTIM1	0.91	
	LPUART1	2.54	
	SBS	0.45	

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5.3.7 Wake-up time from low-power modes and voltage scaling transition times

The wake-up times given in the table below are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (wait for event) instruction

Table 30. Wake-up time from low-power modes

1. Evaluated by characterization - Not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Symbol	Parameter	Conditions	Wakeup clock	f_{HCLK} (MHz)	Typ	Unit
$t_{wu(Sleep)}$	Wakeup from Sleep	Instruction cache enabled or disabled, HSI 48 MHz	-	-	16	CPU clock cycles
		Instruction cache enabled or disabled, HSI 144 HHz				
$t_{wu(Stop)}$	Wakeup from Stop 0	Flash memory in normal mode	HSI	144	3.85	µs
		Flash memory in low-power mode	HSI	144	7.55	
		Flash memory in normal mode	HSI DIV3	48	5.65	
		Flash memory in low-power mode	HSI DIV3	48	9.20	
	Wakeup from Stop 1	Flash memory in normal mode	HSI	144	37.50	
		Flash memory in low-power mode	HSI	144	41.00	
		Flash memory in normal mode	HSI DIV3	48	39.00	
		Flash memory in low-power mode	HSI DIV3	48	43.00	
$t_{wu(Standby)}$	Wakeup from Standby mode	-	-	-	445	

Table 31. Wake-up time using USART/LPUART

Symbol	Parameter	Condition	Typ	Max(1)	Unit
$t_{WUUSART}$/ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when USART/LPUART clock source is 48 MHz by HSIDIV3	Stop 0 mode	4.8	6.6	µs
		Stop 1 mode			

1. *Specified by design - Not tested in production.*

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5.3.8 External clock timing characteristics

5.3.8.1 *High-speed external user clock generated from an external source*

In bypass mode, the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in I/O port characteristics. However, the recommended clock input waveform is shown in the figure below.

Table 32. High-speed external user clock characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Digital mode (HSEYBYP = 1, HSEEXT = 1)	-	-	50	MHz
		Analolog mode (HSEYBYP = 1, HSEEXT = 0)	4	-	50	
V_{HSEH}	OSC_IN input pin high-level voltage	Digital mode (HSEYBYP = 1, HSEEXT = 1)	0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage	Digital mode (HSEYBYP = 1, HSEEXT = 1)	V_{SS}	-	0.3 × V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Digital mode (HSEYBYP = 1, HSEEXT = 1)	7	-	-	ns
$DuCy_{HSE}$	OSC_IN duty cycle	Digital mode (HSEYBYP = 1, HSEEXT = 1)	45	-	55	%
$V_{HSE_ext_PP}$	OSC_IN peak-to-peak amplitude	Analog mode (HSEBYP = 1, HSEEXT = 0)	0.2	-	2/3 V_{DD}	V
V_{HSE_ext}	OSC_IN input range		0	-	V_{DD}	
$t_{r(HSE)}$, $t_{f(HSE)}$	OSC_IN rise and fall time		0.05 / f_{ext_ext}	-	0.3 / f_{ext_ext}	ns

1. *There is no specified rise and fall time for a digital input signal, but the V_{HSEH} and V_{HSEL} conditions must be fulfilled .*
2. *The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS}.*

Figure 14. AC timing diagram for high-speed external clock source (digital mode)

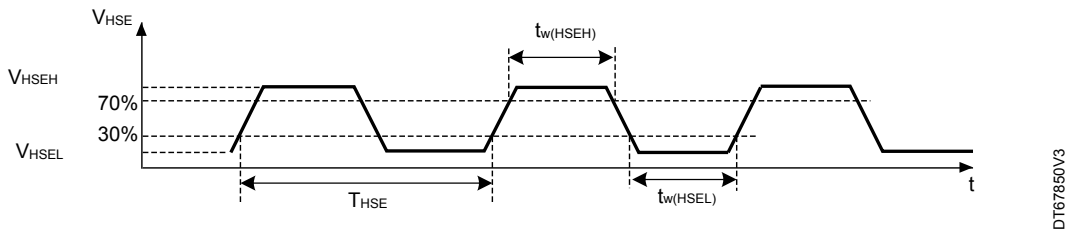
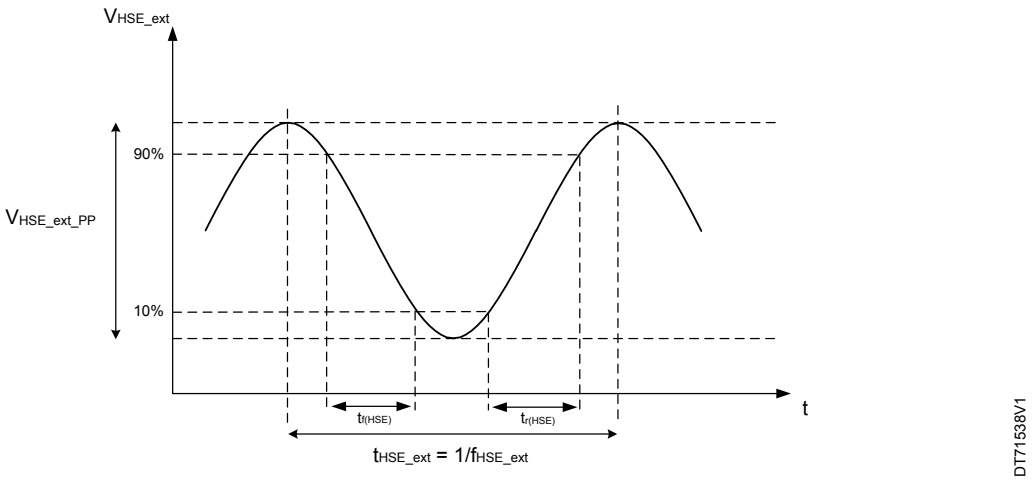


Figure 15. AC timing diagram for high-speed external clock source (analog mode)



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5.3.8.2 *Low-speed external user clock generated from an external source*

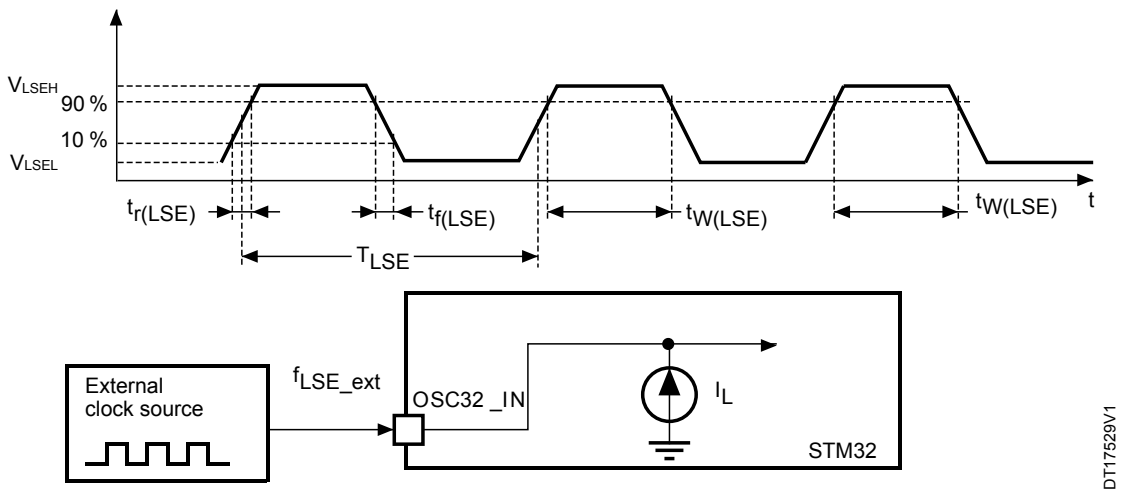
In bypass mode, the LSE oscillator is switched off and the input pin is directly connected to the LSE clock detector (LSECSS). The external clock signal has to respect the parameters specified in Table 33, as shown also by the waveforms in Figure 16.

Table 33. Low-speed external user clock characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC_IN input high level	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	External digital clock	V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}/t_{w(LSEL)}$	OSC32_IN high or low time	External digital clock	250	-	-	ns
V_{lsw_H}	Analog low swing OSC_IN high level	External analog low swing clock	0.6		1.225	V
V_{lsw_L}	Analog low swing OSC_IN low level	External analog low swing clock	0.35		0.8	
V_{lswLSE} (V_{LSEH} - V_{LSEL})	Analog low swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2		0.875	
$DuCy_{LSE}$	Analog low swing OSC_IN duty cycle	External analog Low Swing Clock	45	50	55	%
t_{rLSE}/t_{fLSE}	Analog low swing OSC_IN rise and fall time	Externala analog low swing clock 10 % to 90 %	-	100	200	ns

Figure 16. Low-speed external clock source AC timing diagram



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5.3.8.3 High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below.

In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins, in order to minimize the output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 34. 4-50 MHz HSE oscillator characteristics

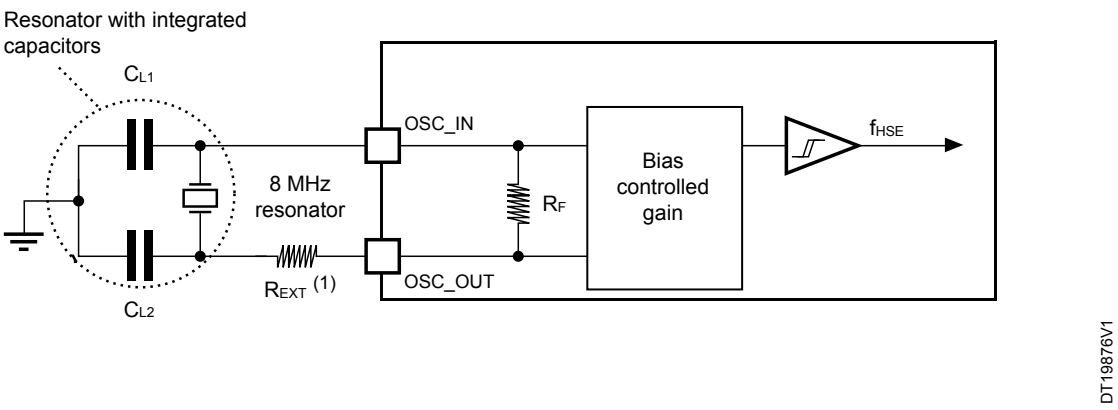
Specified by design and not tested in production.

Symbol	Parameter	Operating conditions[1]	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
RF	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup[2]	-	-	10	mA
		V_{DD} = 3 V, Rm = 20 Ω C_L=10 pF at 4 MHz	-	0.4	-	
		V_{DD}=3 V, Rm = 20 Ω C_L = 10 pF at 8 MHz	-	0.4	-	
		V_{DD} = 3 V, Rm = 20 Ω CL = 10 pF at 16 MHz	-	0.6	-	
		V_{DD} = 3 V, Rm = 20 Ω C_L = 10 pF at 32 MHz	-	0.7	-	
		V_{DD} = 3 V, Rm = 20 Ω C_L=10 pF at 48 MHz	-	1.2	-	
Gmcritmax	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}[3]	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *This consumption level occurs during the first 2/3 of the t_{SU}(HSE) startup time.*
3. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note 'Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs' (AN2867).

Figure 17. Typical application with a 8 MHz crystal



(1): R_{EXT} value depends on the crystal characteristics.

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5.3.8.4 *Low-speed external clock generated from a crystal resonator*

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

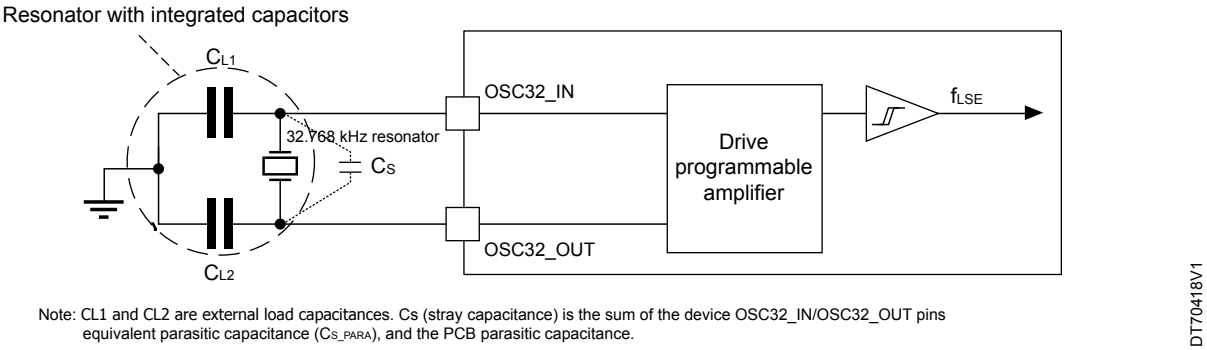
Specified by design and not tested in production.

Symbol	Parameter	Operating conditions[1]	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
Gmcritmax	Maximum critical crystal Gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}[2]	Startup time	V_{DD} is stabilized	-	2	-	s

1. *Refer to the following note and caution paragraphs, and to the application note AN2867 "Oscillator design guide for ST microcontrollers.*
2. *t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note 'Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs' (AN2867).

Figure 18. Typical application with a 32.768 kHz crystal



Note: CL1 and CL2 are external load capacitances. Cs (stray capacitance) is the sum of the device OSC32_IN/OSC32_OUT pins equivalent parasitic capacitance (C_{S_PARA}), and the PCB parasitic capacitance.

Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

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5.3.9 Internal clock timing characteristics

The parameters given in the tables below are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. The curves provided are characterization results, not tested in production.

5.3.9.1 High-speed internal HSI144 oscillator

Table 36. HSI144 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}[1]	HSI frequency	V_{DD} = 3.3 V, T_J = 30 °C	144.07	-	145.08	MHz
TRIM[2]	USER trimming step	-	-	0.1	0.15	%
USER TRIM COVERAGE[2]	USER TRIMMING Coverage positive	80 steps	5.2%	8%	-	
	USER TRIMMING Coverage negative	48 steps	-3.1%	-4.8%	-	
DuCy(HSI)[2]	Duty Cycle	-	45		55	
Δ_{TEMP} (HSI)[3]	HSI oscillator frequency drift over temperature (the reference is 144 MHz.)	T_J = -20 to 130 °C	-1	-	1	
		T_J = −40 to T_{Jmax} °C	-1.5	-	1.5	
$\Delta_{VDD(HSI)}$[2][4]	HSI oscillator frequency drift with V_{DD}Section 5.3.9.1: High-speed internal HSI144 oscillator Section 5.3.9.1: High-speed internal HSI144 oscillator(the reference is 3.3V)	V_{DD} from 2.7 V to 3.6 V	-	-	- 0.1	
$t_{su(HSI)}$[3]	HSI oscillator start-up time (PSI Off)	-	-	3	4.5	µs
	HSI oscillator start-up time (PSI On)	-	-	0.5	-	
t_{stab}[2]	stabilization time (PSI OFF from Enable)	+/-1% of target freq	-	-	8	
	stabilization time (PSI ON from Enable)		-	-	0.7	
$I_{DD(HSI)}$[2][5]	HSI supply regulation block oscillator power consumption	-	-	91	-	µA
	HSI oscillator power consumption	-	-	28	-	
N_T jitter[2]	Next transition jitter[6].	On HSIDIV3	-	52	322	ps
P_T jitter[2]	Paired transition jitter[7]		-	62	394	
P_{er} jitter[2]	Period Jitter standard deviation	On HSIS		15		
		On HSIDIV3		26		

1. *Tested in production.*
2. *Specified by design - Not tested in production.*
3. *Evaluated by characterization - Not tested in production.*
4. $\Delta f_{HSI} = \Delta TEMP + \Delta_{VDD}$
5. *The supply regulation consumption is common to HSI and PSI. (To be counted once if both oscillators are ON).*
6. *Jitter measurements are performed without clock source activated in parallel. Typical value is standard deviation, Maximum is peak measure on TIE-8 over 36 cycles.*
7. *Jitter measurements are performed without clock source activated in parallel. Typical value is standard deviation, Maximum is peak measure on TIE-16 over 36 cycles.*

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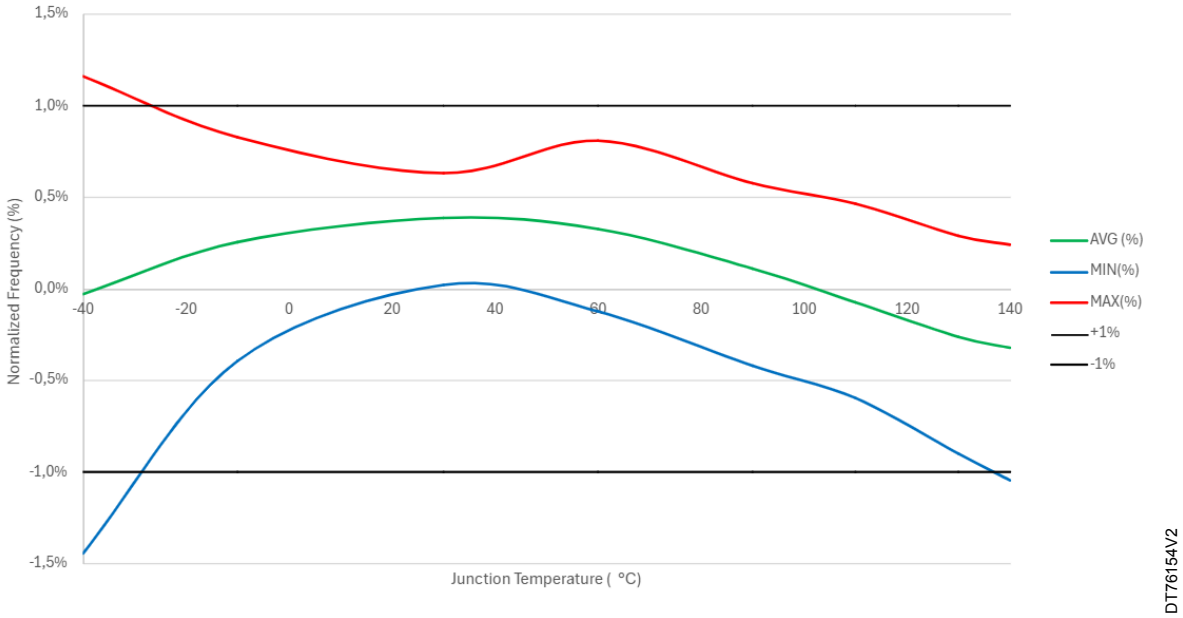
Figure 19. HSI frequency versus temperature



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5.3.9.2 PSI oscillator characteristics

Table 37. PSI oscillator characteristics

Symbol	Parameter	Conditions	Min[1]	Typ	Max	Unit
f_{PSI}	PSI potential frequency	If reference is HSE at 8, 16, 24, 32 or 48 MHz or HSIDIV18	-	100	-	MHz
			-	144	-	
			-	160[2]	-	
		If reference is HSE at 25 or 50 MHz	-	100	-	
			-	141.67	-	
			-	158.33[2]	-	
		If reference is LSE at 32 KHz	-	100.008	-	
			-	144.015	-	
			-	160.006[2]	-	
DuCy(PSI)[3]	Duty Cycle	-	45		55	%
$t_{su(PSI)}$[4]	PSI startup time	On 32 KHz	-	850	1750	µs
	PSI startup time	On 8 MHz	-	25	45	µs
$I_{DD(PSI)}$[3][5]	PSI supply regulation bloc oscillator power consumption	If HSI not ON	-	91	-	µA
	PSI oscillator power consumption	100 MHz	-	95	-	
	PSI oscillator power consumption	144 MHz	-	68	-	
	PSI oscillator power consumption	160 MHz	-	77	-	
N_T jitter[3]	Next transition jitter[6]	On PSIDIV3 (48 MHz with 32 kHz CK_IN)	-	46.8	264	ps
		On PSIDIV3 (48 MHz with 8 MHz CK_IN)	-	52.6	276	ps
P_T jitter[3]	Paired transition jitter [7]	On PSIDIV3 (48 MHz with 32 kHz CK_IN)	-	54.4	331	ps
		On PSIDIV3 (48 MHz with 8 MHz CK_IN)	-	60.6	367	ps
P_{er} jitter[3]	Period Jitter standard deviation	On PSIS (100 MHz)	-	15.5	-	ps
		On PSIDIV3 (33.33 MHz)	-	27	-	ps
		On PSIS (144 MHz)	-	14	-	ps
		On PSIDIV3 (48 MHz)	-	24.5	-	ps
		On PSIS (160 MHz)	-	13.5	-	ps
		On PSIDIV3 (53.33 MHz)	-	23	-	ps
LT jitter[3]	Long term jitter ethernet	On PSIS (100 MHz with 32 kHz CK_IN)	-	-	13.7 (RMS) 96.7 (peak)	ns
		On PSIS	-	-	0.79 (RMS)	ns

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Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
LT jitter(3)	Long term jitter ethernet	(100 MHz with 8 MHz CK_IN)			6.69 (peak)	
	Long term jitter FDCAN	On PSIK (40 MHz with 32 kHz CK_IN)	-	-	13.3 (RMS) 83.6 (peak)	ns
		On PSIK (40 MHz with 8 MHz CK_IN)	-	-	0.775 (RMS) 6.16 (peak)	ns

1. *Tested in production.*
2. *Frequencies above the supported product's maximum frequency can only be used once divided through PSIK or PSIDIV4 dividers.*
3. *Specified by design - Not tested in production.*
4. *Evaluated by characterization - Not tested in production.*
5. *The supply regulation consumption is common to HSI and PSI. (To be counted once if both oscillators are ON)*
6. *Jitter measurements are performed without clock source activated in parallel. The typical value refer to the standard deviation, while the maximum is the peak measurement of TIE-8 over 36 cycles.*
7. *Jitter measurements are performed without clock source activated in parallel. The typical value refer to the standard deviation, while the maximum is the peak measurement of TIE-16 over 36 cycles.*

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5.3.9.3 *Low-speed internal (LSI) RC oscillator*

Table 38. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 30°C	31.4(1)	32	32.6(1)	kHz
		T_J = -40 to 130°C	29.4(2)	-	33.6(2)	
		T_J = -40 to 140°C	28.6(2)	-	33.6(2)	
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	130	280	nA

1. *Guaranteed by test production.*
2. *Evaluated by characterization - Not tested in production.*
3. *Specified by design - Not tested in production.*

5.3.10 Flash memory characteristics

Table 39. Flash memory characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Word program	-	1	-	mA
		Page erase	-	0.8	-	
		Mass erase	-	0.8	-	

Table 40. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
tprog	Word programming time	128 bits (user area)	-	20.0	160.0	µs
		16 bits (OTP / EDATA area)	-	20.0	160.0	
t_{ERASE} 8KB	Page (8 KB) erase time	-	-	2.0	2.1	ms
t_{ERASE} 2KB	Page (2 KB) erase time	-	-	2.0	2.1	
t_{ME}	Bank Mass erase time	-	-	64.0	68.0	
	Mass erase time	-	-	128.0	135.0	
V_{prog}	Programming voltage	-	2.65	-	3.6	V

1. *Evaluated by characterization - Not tested in production.*

Table 41. Flash memory user and EDATA endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_J = -40 to 140 °C	10	Kcycle
t_{RET}	Data retention	1 Kcycle at T_J = 125 °C	10	Year
		1 Kcycle at T_J = 85 °C	30	
		10 Kcycle at T_J = 55 °C	30	

1. *Evaluated by characterization - Not tested in production.*

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5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through the I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs as follows:

- Electrostatic discharge (ESD) (positive and negative): applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB (fast transient voltage burst) (positive and negative): applied to VDD and VSS pins through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the table below. They are based on the EMS levels and classes defined in application note *EMC design guide for STM8, STM32 and Legacy MCUs* (AN1709).

Table 42. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25°C, f_{HCLK} = 144 MHz, LQFP64 package conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25°C, f_{HCLK} = 144 MHz, LQFP64 package conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

The EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Note that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for one second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note *Software techniques for improving microcontrollers EMC performance (AN1015)* for more details.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard that specifies the test board and the pin loading.

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Table 43. EMI characteristics for f_{HSE} = 8 MHz and f_{HCLK} = 144 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, T_A = 25 ° C, LQFP64 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	10	dBµV
			30 MHz to 130 MHz	-1	
			130 MHz to 1 GHz	13	
			1 GHz to 2 GHz	11	
	Level[2]		0.1 MHz to 2 GHz	3.0	-

1. *Refer to the EMI radiated test section of the application note EMC design guide for STM8, STM32 and Legacy MCUs (AN1709).*
2. *Refer to the EMI level classification section of the application note EMC design guide for STM8, STM32 and Legacy MCUs (AN1709).*

5.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, latch-up) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 44. ESD absolute maximum ratings

Specified by design and not tested in production.

Symbol	Ratings	Conditions	Packages	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C conforming to ANSI/ESDA/JEDEC JS-001	LQFP64	2	3100[2]	V
			LQFP48			
			UFQFPN48			
			LQFP32	3A	4000	
			UFQFPN32			
			UFQFPN24			
			UFQFPN20			
			TSSOP20			
VESD(CDM)	Electrostatic discharge voltage (charge device model)	TA = 25°C conforming to ANSI/ESDA/JEDEC JS-002	LQFP64	C3	1000	
			LQFP48		1250	
			UFQFPN48		1250	
			LQFP32		1250	
			UFQFPN32		1250	
			UFQFPN24		1250	
			UFQFPN20		1250	
			TSSOP20		1250	

1. *Evaluated by characterization - Not tested in production.*
2. *All pins are characterized at a maximum value of 4000 V, except for PC15, whose maximum value is 3100 V.*

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Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output, and configurable I/O pin.

These tests are compliant with EIA/JESD 78E IC latch-up standard.

Table 45. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 130°C conforming to JESD78	Level II A

5.3.13 I/O current injection characteristics

As a general rule, the current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) must be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller if abnormal injection accidentally happens, some susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating-input mode. While this current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter, such as an ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the 5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in the table below. The negative induced leakage current is caused by the negative injection. The positive induced leakage current is caused by the positive injection.

Table 46. I/O current injection susceptibility

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
Evaluated by characterization - Not tested in production.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on PA4 and PA5 pins	0	0	mA
	Injected current on PB3, PB4, PB5, PB6, PB12, PB13, PB14, PC13, PC14, PC15 and PH0 pins	0	N/A	
	Injected current on all other pins	5	N/A	

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5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 47 are derived from tests performed under the conditions summarized in Table 17. All I/Os are designed as CMOS and TTL-compliant.

Note: For information on GPIO configuration, refer to the application note STM32 GPIO configuration for hardware settings and low-power consumption (AN4899).

Table 47. I/O static characteristics

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in the figure below.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	2.7 V<V_{DDIOx}<3.6 V	-	-	$0.3V_{DD}$ (1)	V
	I/O input low level voltage		-	-	$0.4\ V_{DD} - 0.1$(2)	
V_{IH}	I/O input high level voltage	2.7 V < V_{DDIOx} < 3.6 V	$0.7V_{DD}$ (1)	-	-	V
	I/O input high level voltage		$0.52V_{DD} + 0.18$(2)	-	-	
I_{leak} (3)	FT_xx Input leakage current(2)	0 < V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±-200	nA
		Max(V_{DDXXX}) < V_{IN} ≤ Max(V_{DDXXX} + 1 V)(5)(6)(4)	-	-	±2500	
		Max(V_{DDXXX} + 1) < V_{IN} ≤ 5.5 V (5)(6)(4)	-	-	750	
	TT_xx Input leakage current	0 < V_{IN} ≤ Max(V_{DDXXX} + 1 V)(4)	-	-	±200	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Compliant with CMOS requirements.*
2. *Specified by design - Not tested in production.*
3. *This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: ITotal_Ileak_max = 10 µA + [number of I/Os where V_{IN} is applied on the pad] × Ilkg max.*
4. *Max(V_{DDXXX}) is the maximum value of all the I/O supplies.*
5. *To sustain a voltage higher than the minimum of V_{DD} or V_{DDA} plus 0.3 V, disable the internal pull-up and pull-down resistors.*
6. *V_{IN} must be less than Max(V_{DDXXX}) + 3.6 V.*
7. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in the following figure.

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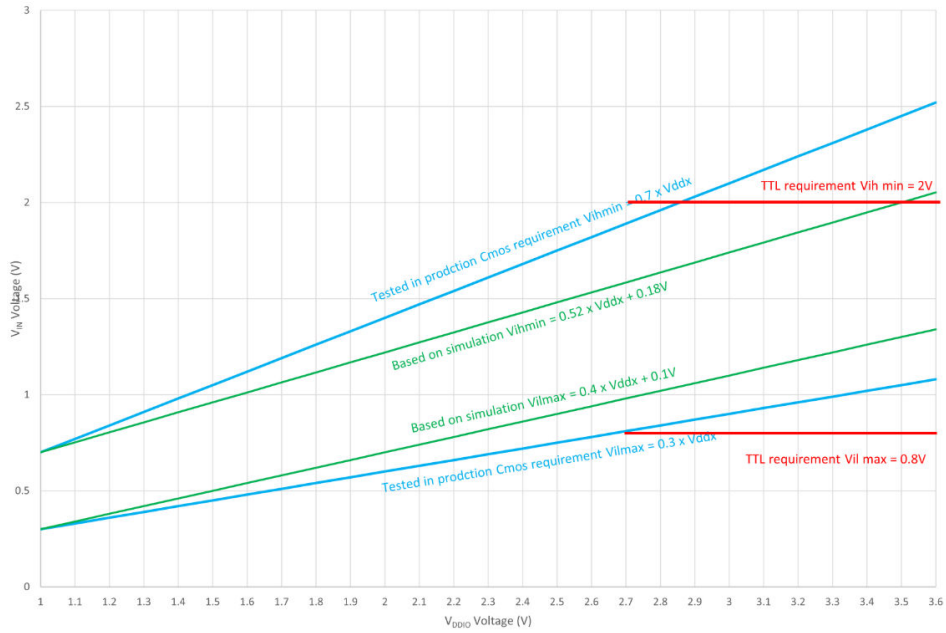
Figure 20. I/O input characteristics (all I/Os)



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Output driving current

The GPIOs (except PC13, PC14, PC15) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}). PC13, PC14, PC15 are limited in source capability: +3 mA shared between the I/Os.

In the user application, the number of I/O pins tat can drive current must be limited to respect the absolute maximum rating specified in Section 5.2: Absolute maximum ratings:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $\sum I_{VDD}$ (see Table 15. Current characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating $\sum I_{VSS}$ (see Table 15. Current characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 17. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

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Table 48. Output voltage characteristics (all I/Os except PC14 and PC15)

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in the FOLLOWING figure.
The minimum and maximum values are specified for a junction temperature (T_J) of 125°C.

Symbol	Parameter	Conditions[2]	Min	Max	Unit
V_{OL}	Output low-level voltage	CMOS port[1], $\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high-level voltage	CMOS port[1], $\|I_{IO}\|$ = -8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}[2]	Output low-level voltage	TTL port[1],$\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[2]	Output high-level voltage	TTL port[1],$\|I_{IO}\|$ = -8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[2]	Output low-level voltage	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD}≤ 3.6 V	-	1.3	
V_{OH}[2]	Output high-level voltage	$\|I_{IO}\|$ = -20 mA, 2.7 V ≤ V_{DD}≤ 3.6 V	V_{DD} - 1.3	-	
V_{OLFM+}[2]	Output low-level voltage for a FT_f I/O pin in FM+ mode	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
2. *Specified by design - Not tested in production.*

Table 49. Output voltage characteristics for PC14 and PC15

Specified by design and not tested in production.
The minimum and maximum values are specified for a junction temperature T_J = 125°C.
The IIO current sourced or sunk by the device must always comply with the absolute maximum rating specified in Table 15. Current characteristics. Additionally, the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always comply with the absolute maximum ratings ΣIIO.

Symbol	Parameter	Conditions(3)	Min	Max	Unit
VOL	Output low level voltage	CMOS port[1] IIO=0.5 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
VOH	Output high level voltage	CMOS port[1] IIO=-0.5 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD} - 0.4	-	
VOL[2]	Output low level voltage	TTL port[1] IIO = 0.5 mA 2.7 V ≤ V_{DD} ≤3.6 V	-	0.4	
VOH[2]	Output high level voltage	TTL port[1] IIO = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	

1. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
2. *Specified by design - Not tested in production.*

Output AC characteristics

The definition and values of output AC characteristics are given in Figure 21. Output AC characteristics definition and in the table below respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 17.

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Table 50. Output AC characteristics (all I/Os except PC13)

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the product reference manual for a description of GPIO port configuration register
Specified by design - Not tested in production.
The minimum and maximum values are specified for a junction temperature T_J = 125°C .

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	Fmax(1)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4	
			C = 10 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	4	
	tr/tf (2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	51	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	46	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	40	
01	Fmax(1)	Maximum frequency	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	12	MHz
			C = 30 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	12	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	
	tr/tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	ns
			C = 30 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	17	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤3.6 V	-	14	
10	Fmax(1)(3)	Maximum frequency	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	45	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
	tr/tf(2)(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	7	ns
			C = 30 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	6	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4	
11	Fmax(1)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	90	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	96	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	110	
	tr/tf(2)(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3	

1. *The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T*
2. *The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.*
3. *Compensation system enabled.*

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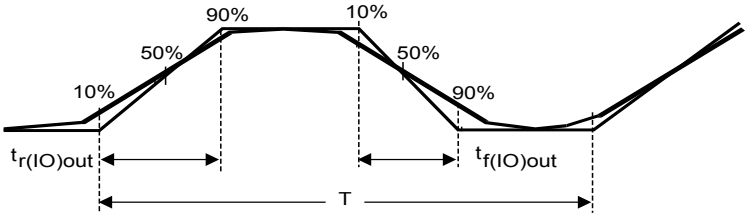
Figure 21. Output AC characteristics definition



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

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5.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 17.

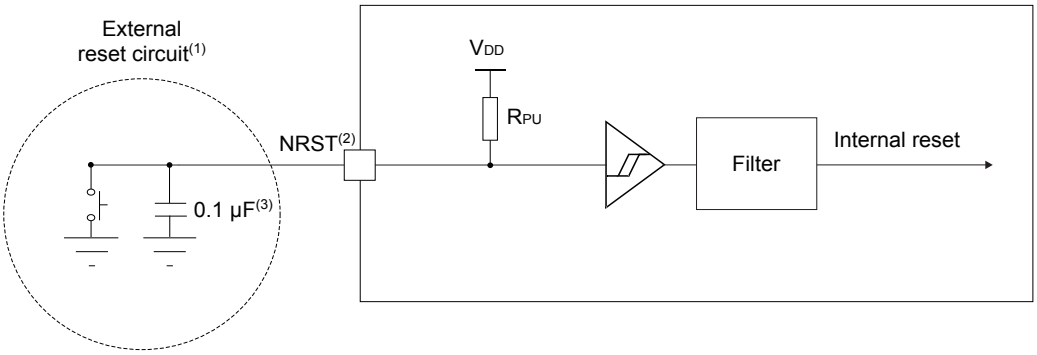
Table 51. NRST pin characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low-level voltage	-	-	-	0.3 x V_{DDIOx}	V
$V_{IH(NRST)}$	NRST input high-level voltage	-	0.7 x V_{DDIOx}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{F(NRST)}$	NRST input filtered pulse	-	-	-	50	ns
$t_{NF(NRST)}$	NRST input not-filtered pulse	2.7 V ≤ V_{DD} ≤ 3.6 V	350	-	-	

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10 % order).*

Figure 22. Recommended NRST pin protection



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(1): The reset network protects the device against parasitic resets.

(2): The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in the above table. Otherwise the reset is not taken into account by the device.

(3): The external capacitor on NRST must be placed as close as possible to the device.

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5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 52. EXTI input characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

5.3.17 12-bit analog-to-digital converter ADC characteristics

Unless otherwise specified, the parameters given in Table 53 are values derived from tests performed under ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage conditions summarized in Table 17.

Note: It is recommended to perform a calibration after each power-up.

Table 53. 12-bit ADC characteristics

Specified by design - Not tested in production.

Symbol	Parameter	Conditions						Min	Typ	Max	Unit
V_{DDA}	Analog power supply for ADC ON	-						2.70	-	3.6	V
V_{REF+}	Positive reference voltage	-						2.5	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-						V_{SSA}			V
f_{ADC}	ADC clock frequency	$2.7V \le V_{DDA} \le 3.6$ V						8	-	36	MHz
f_S with R_{AIN}=47 Ω and C_{PCB} = 22 pF	Sampling rate for slow channels	Resolution = 12 bits	All modes	2.7 V ≤ V_{DDA} ≤ 3.6 V	-40°C ≤ T_J ≤ 140°C	f_{ADC}= 36 MHz	SMP = 2.5	-	2.25	-	MSPS
		Resolution = 10 bits						-	2.57	-	
		Resolution = 8 bits						-	3	-	
		Resolution = 6 bits						-	4.5	-	
t_{TRIG}	External trigger period	Resolution = 12 bits						16	-	-	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-						0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	Resolution = 12 bits, T_J = 140°C						-	-	110	Ω
		Resolution = 12 bits, T_J = 125°C						-	-	610	
		Resolution = 10 bits, T_J = 140°C						-	-	2305	
		Resolution = 10 bits, T_J = 125°C						-	-	4290	
		Resolution = 8 bits, T_J = 140°C						-	-	11110	
		Resolution = 8 bits, T_J = 125°C						-	-	15860	
		Resolution = 6 bits, T_J = 140°C						-	-	46890	
		Resolution = 6 bits, T_J = 125°C						-	-	79000	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup time	-	-	-	10	µs
t_{STAB}	ADC power-up time	LDO already started	1	-	-	conversion cycle
t_{OFF_CAL}	Offset calibration time	-	85			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency for regular and injected channels	Trigger from an asynchronous clock	3	-	4	
		Trigger from a synchronous clock	3			
t_S	Sampling time	-	2.5	-	288.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	t_S + 1.5 + N			
$I_{DDA(ADC)}$	ADC consumption on V_{DD}, V_{DDA} and V_{REF}	f_S = 2.25 MSPS	-	200	-	µA

1. *High temperature generate leakage current on ADC inputs. This current create voltage drop through Rain directly affecting ADC accuracy (the worst case when V_{AIN} = V_{DDA}). To limit this effect to a tolerance of 2LSBs, it must respect rain max tables.*

Table 54. 12-bit ADC accuracy

ADC accuracy values are measured after internal calibration. Resolution = 12 bits, no oversampling.
Evaluated by characterization on LQFP64. Packages without a VREF- pad can have degraded specifications. Not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
ET	Total unadjusted error	-	4	5.7	LSB
EO	Offset error	-	±2.5	±5	
EG	Gain error	-	2.6	6	
ED	Differential linearity error	-1	-	1.3	
EL	Integral linearity error	-3	±2.5	3	
ENOB	Effective number of bits	-	10.7	-	bits
SINAD	Signal-to-noise and distortion ratio	-	66	-	
SNR	Signal-to-noise ratio	-	68	-	dB
THD	Total harmonic distortion	-	-70	-	

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Figure 23. Minimum sampling time versus RAIN for 12 bits resolution

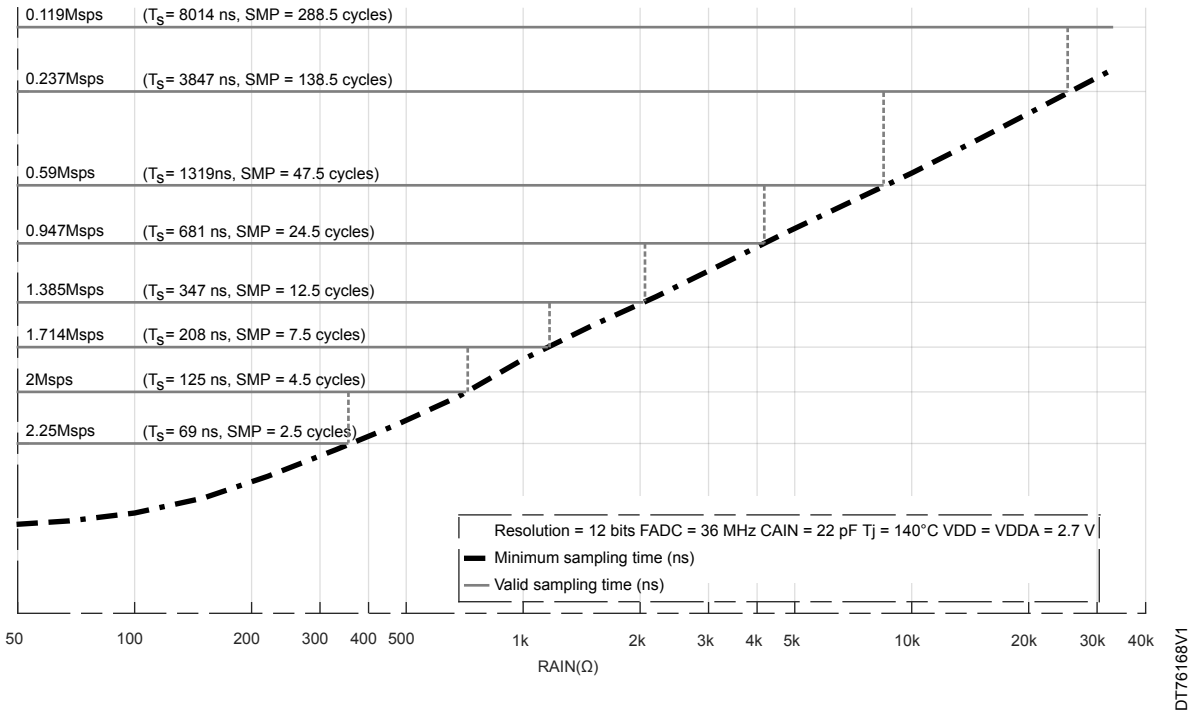

Figure 24. Minimum sampling time versus RAIN for 10 bits resolution

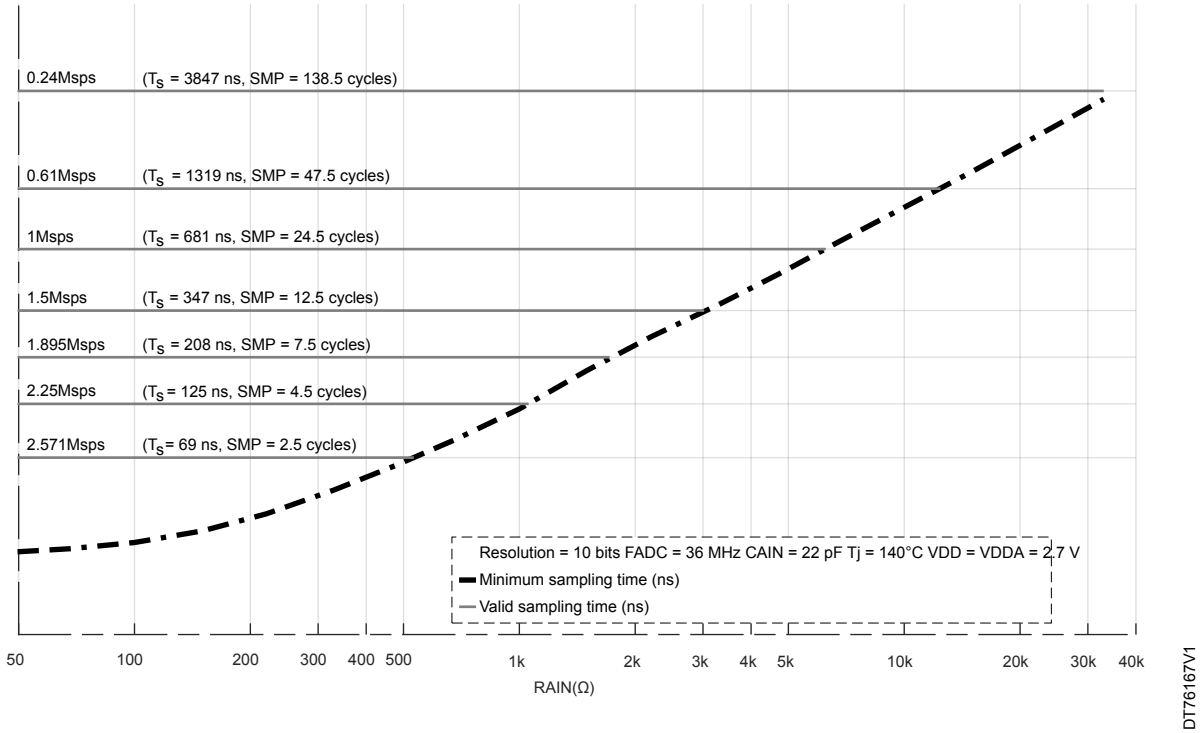

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Figure 25. Minimum sampling time versus RAIN for 8 bits resolution

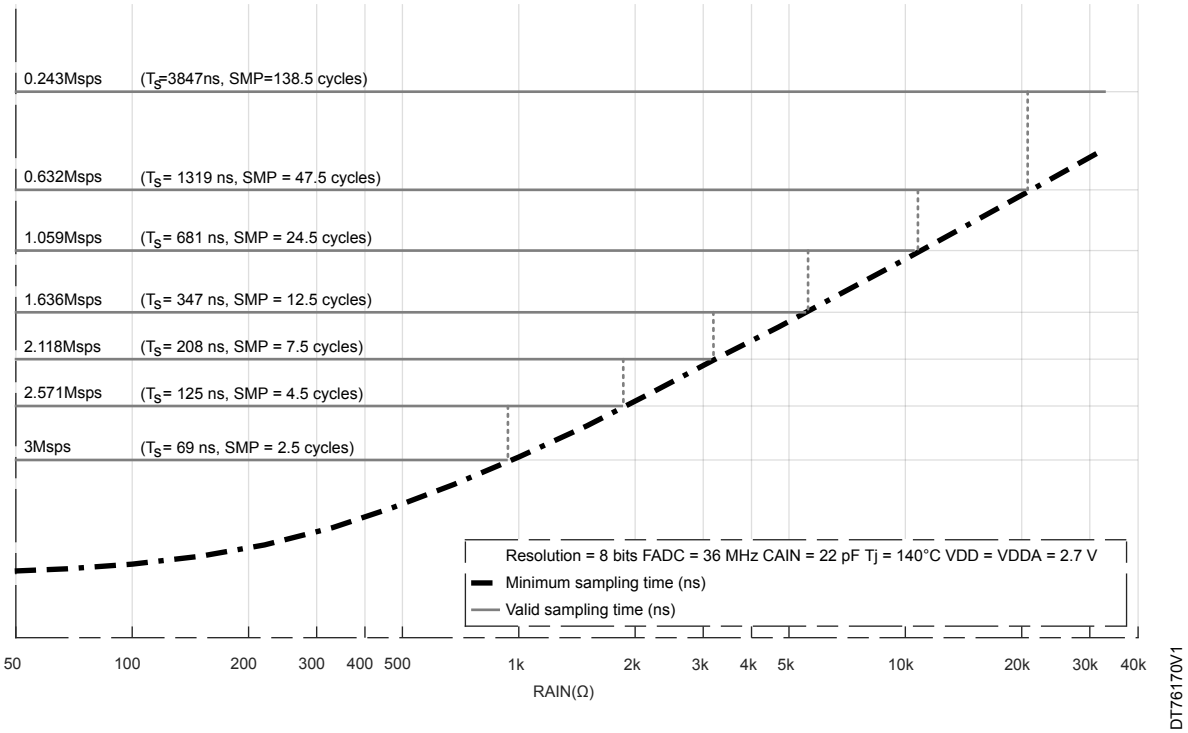

Figure 26. Minimum sampling time versus RAIN for 6 bits resolution

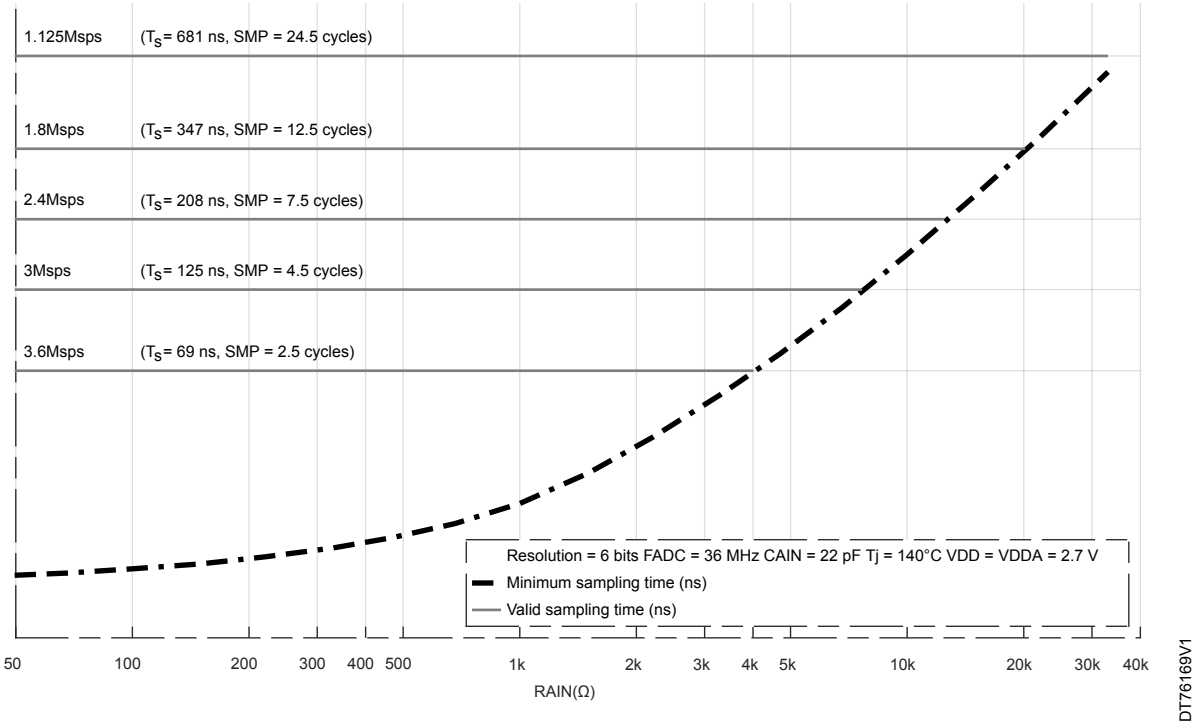

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Figure 27. ADC accuracy characteristics

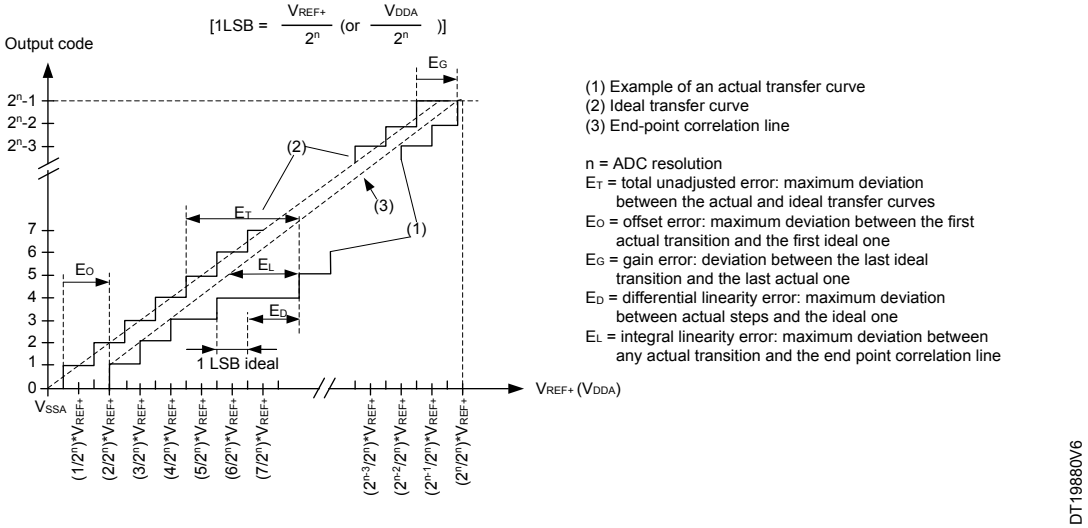
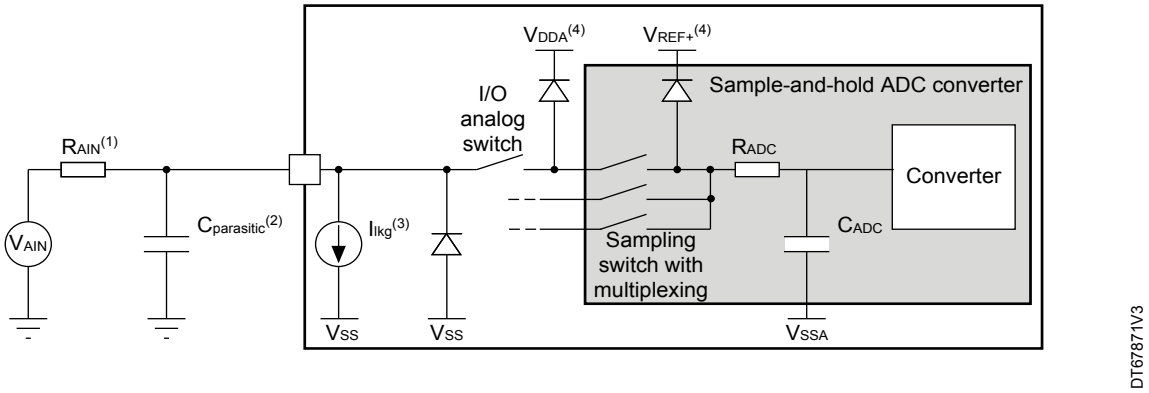


Figure 28. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



(1): Refer to the ADCx characteristic table for the values of R_{AIN} and C_{ADC}.

(2): $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Section 5.3.14: I/O port characteristics for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades the conversion accuracy. To remedy this, f_{ADC} must be reduced.

(3): Refer to Section 5.3.14: I/O port characteristics for the values of I_{lkg}.

(4): Refer to Section 5.1.6: Power supply scheme.

General PCB design guidelines

The power-supply decoupling must be performed as shown in the corresponding power-supply scheme. The 100 nF capacitor must be ceramic (good quality) and must be placed as close as possible to the chip.

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5.3.18 Temperature sensor characteristics

Table 55. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature (from V_{sensor} voltage)	-	-	3	°C
Avg_Slope (2)	Average slope (from V_{sense} voltage)	-	2.14	-	mV/°C
V_{30} (3)	Voltage at 30° C (± 1 ° C)	-	0.65	-	V
t_{start_run} (1)	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp} (1)	ADC sampling time when reading the temperature	13	-	-	
I_{sens} (1)	Sensor consumption	-	0.18	0.29	µA
$I_{sensbuf}$ (1)	Sensor buffer consumption	-	3.8	6.5	

1. *Specified by design - Not tested in production.*
2. *Evaluated by characterization - Not tested in production.*
3. *Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1.*

Table 56. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA} = 3.3 V	0x08FF F814 - 0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 140 °C, V_{DDA} = 3.3 V	0x08FF F818 - 0x08FF F819

5.3.19 Digital-to-analog converter characteristics (DAC)

Table 57. DAC characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.7	-		V
V_{REF+}	Positive reference voltage	-		2.5	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	KΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		10.3	13.00	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	KΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	KΩ
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode			0.10	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode DAC output buffer ON $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.66	2.87	
			±2 LSB	-	1.65	2.84	
			±4 LSB	-	1.63	2.78	
			±8 LSB	-	1.61	2.7	
		Normal mode, DAC output buffer OFF, ±1 LSB C_L = 10 pF		-	1.7	2	
t_{WAKEUP}	Wakeup time from off state (setting the Enx bit in the DAC Control register) until the ±1LSB final value	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, R_L = 5 kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \leq 10$ pF		-	2	5.0	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON $C_L \leq 50$ pF, R_L = 5 kΩ		-	-80	-28	dB
t_{SAMP}	Sampling time in Sample and Hold mode C_{SH}=100nF (Code transition between the lowest input code and the highest input code when DACOUT reaches final value +/- 1LSB)	MODE<2:0>_V12 = 100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12 = 110 (BUFFER OFF)		-	11.5	18.7	
		MODE<2:0>_V12=111 BUFFER OFF (DAC_OUT pin not connected, internal connection only)		-	0.3	0.6	µs
I_{leak}	Output leakage current	-		-	-	-	nA
CI_{int}	Internal sample and hold capacitor	-		1.43	1.75	2	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
I_{DDA}(DAC)	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	-	µA
			No load, worst code (0xF1C)	-	450	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}=100 nF		-	315*Ton/ (Ton+Toff)	-	
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	-	
			No load, worst code (0xF1C)	-	185	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	155	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	185*Ton/ (Ton+Toff)	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	155*Ton/ (Ton+Toff)	-	

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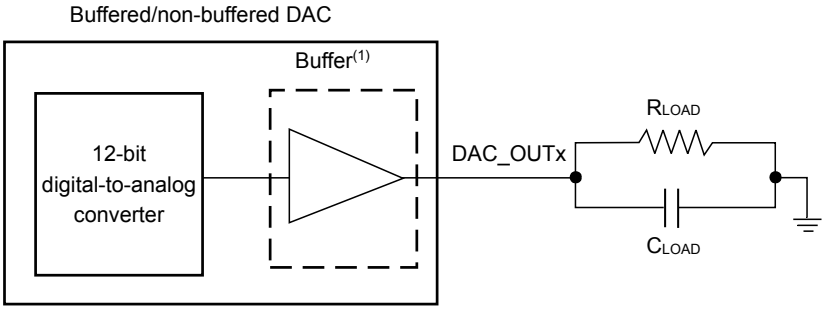
Figure 29. 12-bit buffered/non-buffered DAC



(1) The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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Table 58. DAC accuracy

Specified by design - not tested in production unless otherwise stated.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(1)	DAC output buffer ON		-2	-	2	LSB
		DAC output buffer OFF		-2	-	2	
	Monotonicity	10 bits		-	-	-	-
INL	Integral non linearity(2)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5\ \Omega$		-4	-	4	LSB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-4	-	4	
Offset	Offset error at code 0x800 (2)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5\ \Omega$	V_{REF+} = 3.6 V	-	-	±12	LSB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±8	
Offset1	Offset error at code 0x001(3)	DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5\ \Omega$	V_{REF+} = 3.6 V	-	-	±5	LSB
Gain	Gain error(4)	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5\ \Omega$		-	-	±1	%
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±1	
TUE	Total unadjusted error	DAC output buffer ON $C_L \leq 50$ pF, $R_L \geq 5$ kΩ		-	-	±30	LSB
		DAC output buffer OFF $C_L \leq 50$pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON $C_L \leq 50$pF, R_L>=5kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio(5)	DAC output buffer ON $C_L \leq 50$ pF, $R_L \geq 5$ kΩ 1 kHz, BW 500KHz		-	67.8	-	dB
		DAC output buffer OFF $C_L \leq 50$pF, no RL 1 kHz, BW 500 KHz		-	67.8	-	
THD	Total harmonic distortion(5)	DAC output buffer ON $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, 1 kHz		-	-78,6	-	dB
		DAC output buffer OFF $C_L \leq 50$ pF, no R_L, 1 kHz		-	-78,6	-	
SINAD	Signal-to-noise and distortion ratio(5)	DAC output buffer ON $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, 1 kHz		-	67.5	-	dB
		DAC output buffer OFF $C_L \leq 50$ pF, no R_L, 1 kHz		-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, 1 kHz		-	10.9	-	bits
		DAC output buffer OFF $C_L \leq 50$ pF, no R_L, 1 kHz		-	10.9	-	

1. *Difference between two consecutive codes minus 1 LSB.*
2. *Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.*
3. *Difference between the value measured at Code (0x001) and the ideal value.*
4. *Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.*
5. *The signal is -0.5 dBFS with $F_{sampling}$=1 MHz.*

5.3.20 Comparator characteristics

Table 59. COMP characteristics

The input capacitance is negligible compared to the I/O capacitance.
Specified by design - not tested in production, unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.70	-	3.60	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		(1)		
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)		-	0.82	1	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	2	5	µs
		Medium mode		-	5	20	
t_D[(2)]	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	80	ns
		Medium mode		-	0.5	0.9	µs
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode		-	50	120	ns
		Medium mode		-	0.5	1.2	µs
V_{offset}	Comparator offset error	Full common mode range		-	-	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	10	-	
		Medium hysteresis		-	20	-	
		High hysteresis		-	30	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Medium mode	Static	-	5	9	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	110	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. *Refer to Section 5.3.5: Embedded voltage reference.*
2. *Evaluated by characterization - Not tested in production.*

5.3.21 OPAMP characteristics

Table 60. OPAMP characteristics

Specified by design – not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2.5	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±3	
		All voltages and temperature, no load high speed mode		-	±4	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±10	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1*V_{DDA})	-	-	0.8	-	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9*V_{DDA})	-	-	0.8	-	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CMRR	Common mode rejection ratio	-		-	70	-	dB
PSRR	Power supply rejection ratio	C_{LOAD} ≤ 50 pf / R_{LOAD} ≥ 4 kΩ[1] at 1 kHz, Vcom = V_{DDA}/2		-	70	-	dB
GBW	Gain bandwidth Product	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV		6	15	-	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode		4	7.5	-	V/µs
		High-speed mode		35	65	-	
AO	Open loop gain	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV		58	100	-	dB
φm	Phase margin	-		-	60	-	°
GM	Gain margin	-		-	11	-	dB
V_{OHSAT}	High saturation voltage	I_{load} = max or R_{LOAD} = min[1], Input at V_{DDA}		V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{LOAD} = max or R_{LOAD} = min[1], Input at 0 V		-	-	100	
t_{WAKEUP}	Wake up time from OFF state	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ[1], follower configuration	-	1.1	2.0	µs
		High speed	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ[1], follower configuration	-	1.1	2.0	
PGA gain	Non inverting gain error value	PGA gain = 2		-1		1	%
		PGA Gain = 4		-1		1	
		PGA Gain = 8		-1		1	
		PGA Gain = 16		-1		1	
	Inverting gain error value	PGA Gain = 2		-1		1.4	
		PGA Gain = 4		-1		1	
		PGA Gain = 8		-1		1	
		PGA Gain = 16		-1		1	
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode[2]	PGA Gain = 2		-	10/10	-	kΩ/ kΩ
		PGA Gain = 4		-	30/10	-	
		PGA Gain = 8		-	70/10	-	
		PGA Gain = 16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode[2]	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	
		PGA Gain = -7		-	70/10	-	
		PGA Gain = -15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2		-	GBW/2	-	MHz
		Gain = 4		-	GBW/4	-	
		Gain = 8		-	GBW/8	-	
		Gain = 16		-	GBW/16	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	GBW/2	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PGA BW	PGA bandwidth for different inverting gain	Gain = -3		-	GBW/4	-	MHz
		Gain = -7		-	GBW/8	-	
		Gain = -15		-	GBW/16	-	
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	360	-	nV/√ Hz
		at 10 KHz		-	160	-	
I_{DDA}(OPAMP)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	1.6	2.8	mA
		High- speed mode		-	1.8	3	
		Normal mode	OPAMPint, follower	-	0.8	1.6	
		High- speed mode		-	1	1.8	

1. *R_{LOAD} is the resistive load connected to V_{SSA} or to V_{DDA}.*
2. *R2 is the internal resistance between the OPAMP output and the OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. The programmable gain amplifier (PGA) is calculated as 1 + R2/R1.*

5.3.22 Timer characteristics

The parameters given in Section 5.3.22, Table 62, and Section 5.3.22 are specified by design, not tested in production.

Refer to Table 47. I/O static characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 61. TIMx characteristics

Symbol	Parameter	Conditions	Min	Max	Unit[1]
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 144 MHz	6.9	-	ns
fEXT	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 144 MHz	0	72	
ResTIM	Timer resolution	TIMx (except TIM2/TIM5)	-	16	bit
		TIM2/TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 144 MHz	0.007	455.1	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	4, 294, 967, 296	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 144 MHz	-	29.826	s

1. *TIMx, is used as a general term in which x stands for 1, 2, 5, 6, 7, 8, 12, 15, 16, 17.*

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Table 62. IWDG min/max timeout period at 32 kHz (LSI)

e: For the values in this table, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock, so that there is always a full RC period of uncertainty.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

Table 63. WWDG min/max timeout value at 144 MHz (PCLK)

Prescaler	WDGTB	Min timeout values	Max timeout value	Unit
1	0	0.0284	1.820	ms
2	1	0.0569	3.641	
4	2	0.1138	7.282	
8	3	0.2276	14.564	
16	4	0.4551	29.127	
32	5	0.9102	58.254	
64	6	1.820	116.508	
128	7	3.641	233.017	

5.3.23 I3C interface characteristics

The I3C interface meets the timing requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in Table 64 below are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O Compensation cell activated
- Voltage scaling range 1

The I3C timings are in line with the MIPI specification, except for the ones given in Table 64, I3C open-drain measured timing. For t_{SU_OD}, this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 64. Open drain timing measurements

Evaluated by characterization - Not tested in production.

Symbol	Parameter	Conditions	Min	Unit
t_{SU_OD}	SDA data setup time in open drain mode	Controller 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	22[(1)]	ns

1. *The minimum SDA data setup time during open-drain-mode is 3 ns, as specified in the MIPI Alliance specification for I3C.*

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5.3.24 I²C interface characteristics

The I²C interface meets the timing requirements of the I2C-bus specification and user manual rev. 03 for:

- Standard mode (Sm): Bit rate up to 100 kbit/s.
- Fast mode (Fm): Bit rate up to 400 kbit/s.
- Fast mode plus (Fm+): Bit rate up to 1 Mbit/s.

The I²C timing requirements are specified by design, not tested in production, when the I²C peripheral is properly configured (refer to the product reference manual).

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not true open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled but remains present.
- Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to Section 5.3.14: I/O port characteristics for the I²C I/Os characteristics.

Al I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics.

Table 65. I²C analog filter characteristics

Evaluated by characterization - Not tested in production.
Measurement points are taken at 50% V_{DD}.

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(1)	160(2)	ns

1. *Spikes with widths below $t_{AF(min)}$ are filtered.*
2. *Spikes with widths above $t_{AF(max)}$ are not filtered.*

5.3.25 USART characteristics

Unless otherwise specified, the parameters given in Table 66 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in not found, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 66. USART (SPI mode) characteristics

Evaluated by characterization - Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master transmitter mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	18	
		Slave receiver mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	48	
		Slave transmitter mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	27	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}(1) + 2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(CKH)}$	CK high and low time	Master mode	1/ f_{CK} /2-1	1/ f_{CK} /2	1/ f_{CK} /2+1	
$t_{w(CKL)}$						
$t_{su(RX)}$	Data input setup time	Master mode	18	-	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(RX)}$	Data input setup time	Slave mode		2.5	-	-	ns
$t_{h(RX)}$	Data input hold time	Master mode		0.5	-	-	
$t_{h(RX)}$		Slave mode		1	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode	$2.7\ V \le V_{DD} \le 3.6\ V$	-	13.5	18	
		Master mode	$2.7\ V \le V_{DD} \le 3.6\ V$	-	2	2.5	
$t_{h(TX)}$	Data output hold time	Slave mode		9	-	-	
$t_{h(TX)}$	Data output hold time	Master mode		0.5	-	-	

1. *T_{ker} is the usart_ker_ck_pres clock period.*

Figure 30. USART timing diagram in SPI master mode

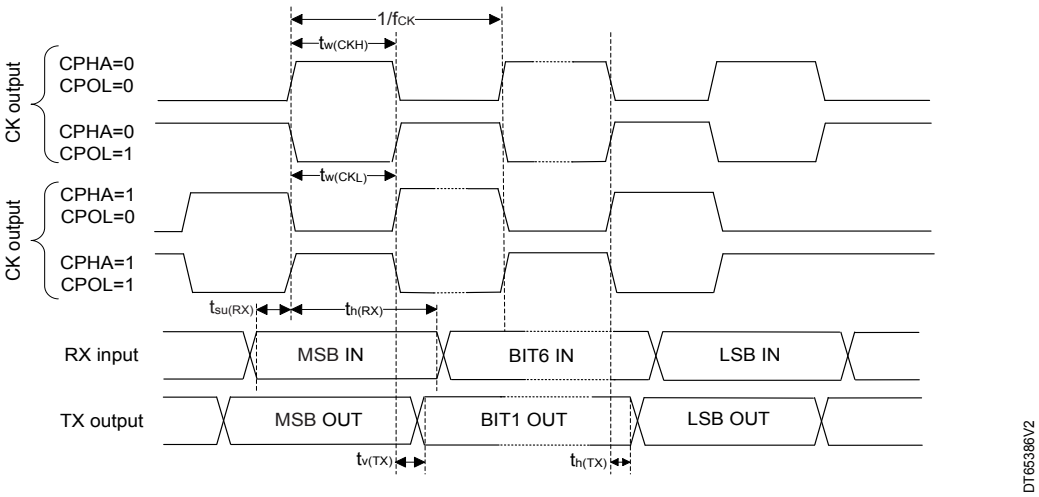
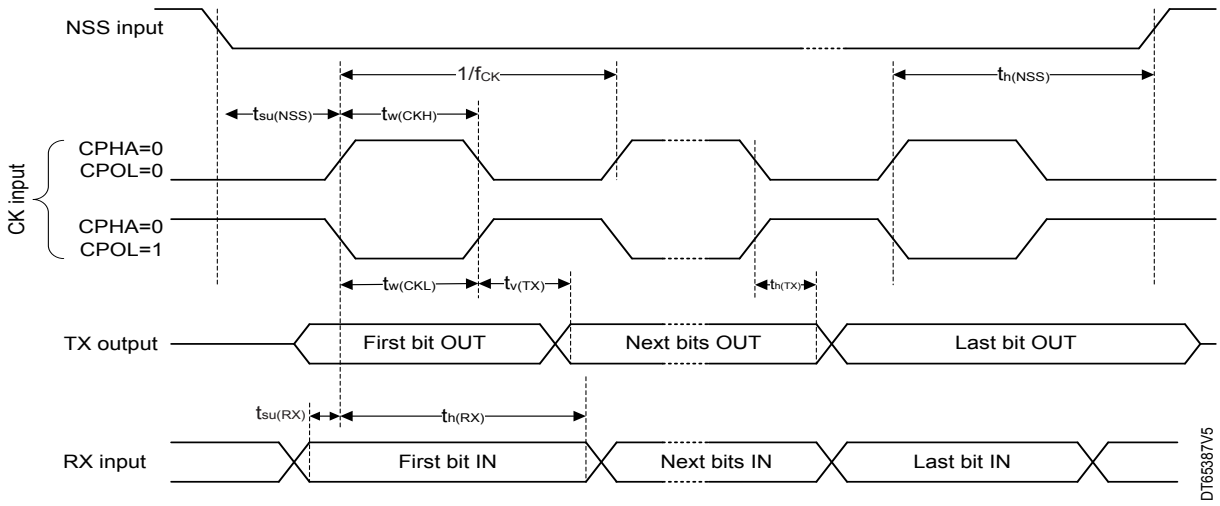


Figure 31. USART timing diagram in SPI slave mode



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5.3.26 SPI characteristics

Unless otherwise specified, the parameters given in Table 67 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in Table 17.

- Output speed set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated

Refer to Table 47. I/O static characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 67. SPI characteristics

Evaluated by characterization - Not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master receiver mode, 2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	72	MHz
		Slave receiver mode, 2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	100	
		Slave transmitter mode, 2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	32	
$t_{su(NSS)}$	NSS setup time	Slave mode		3	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode		1	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode		T_{SCK}(1) - 1	T_{SCK}(1)	T_{SCK}(1)+ 1	
$t_{su(MI)}$	Data input setup time	Master mode	DRDS = 0	2.5	-	-	
			DRDS = 1	13 - T_{SCK}(1)/2	-	-	
$t_{su(SI)}$		Slave mode		2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	DRDS = 0	1	-	-	
			DRDS = 1	T_{SCK}(1)/2 - 8	-	-	
$t_{h(SI)}$		Slave mode		1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode		11	13.5	15.5	
$t_{dis(SO)}$	Data output disable time	Slave mode		8.5	10.5	12.5	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V ≤ V_{DD} ≤ 3.6 V		-	12	15.5	
$t_{v(MO)}$	Data output valid time	Master mode		-	1.5	2	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)		8	-	-	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)		0	-	-	

1. *T_{SCK} = T_{PCLK} × Baud rate prescaler/2.*

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Figure 32. SPI timing diagram - slave mode and CPHA = 0

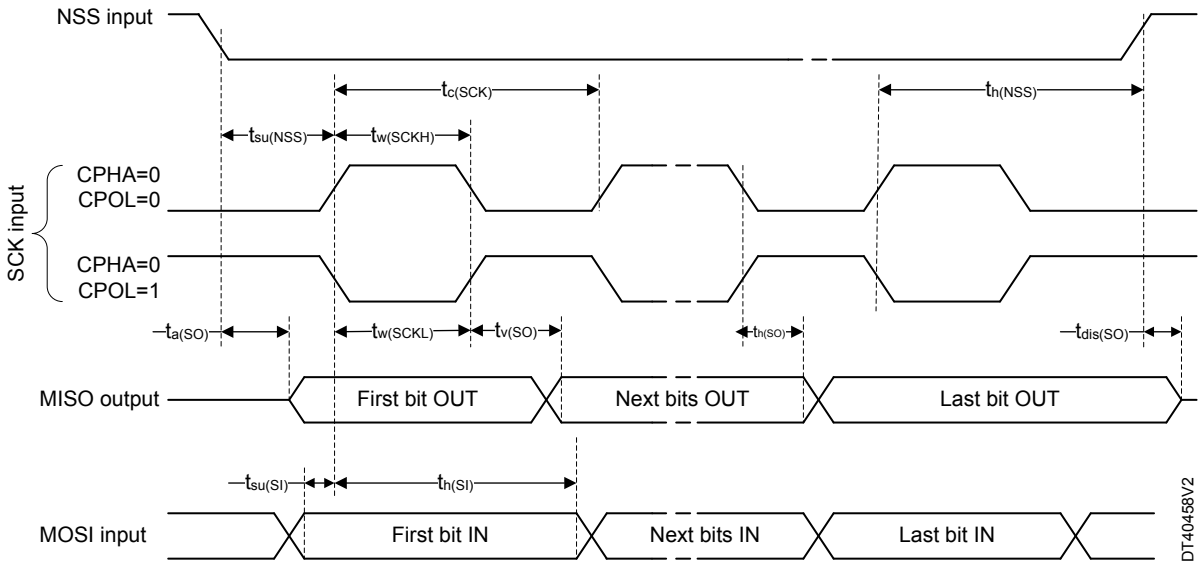
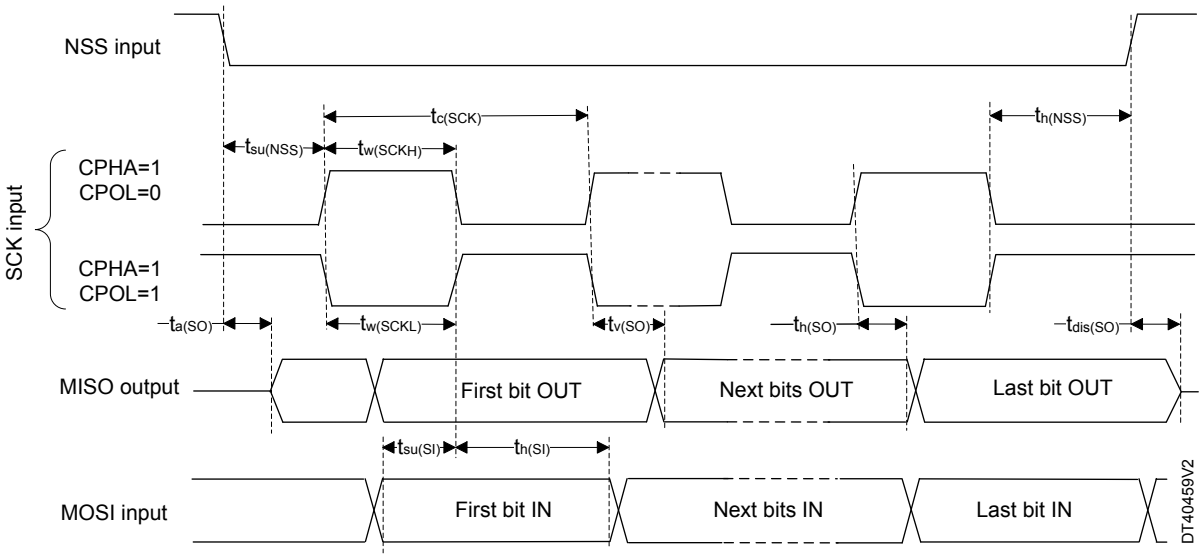


Figure 33. SPI timing diagram - slave mode and CPHA = 1



Note: Measurement points are done at 0.3 V_{DD} and 0.7 V_{DD} levels.

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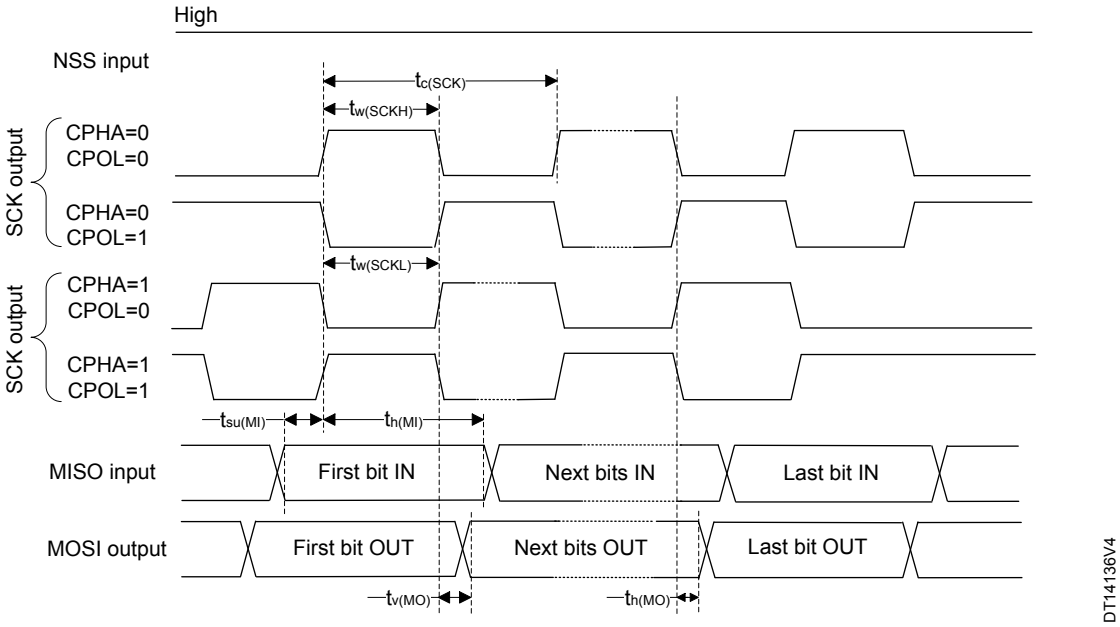
Figure 34. SPI timing diagram - master mode



Note: Measurement points are done at 0.3 V_{DD} and 0.7 V_{DD} levels.

5.3.27 I2S interface characteristics

Unless otherwise specified, the parameters given in **Table xx** for I2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 68. I2S characteristics, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- IO Compensation cell activated

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Refer to Section 5.3.14: I/O port characteristics: I/O port characteristics for more details on the input/output alternate function characteristics (CK, SDO, SDI, WS).

Table 68. I2S characteristics

Evaluated by characterization – Not tested in production.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	-	50	MHz
f_{CK}	I2S clock frequency	Master Tx or RX, slave Rx	-	50	MHz
		Slave Tx	-	17	
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	1	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	2.5	-	ns
$t_{su(SD_SR)}$	Data input setup time	Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	1.5	-	
$t_{h(SD_SR)}$		Slave receiver	2.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	17.5	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	2.5	
$t_{h(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0.5	-	

5.3.28 USB_FS characteristics

Table 69. USB_FS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating supply voltage	-	3.0[(1)]	-	3.6	V
R_{PUI}	Embedded USB_DP pullup value during idle	-	900	-	1575	Ω
R_{PUR}	Embedded USB_DP pullup value during reception	-	1425	-	3090	
Z_{DRV}	Output driver impedance[(2)]	High and low driver	28	36	44	

1. *USB functionality is ensured down to 2.7 V, but some USB electrical characteristics are degraded in 2.7 to 3.0 V range.*
2. *No external termination series resistors are required on USB_DP (D+) and USB_DM (D-). The matching impedance is already included in the embedded driver.*

5.3.29 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 70 and Table 71 are derived from tests performed under the ambient temperature, f_{HCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 17, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level

Refer to Table 47. I/O static characteristics for more details on the input/output characteristics.

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Table 70. JTAG characteristics

Evaluated by characterization - Not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
F_{TCK}	TCK clock frequency	-	-	34	MHz
$ti_{su(TMS)}$	TMS input setup time	2	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	0.5	-	-	
$ti_{su(TDI)}$	TDI input setup time	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	0.5	-	-	
$t_{ov(TDO)}$	TDO output valid time	-	11	14.5	
$t_{oh(TDO)}$	TDO output hold time	7.5	-	-	

Figure 35. JTAG timing diagram

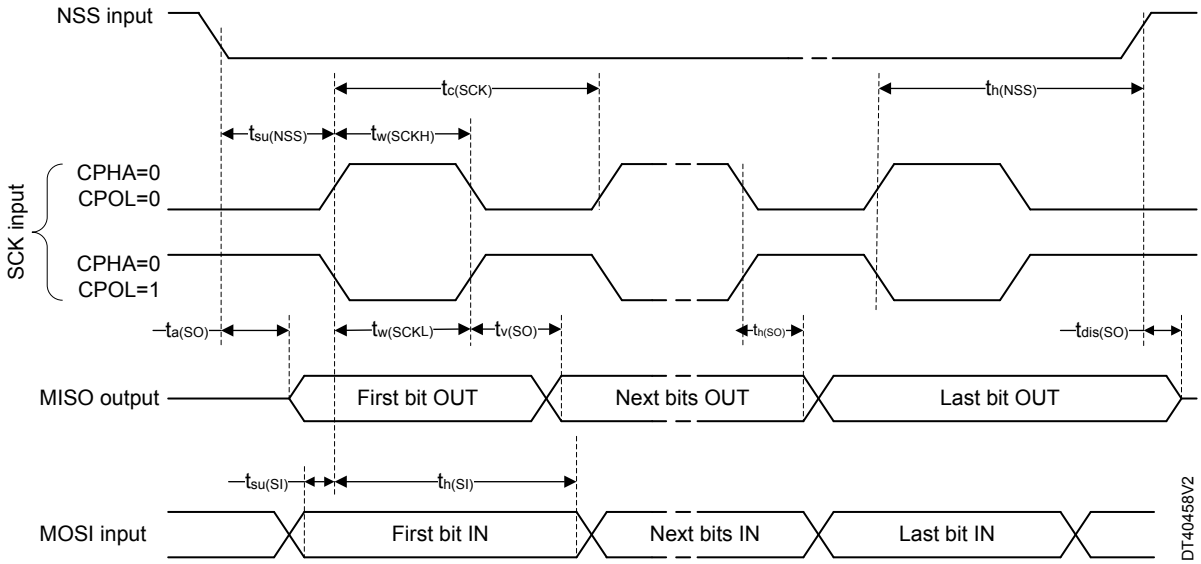

Table 71. SWD characteristics

Evaluated by characterization - Not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
F_{SWCLK}	SWCLK clock frequency	-	-	71	MHz
$ti_{su(SWDIO)}$	SWDIO input setup time	3	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	0.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	-	11.5	14	
$t_{oh(SWDIO)}$	SWDIO output hold time	9.5	-	-	

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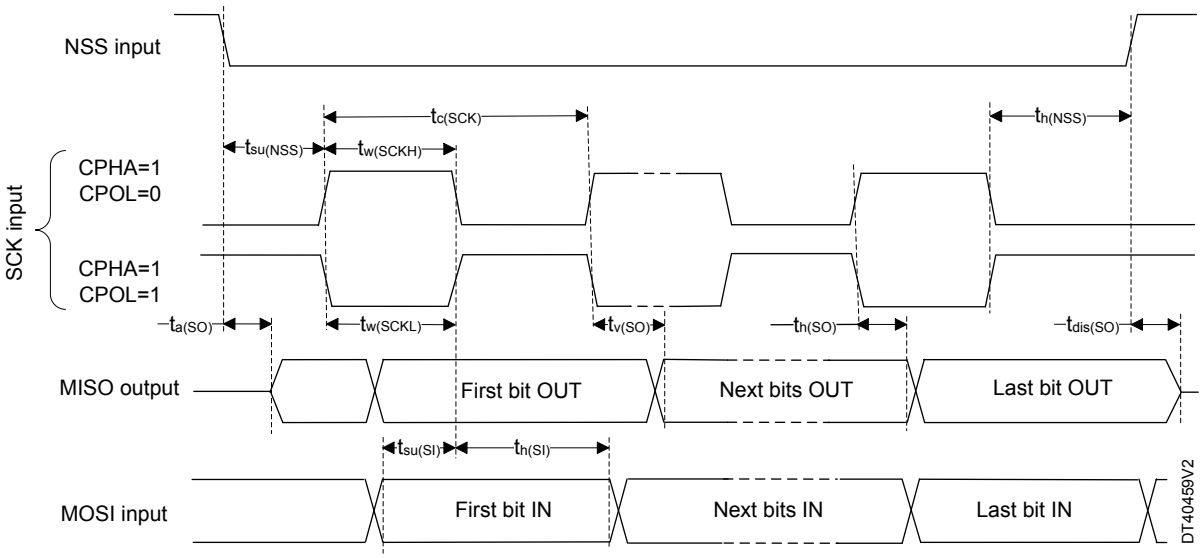
Figure 36. SWD timing diagram



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6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

6.2 TSSOP20 package information (YA)

Figure 37. TSSOP20 - Outline

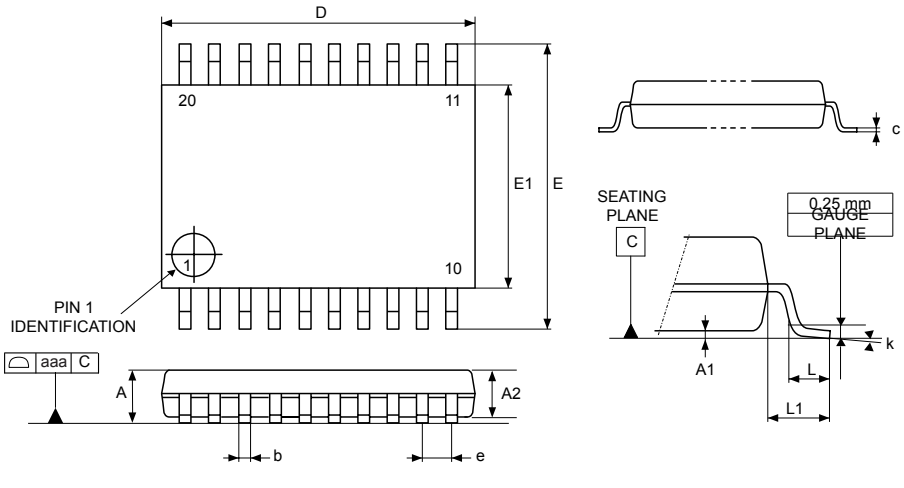

Table 72. TSSOP20 - Mechanical data

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.2	-	-	0.0472
A1	0.05	-	0.15	0.002	-	0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19	-	0.3	0.0075	-	0.0118
c	0.09	-	0.2	0.0035	-	0.0079
D	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e	-	0.65	-	-	0.0256	-
L	0.45	0.6	0.75	0.0177	0.0236	0.0295

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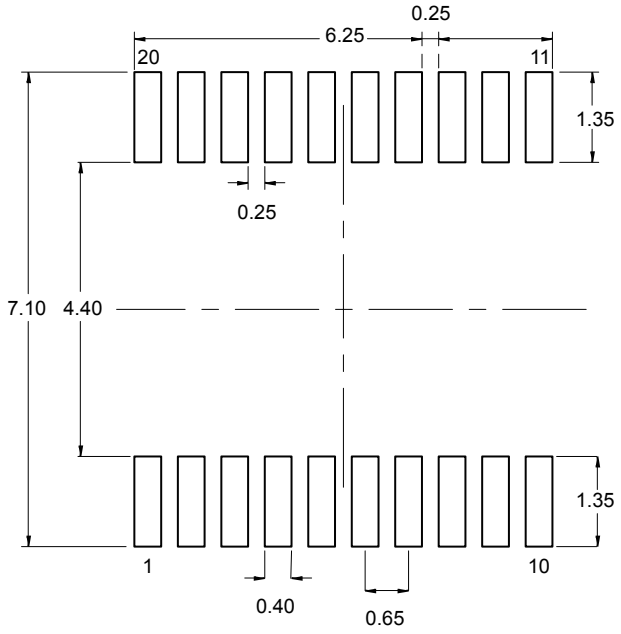
Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
L1	-	1	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.1	-	-	0.0039

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 38. TSSOP20 - Footprint example



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6.3 UFQFPN20 package information (A0A5)

This UFQFPN is a 20-lead, 3 x 3 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Note: Figure 39 is not to scale.
Refer to the notes section for the list of notes on Figure 39 and Table 73.

Figure 39. UFQFPN20 - Outline

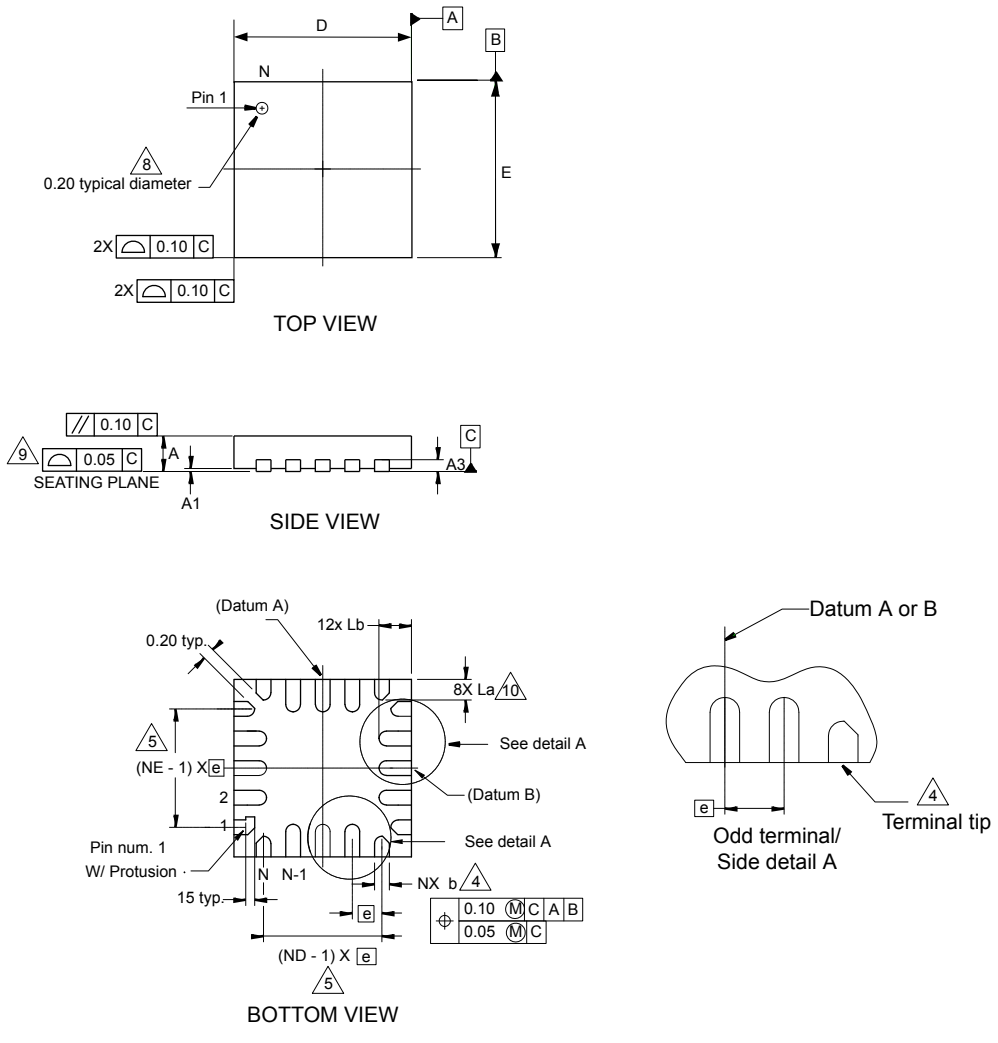

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Table 73. UFQFPN20 - Mechanical data

Symbol	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3		0.152 reference			0.060 reference	
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
θ	0	-	12	0	-	0.0020
e	-	0.500 BSC(11.)	-	-	0.0197 BSC	-
b(4.)	0.180	0.250	0.300	0.0071	0.0098	0.0118
N(3.)		20			20	
ND(5.)		5			5	
NE(5.)		5			5	
La	0.300	0.350	0.400	0.0118	0.0138	0.0157
Lb	0.500	0.550	0.600	0.0197	0.0217	0.0236

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters except for θ, which is in degrees. Values in inches are converted from millimeters and rounded to four decimal digits.
3. N is the total number of terminals.
4. Dimension b applies to the metallized terminal and is measured between 0.15 and 0.30 mm from the terminal tip. If the terminal has an optional radius on the other end, dimension b should not be measured in that radius area.
5. ND and NE refer to the number of terminals on each D and E side, respectively.
6. The maximum package warpage is 0.05 mm.
7. The maximum allowable burrs are 0.076 mm in all directions.
8. Pin number 1 ID on top is laser marked.
9. Bilateral coplanarity zone applies to the terminals.
10. Allow chamfered corner lead.
11. BSC stands for basic dimensions.

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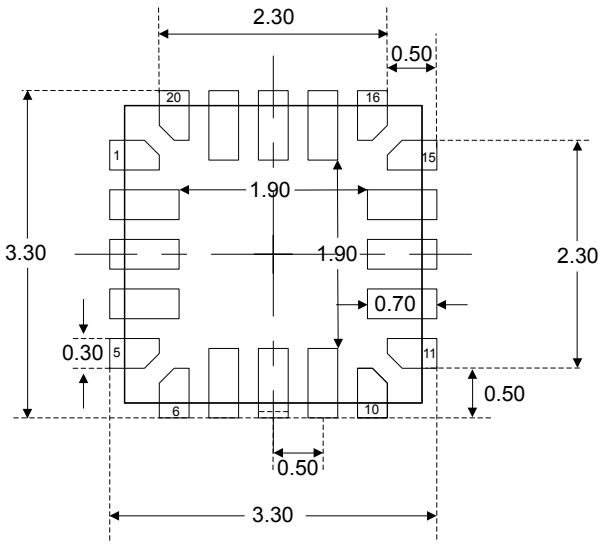
Figure 40. UFQFPN20 - Footprint example



A0A5_UFQFPN20_FP_V1

1. *Dimensions are expressed in millimeters.*

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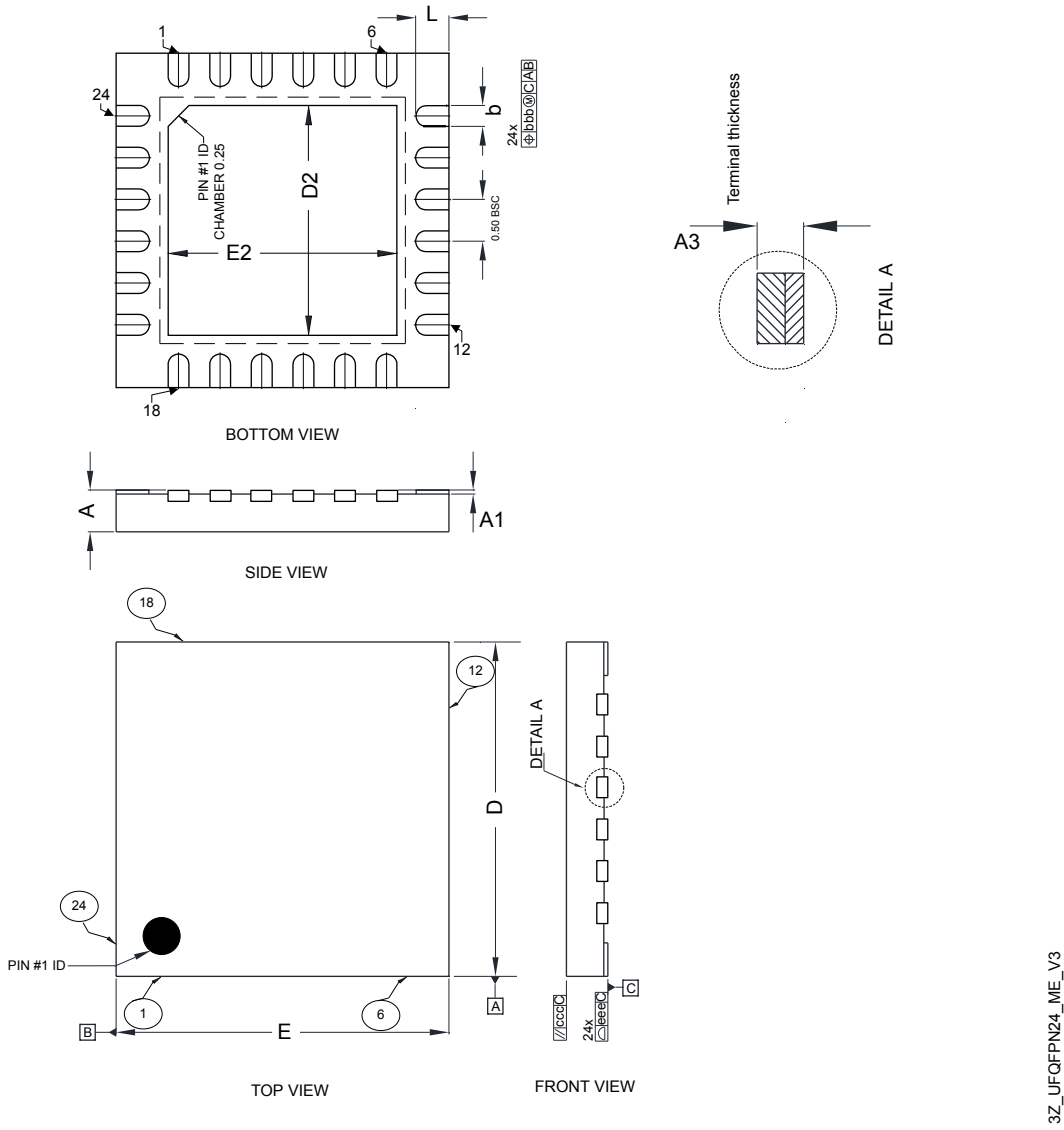
6.4 UFQFPN24 package information (3Z)

This UFQFPN is a 24-pin, 4 x 4 mm, 0.5 mm pitch, thermally enhanced ultra-thin fine pitch quad flat no lead package.

Figure 41. UFQFPN24 - Outline



1. *Drawing is not to scale.*
2. *Coplanarity applies to the exposed pad as well as the terminal.*

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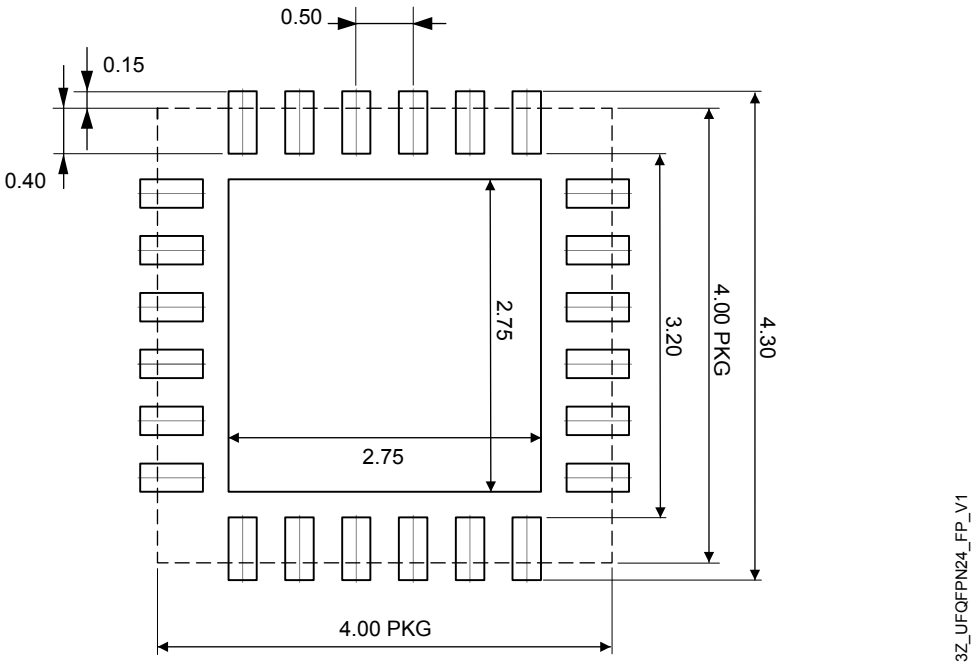
Table 74. UFQFPN24 - Mechanical data

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.45	-	0.60	0.0177	-	0.0236
A1	0	-	0.05	0	-	0.0020
A3[2]	0.152 REF			0.0060 REF		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[3]	4.00 BSC			0.1575 BSC		
E[3]	4.00 BSC			0.1575 BSC		
e[3]	0.50 BSC			0.0197 BSC		
D2	2.60	-	2.85	0.1024	-	0.1122
E2	2.60	-	2.85	0.1024	-	0.1122
bbb	-	0.10	-	-	0.0039	-
ccc	-	0.10	-	-	0.0039	-
eee	-	0.08	-	-	0.0031	-
N[4]	24			24		

1. *Values in inches are converted from mm and rounded to three decimal digits.*
2. *REF stands for reference.*
3. *BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to the form and position table*
4. *Total number of terminals*

Figure 42. UFQFPN24 - Footprint example



1. *Dimensions are expressed in millimeters.*

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6.5 LQFP32 package information (5V)

This LQFP is a 32-pin, 7 x 7 mm, low-profile quad flat package.

Note: *Figure 43 is not to scale.*
Refer to the notes section for the list of notes on Figure 43 and Table 75.

Figure 43. LQFP32- Outline

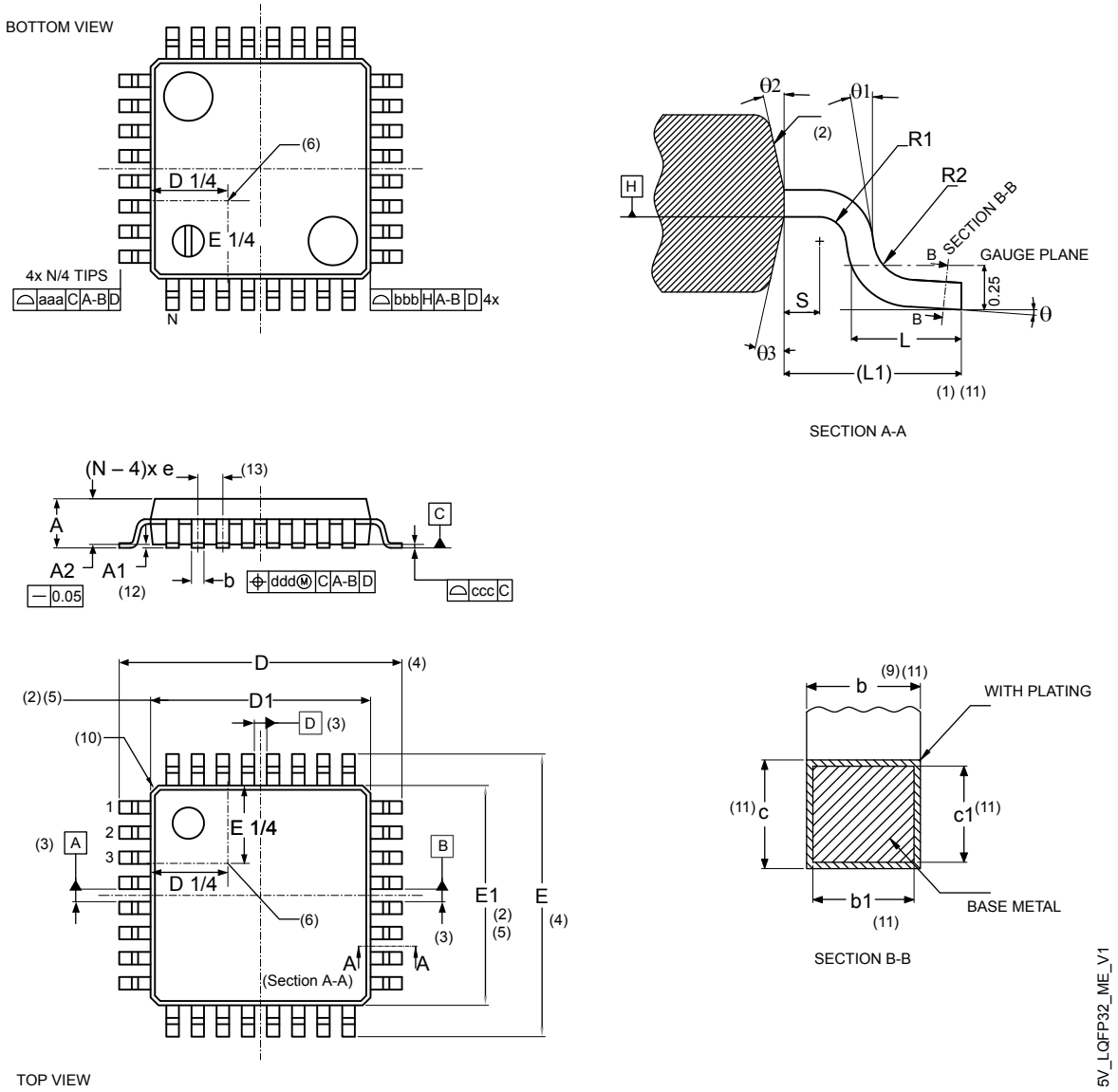

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Table 75. LQFP32 - Mechanical data

Symbol	Millimeters			Inches[14.]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.30	0.37	0.45	0.0118	0.0146	0.0177
b1[11.]	0.30	0.35	0.40	0.0118	0.0128	0.0157
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	9.00 BSC			0.3543 BSC		
D1[2.][5.]	7.00 BSC			0.2756 BSC		
e	0.80 BSC			0.0315 BSC		
E[4.]	9.00 BSC			0.3543 BSC		
E1[2.][5.]	7.00 BSC			0.2756 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	32					
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.][7.][15.]	0.20			0.0079		
bbb[1.][7.][15.]	0.20			0.0079		
ccc[1.][7.][15.]	0.10			0.0039		
ddd[1.][7.][15.]	0.20			0.0079		

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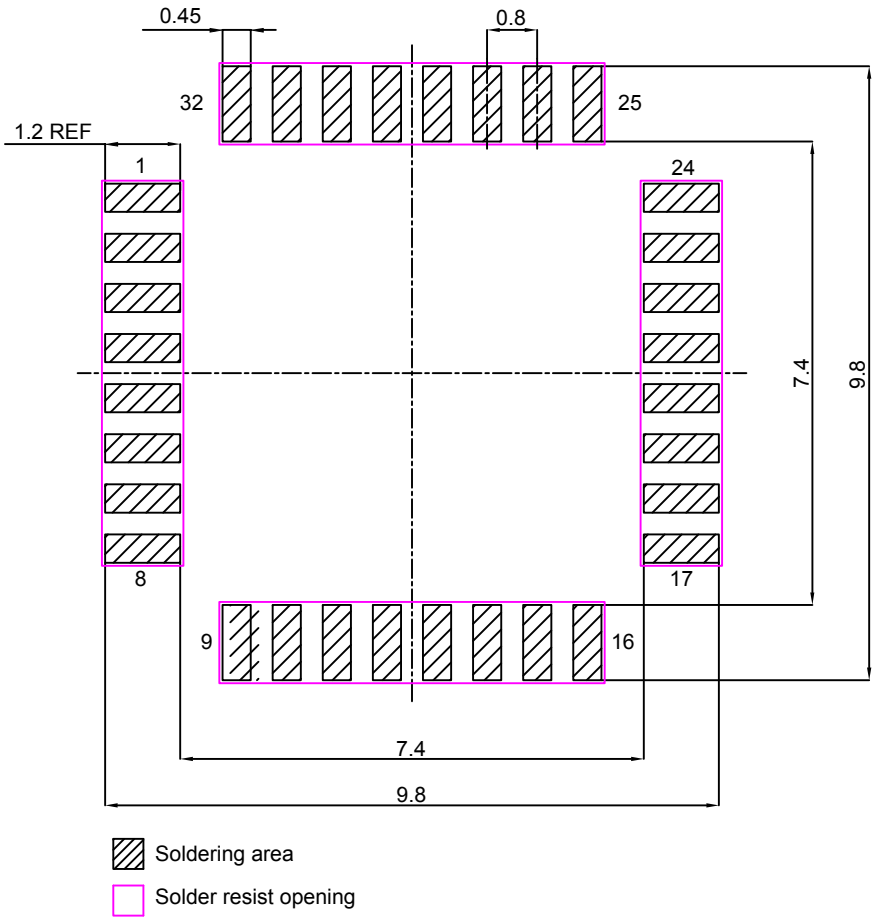
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at the seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion is allowed inwards the leads.
9. Dimension b does not include a dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. N is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to four decimal digits.
15. Recommended values and tolerances.

Figure 44. LQFP32 - Footprint example



1. *Dimensions are expressed in millimeters.*

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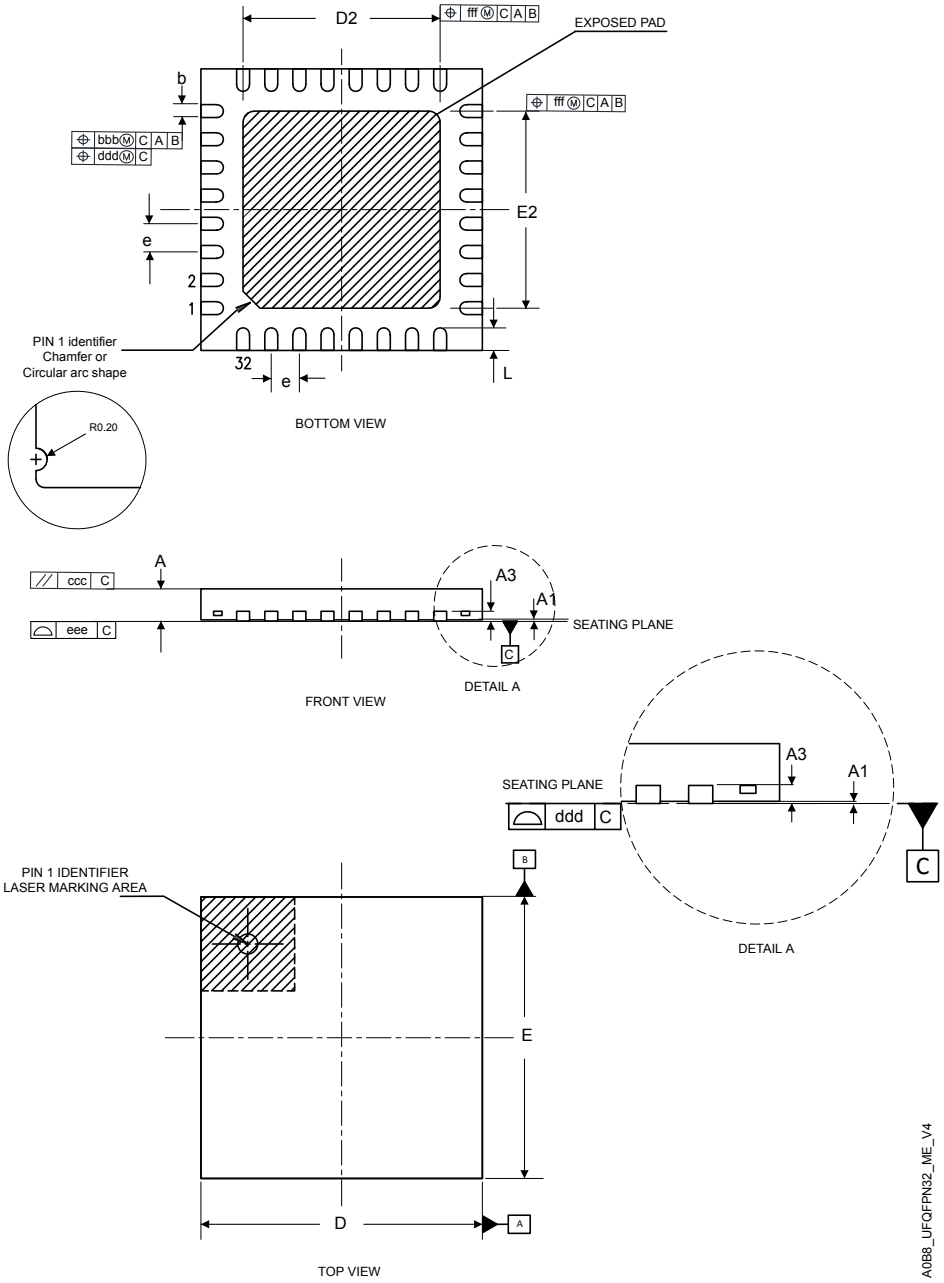
6.6 UFQFPN32 package information (A0B8)

This UFQFPN is a 32-pin, 5 x 5 mm, 0.5 mm pitch ultra-thin fine pitch quad flat package.

Figure 45. UFQFPN32 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.*

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Table 76. UFQFPN32 - Mechanical data

Symbol	Millimeters[1]			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
A[3][4]	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1[5]	0.00	-	0.05	0.000	-	0.0020
A3[6]	-	0.15	-	-	0.0060	-
b[7]	0.18	0.25	0.30	0.0071	0.010	0.0118
D[8][9]	5.00 BSC			0.1969 BSC		
D2	3.50	3.60	3.70	0.139	0.143	0.147
E[8][9]	5.00 BSC			0.1969 BSC		
E2	3.50	3.60	3.70	0.139	0.143	0.147
e[9]	-	0.50	-	-	0.02	-
N[10]	32					
K	0.15	-	-	0.006	-	-
L	0.30	-	0.50	0.0119	-	0.0199
R	0.09	-	-	0.004	-	-

1. *All dimensions are in millimeters. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
2. *Values in inches are converted from mm and rounded to 4 decimal digits.*
3. *UFQFPN stands for Ultra thin Fine pitch Quad Flat Package No lead: A ≤ 0.60mm / Fine pitch e ≤ 1.00mm.*
4. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
5. *A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.*
6. *A3 is the distance from the seating plane to the upper surface of the terminals.*
7. *Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b must not be measured in that radius area.*
8. *Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.*
9. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to Table 77*
10. *N represents the total number of terminals.*

Table 77. Tolerance of form and position

Symbol[1]	Tolerance of form and position[2] In millimeters	Tolerance of form and position[3] In inches
aaa	0.15	0.006
bbb	0.10	0.004
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.10	0.004
fff	0.10	0.004

1. *For the tolerance of form and position definitions see Table 78.*
2. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
3. *Values in inches are converted from mm and rounded to 4 decimal digits.*

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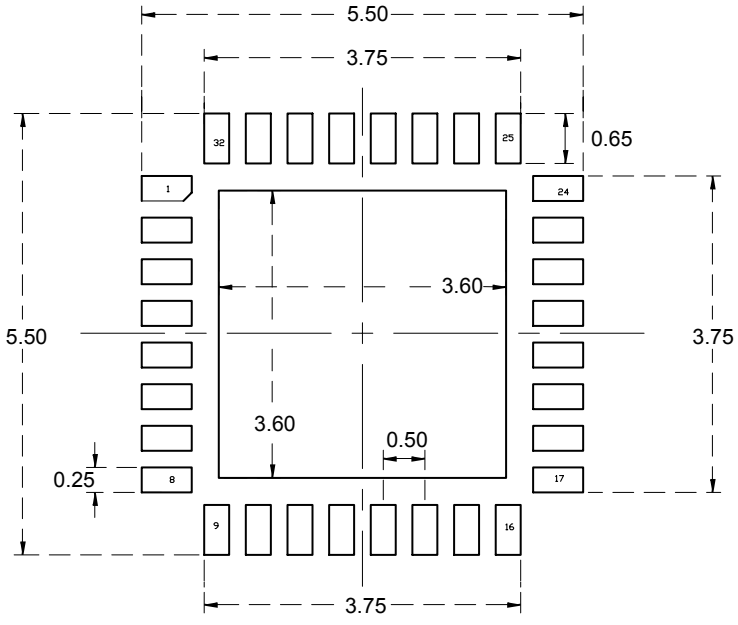
Table 78. Tolerance of form and position symbol definition

Symbol	Definition
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centres of the profile zones are defined by the basic dimensions D and E.
bbb	The tolerance that controls the position of the terminals with respect to Datums A and B. The centre of the tolerance zone for each terminal is defined by basic dimension e as related to datums A and B.
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.
ddd	The tolerance that controls the position of the terminals to each other. The centres of the profile zones are defined by basic dimension e.
eee	The unilateral tolerance located above the seating plane wherein the bottom surface of all terminals must be located = coplanarity
fff	The tolerance that controls the position of the exposed metal heat feature. The centre of the tolerance zone is the data defined by the centrelines of the package body

Figure 46. UFQFPN32 - Footprint example



1. *Dimensions are expressed in millimeters.*

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6.7 LQFP48 package information (5B)

This LQFP is a 48-pins, 7 x 7 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 47. LQFP48- Outline(15.)

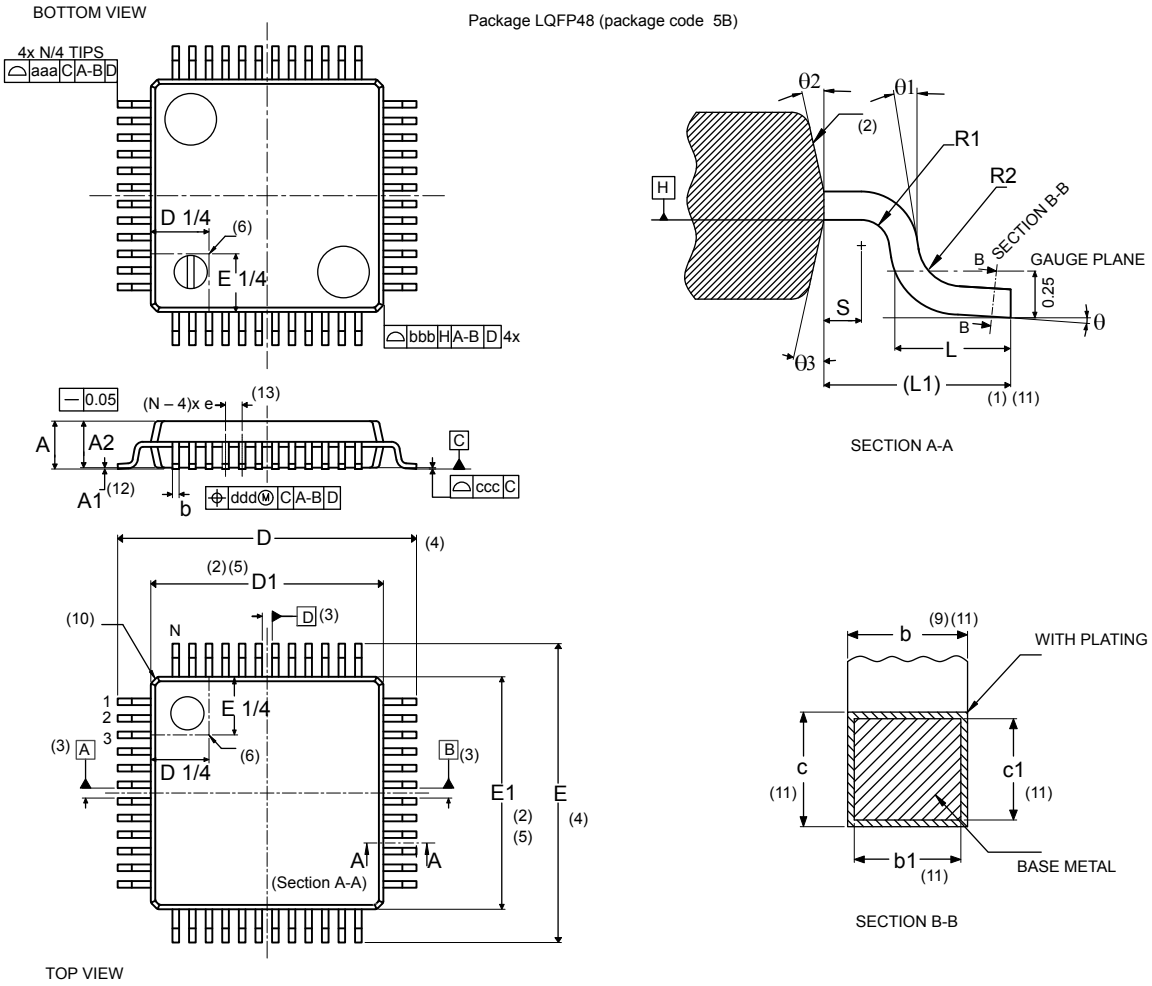

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Table 79. **LQFP48 - Mechanical data**

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	9.00 BSC			0.3543 BSC		
D1[4.][5.]	7.00 BSC			0.2756 BSC		
E[4.]	9.00 BSC			0.3543 BSC		
E1[4.][5.]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.][7.]	0.20			0.0079		
bbb[1.][7.]	0.20			0.0079		
ccc[1.][7.]	0.08			0.0031		
ddd[1.][7.]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

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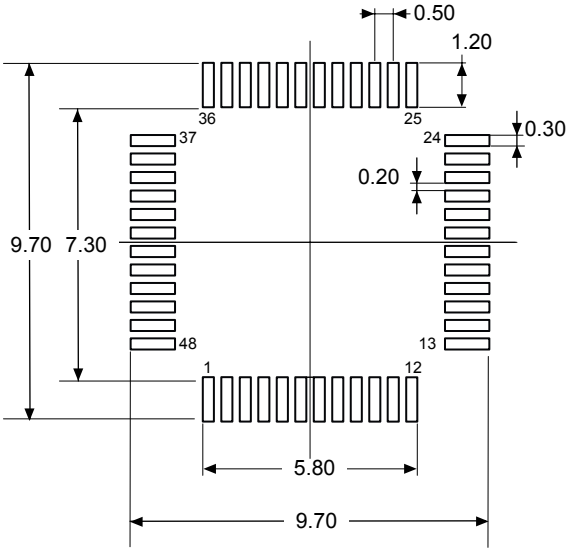
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits
15. Drawing is not to scale.

Figure 48. LQFP48 - Footprint example



1. Dimensions are expressed in millimeters.

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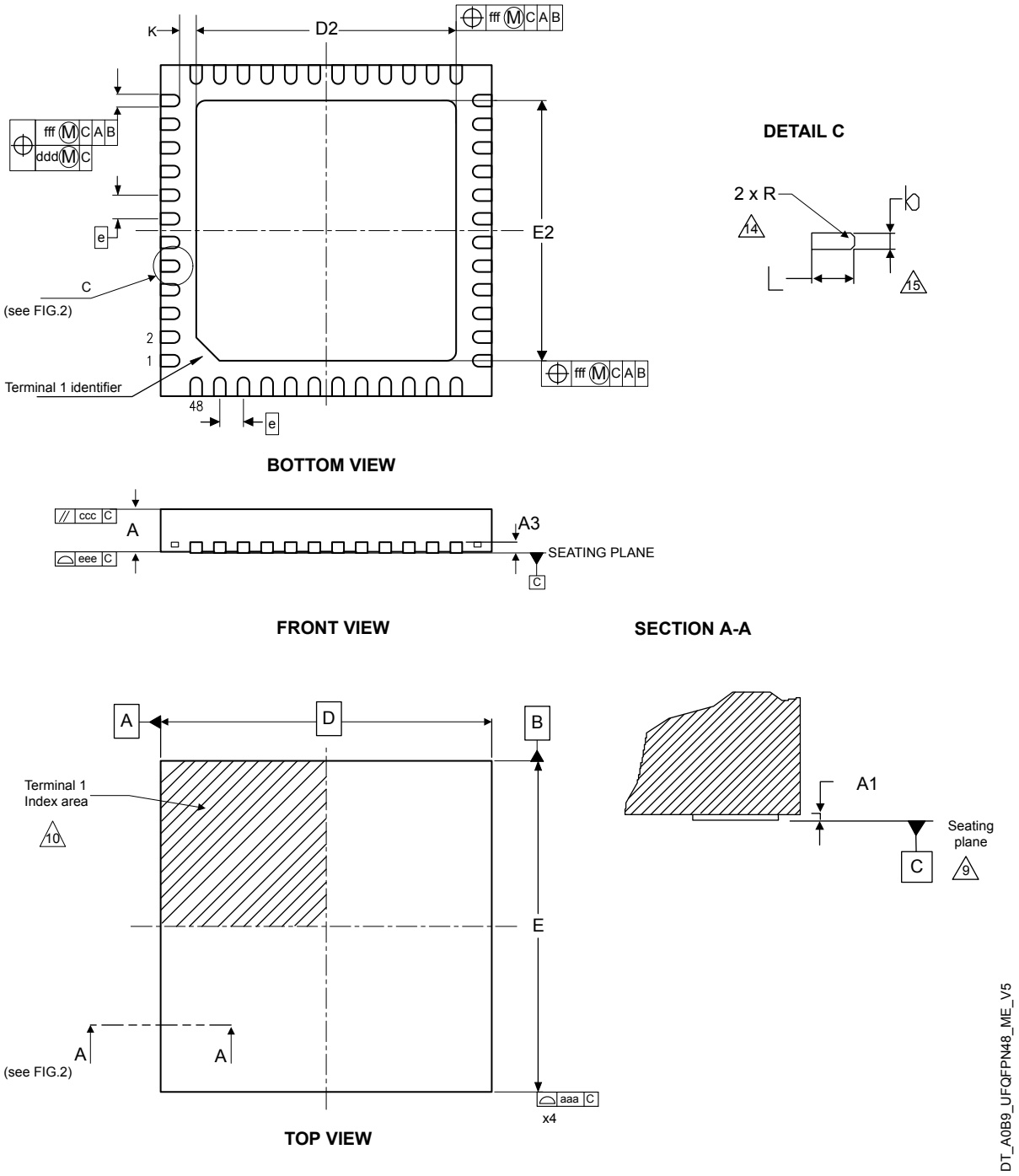
6.8 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 49. UFQFPN48 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the under side of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.*

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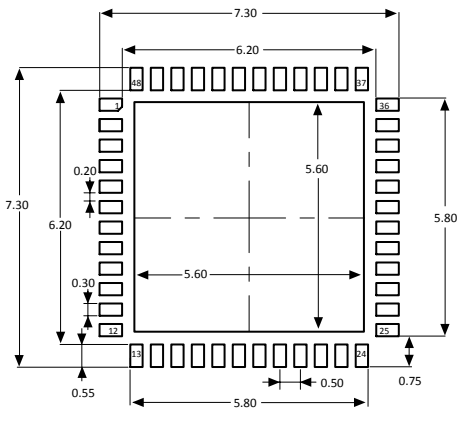
Table 80. UFQFPN48 - Mechanical data

Symbol	Millimeters			Inches [1]		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.0000	-	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[2]	7.00 BSC			0.2756 BSC		
D2[3]	5.50	5.60	5.70	0.2165	0.2205	0.2244
E[2]	7.00 BSC			0.2756 BSC		
E2[3]	5.50	5.60	5.70	0.2165	0.2205	0.2244
e	0.50 BSC			0.0197 BSC		
N	48					
L	0.30	-	0.50	0.0118	-	0.0197
R	0.10	-	-	0.0039	-	-
aaa	0.15			0.0059		
bbb	0.10			0.0039		
ccc	0.10			0.0039		
ddd	0.05			0.0020		
eee	0.08			0.0031		
fff	0.10			0.0039		

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.*
3. *Dimensions D2 and E2 are not in accordance with JEDEC.*

Figure 50. UFQFPN48 - Footprint example



1. *Dimensions are expressed in millimeters.*

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6.9 LQFP64 package information (5W)

This is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 51. LQFP64 - Outline[15.]

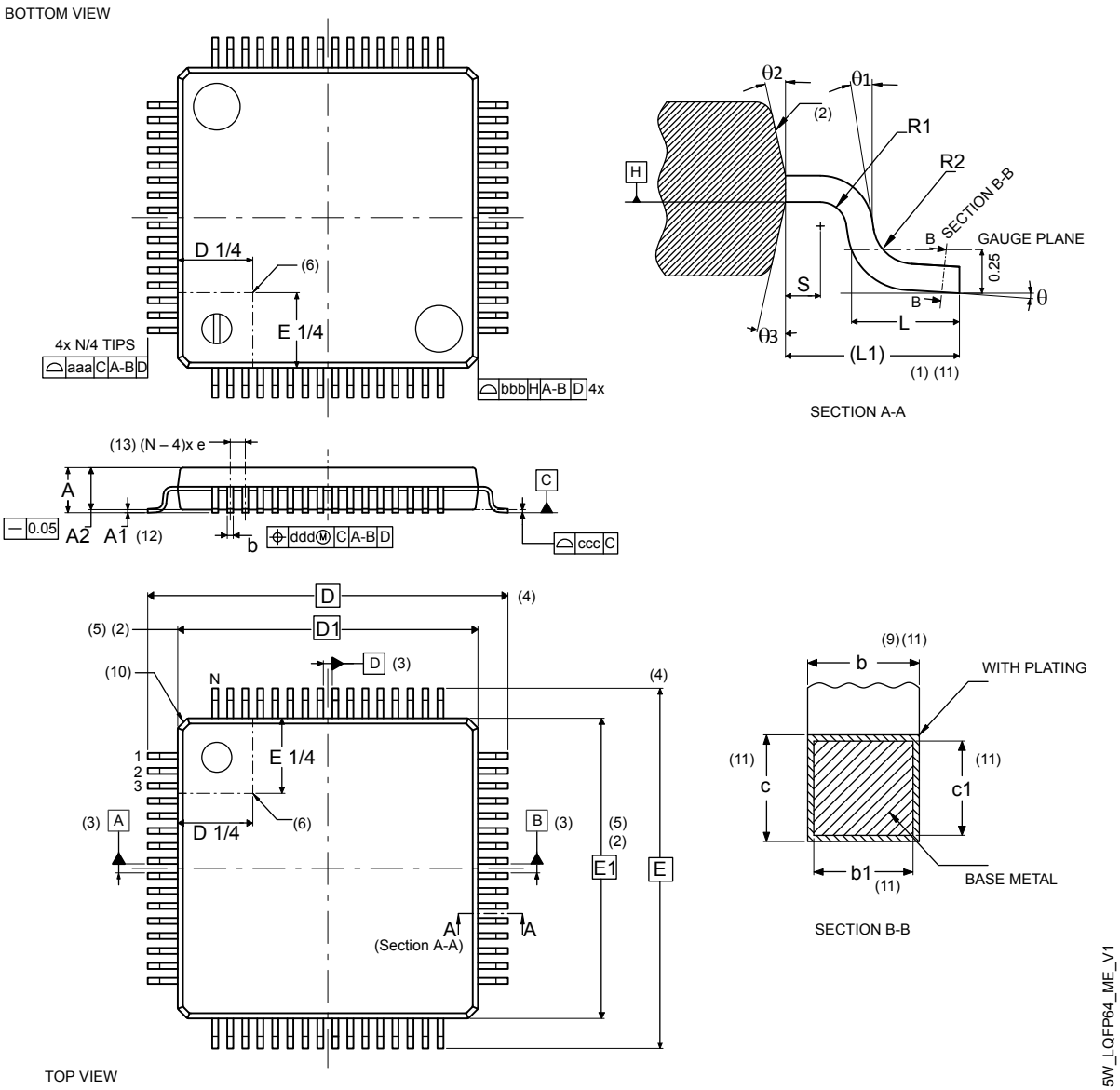

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Table 81. LQFP64 - Mechanical data

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	00067	0.0079	0.0091
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	12.00 BSC			0.4724 BSC		
D1[2.][5.]	10.00 BSC			0.3937 BSC		
E[4.]	12.00 BSC			0.4724 BSC		
E1[2.][5.]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	64					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

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Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. N is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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6.10 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

Where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max)$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \max = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right)\right) \times I_{OH}$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 82. Package thermal characteristics

Symbol	Definition	Parameter	Value			Unit
			Junction-ambient Θ_{JA}	Junction-board Θ_{JB}	Junction-case Θ_{JC}	
Θ	Thermal Resistance	LQFP64	45.3	27.6	14.2	°C/W
		LQFP48	52.3	29.7	16.9	
		LQFP32	52.3	29.7	16.9	
		UFQFPN48	31.4	15.6	11.4	
		UFQFPN32	43.3	25.2	18.8	
		UFQFPN24	47.5	27.4	25.8	
		UFQFPN20	64.3	21.7	33.9	
		TSSOP20	78.9	52.4	28.4	

6.10.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

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7 Ordering information

Example:	STM32	C	542	K	C	T	6	TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

C = General purpose

Device subfamily

542 = Product with FDCAN

Pin count

F = 20 pins

E = 24 pins

K = 32 pins

C = 48 pins

R = 64 pins

Flash memory size

C = 256 Kbytes

Package

U = UFQFPN

T = LQFP

P = TSSOP

Temperature range

6 = Temperature range, -40 to +85°C (+105°C junction)

3 = Temperature range, -40 to +125°C (+140°C junction)

Packing

TR = Tape and reel

xxx = Programmed parts

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 83. **Document revision history**

Date	Revision	Changes
26-Feb-2026	1	Initial release.
31-Jul-2026	2	Updated: • Section 2: Description • Table 9. USART, UART, and LPUART features • Table 44. ESD absolute maximum ratings • Table 55. Temperature sensor characteristics • Table 57. DAC characteristics • Table 60. OPAMP characteristics

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