REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update absolute maximum supply voltage(Vcc), Input and output voltage (Vin,Vout) to section 1.3. Update low level output voltage(Vol) maximum level at IOL=2mA and propagation delay tphl, tplh test conditions table IA. - LTG	18-09-24	Thomas M. Hess

REV																				
SHEET																				
REV	A	A	A	A	A	A	A													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Muhammad Akbar

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
18-06-27

REVISION LEVEL
A

MICROCIRCUIT, DIGITAL, QUAD HIGH SPEED NAND GATE, MONOLITHIC SILICON

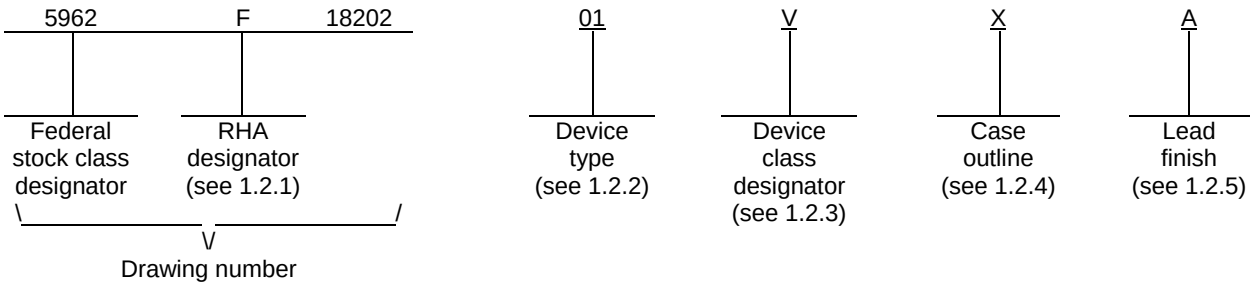
SIZE	CAGE CODE	
A	**67268**	**5962-18202**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AHC00	Rad hard, Quad high speed NAND gate

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP3	14	Flat pack 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Package case outline X flat pack with grounded lid.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.3 V dc to 4.8 V dc
DC input voltage range (V_{IN}) ..... -0.3 V dc to V_{CC} + 0.3 V dc (4.8 V max)
DC output voltage range (V_{OUT})..... -0.3 V dc to V_{CC} + 0.3 V dc (4.8 V max)
Max input current of any pin ..... ±10 mA
DC output current (per pin) (I_{OUT}) ..... ±50 mA
Maximum power dissipation (P_D)..... 1 W
Storage temperature range (T_{STG})..... -65°C to +150°C
Lead temperature (soldering, 10 seconds)..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 22°C/W
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 125°C/W
Junction temperature (T_J)..... +150°C 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}): ..... +1.65 V dc to +3.6 V dc
Input voltage range (V_{IN})..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT})..... +0.0 V dc to V_{CC}
Input rise or fall time rate ($\Delta t/\Delta V$):
V_{CC} = 3.0 V ..... 0 to 10 ns/V
Case operating temperature range (T_C)..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 0.086 Rad(Si)/s): ..... 300 krad(Si) 5/
Maximum total dose available (dose rate = 50 Rad(Si)/s): ..... 300 krad(Si) 5/
Single Event Effects (SEE) for device type 01:
No Single Event Latch-up (SEL) occurs at effective LET (see 4.4.4.2)..... ≤ 125 MeV-cm^2/mg 6/
No Single Event Transient (SET) occurs at effective LET (see 4.4.4.2)..... < 62.5 MeV-cm^2/mg 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ Device type 01 is irradiated at dose rate = 0.086 Rad (Si)/s in accordance with MIL-STD-883, method 1019, condition B, as agreed by the parties intended application, and are guaranteed to the maximum total dose specified herein. Manufacturer also performed high dose rate = 50 Rad (Si)/s irradiation in accordance with MIL-STD-883, method 1019, condition A.

6/ Manufacturer performed heavy ion single event effects (SEE) test at U.C.L. Heavy Ion Test Facility (Université Catholique de Louvain - Belgium) with Xenon (Xe) ion beam and observed no SEL occurs at effective LET ≤ 125 MeV/(mg/cm^2). No SET observed with a LET < 62.5 MeV.cm^2/mg. For more information on SEE test, contact manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The Switching waveforms and test circuit shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+1.8\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified		Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
							Min	Max	
High level output voltage 3006	V_{OH}	$V_{IN} = V_{CC}$ or 0.0 V	I_{OH} = -100 µA	All	1.65 V	1, 2, 3	1.45		V
				All	2.3 V	1, 2, 3	2.1		
					3.0 V	1, 2, 3	2.8		
			I_{OH} = -2 mA	All	1.65 V	1, 2, 3	1.2		
				All	2.3 V	1, 2, 3	1.7		
					3.0 V	1, 2, 3	2.4		
Low level output voltage 3007	V_{OL}	$V_{IN} = V_{CC}$ or 0.0 V	I_{OL} = +100 µA	All	1.65 V	1, 2, 3		0.2	V
				All	2.3 V	1, 2, 3		0.2	
					3.0 V	1, 2, 3		0.2	
			I_{OL} = +2 mA	All	1.65 V	1, 2, 3		0.450	
				All	2.3 V	1, 2, 3		0.430	
					3.0 V	1, 2, 3		0.400	
High level input voltage	V_{IH} 5/			All	1.65 V	1, 2, 3	1.0		V
				All	2.3 V	1, 2, 3	1.7		
					3.0 V	1, 2, 3	2.0		
Low level input voltage	V_{IL} 5/			All	1.65 V	1, 2, 3		0.5	V
				All	2.3 V	1, 2, 3		0.7	
					3.0 V	1, 2, 3		0.8	
Input leakage current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ All other inputs are disconnected		All	1.8 V	1, 2, 3		0.1	µA
				All	2.5 V	1, 2, 3		0.1	
					3.3 V	1, 2, 3		0.1	
Input leakage current low 3009	I_{IL}	For input under test, V_{IN} = GND All other inputs are disconnected		All	1.8 V	1, 2, 3		-0.1	µA
				All	2.5 V	1, 2, 3		-0.1	
					3.3 V	1, 2, 3		-0.1	
Quiescent supply current, output high 3005	I_{CCH}	V_{IN} = GND		All	3.3 V	1, 2, 3		50	µA
				All					
Quiescent supply current, output low 3005	I_{CCL}	$V_{IN} = V_{CC}$		All	3.3 V	1, 2, 3		50	µA
				All					
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		All	GND	4		2.0	pF
				All					
Power dissipation capacitance	C_{PD} 6/	See 4.4.1c T_C = +25°C, f = 1 MHz		All	3.3 V	4		7	pF
				All	1.8 V	4		5	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+1.8\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Functional tests 3014	7/	$V_{IN} = V_{CC}$ or 0V Verify output V_{OUT} f = 150 MHz See 4.4.1b	All All	1.8 V	7, 8	L	H	
				2.3 V	7, 8	L	H	
				3.6 V	7, 8	L	H	
	7/	$V_{IN} = V_{ILmax}$ or V_{IHmin} f = 25 MHz	All All	1.8 V	7, 8	L	H	
				2.3 V	7, 8	L	H	
				3.6 V	7, 8	L	H	
Propagation delay time, mAn or mBn to mYn 3003	t_{PHL}, t_{PLH}	C_L = 10 pF See figure 6	All All	1.8 V	9, 10, 11	1.5	5.5	ns
				2.5 V	9, 10, 11	1.2	3.5	
				3.3 V	9, 10, 11	1.0	3.0	

1/ For tests not listed in the referenced MIL-STD-883, [e.g. V_{IH}, V_{IL}], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

3/ RHA device type 01 supplied to this drawing have been characterized through all levels M, D, P, L, R and F of irradiation. However, device type 01 is only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level T_A = +25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $1.8\ V \le V_{CC} \le 3.6\ V$.

5/ V_{IH} and V_{IL} are not required if applied as forcing inputs during 25 MHz functional test.

6/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$P_D = (C_{PD} + C_L)\ (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L)\ V_{CC}f + I_{CC}$

f is the frequency of the input signal; and C_L is the external output load capacitance.

7/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For outputs, $L \le V_{IL}$ maximum, $H \ge V_{IH}$ minimum.

TABLE IB. SEP test limits. 1/ 2/ 3/ 4/

Device types	V_{CC} = 1.8 and 3.6 V Effective LET No SET observed	Bias V_{CC} = 3.6 V For single event latch-up (SEL) test no SEL occurs at effective LET
01	LET < 62.5 MeV/(mg/cm^2)	LET ≤ 125 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature is T_A = +125°C ± 10°C for SEL and T_A = +25°C ± 10°C for SET
4/ Manufacturer performed heavy ion single event effects (SEE) test at U.C.L. Heavy Ion Test Facility (Université Catholique de Louvain - Belgium) with Xenon (Xe) ion beam and observed no SEL occurs at effective LET ≤ 125 MeV/(mg/cm^2). No SET observed with an effective LET < 62.5 MeV.cm^2/mg. For more information on SEE test, contact manufacturer.

Device type	All
Case outline	X
Terminal number	Terminal symbol
1	1A
2	1B
3	1Y
4	2A
5	2B
6	2Y
7	GND
8	3Y
9	3A
10	3B
11	4Y
12	4A
13	4B
14	V_{CC}

FIGURE 1. Terminal connections.

Inputs		Outputs
mA	mB	mY
L	L	H
H	L	H
L	H	H
H	H	L

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

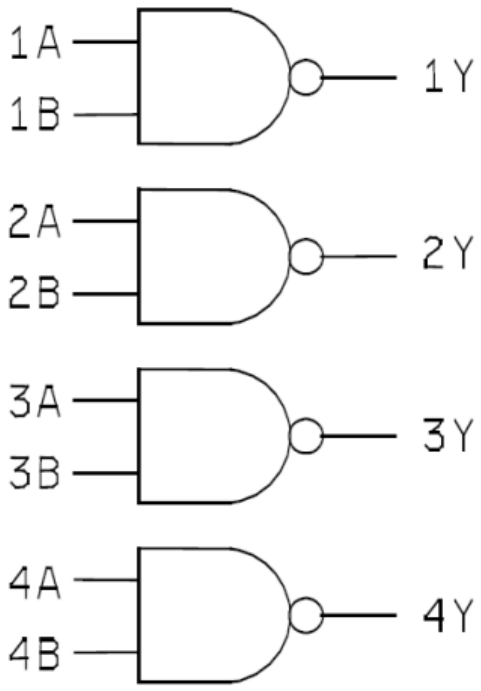
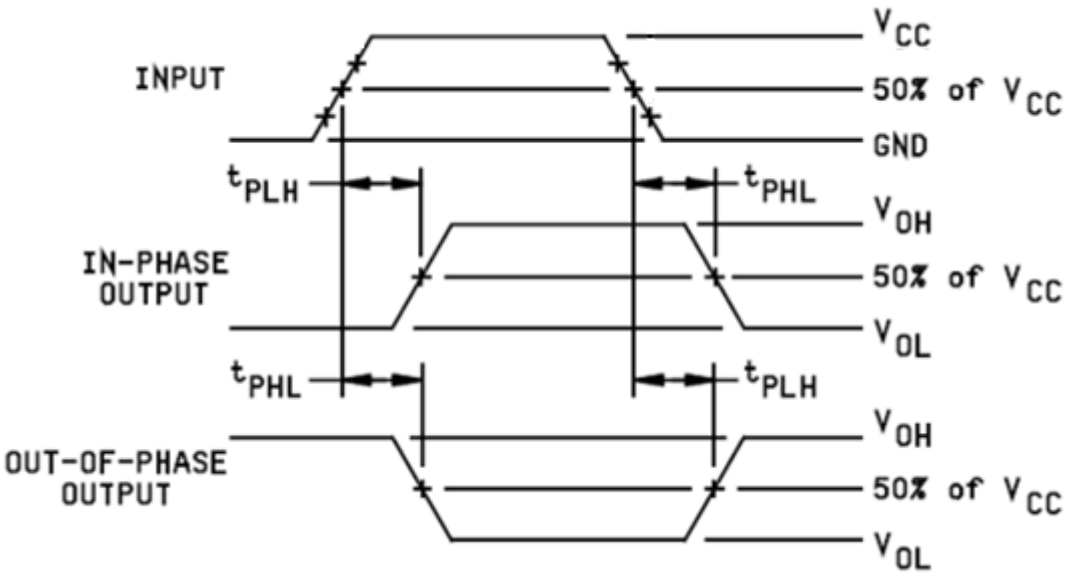
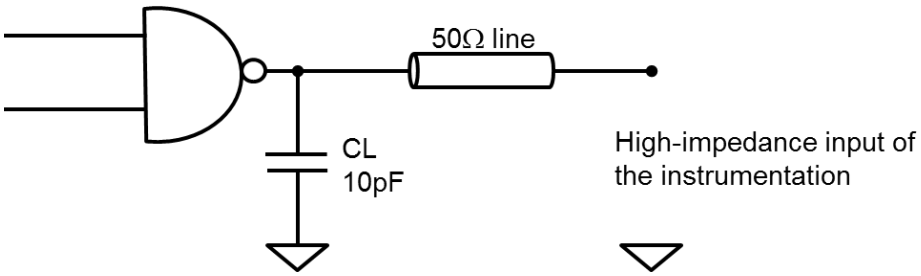


FIGURE 3. Logic diagram.





NOTES:
1. CL = 10 pF or equivalent (includes probe and jig capacitance).
2. Timing parameters shall be tested at a minimum input frequency of 1MHz.
3. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Dynamic burn-in (Method 1015)	Required	Required
Post burn-in interim electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Final electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 7,8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test Delta parameters (+25°C). 1/

Parameter 2/	Symbol	Delta Limits
Quiescent supply current	I_{CCH}, I_{CCL}	±100 nA
Output voltage low level (V_{CC} = 3.0 V, I_{OL} = +2 mA)	V_{OL}	±0.02 V
Output voltage high level (V_{CC} = 3.0 V, I_{OH} = -2 mA)	V_{OH}	±0.1 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition B and condition A and as specified herein 1.5.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K Rad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature shall be the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 General applications: The manufacturer is supplying this SMD device as a high-speed pure CMOS technology radiation hardened, quad 2 input NAND gate. This device can be used in many applications/systems but general applications are Oscillators in space applications, FPGA and microcontroller.

6.1.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions of SEP.

b. Number of transients (SET).

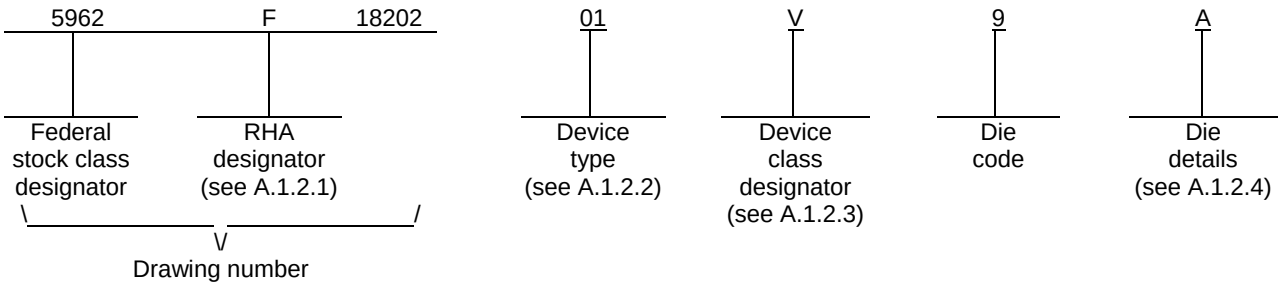
c. Occurrence of latch-up (SEL).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:

For device class V:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AHC00	Quad high speed NAND gate

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

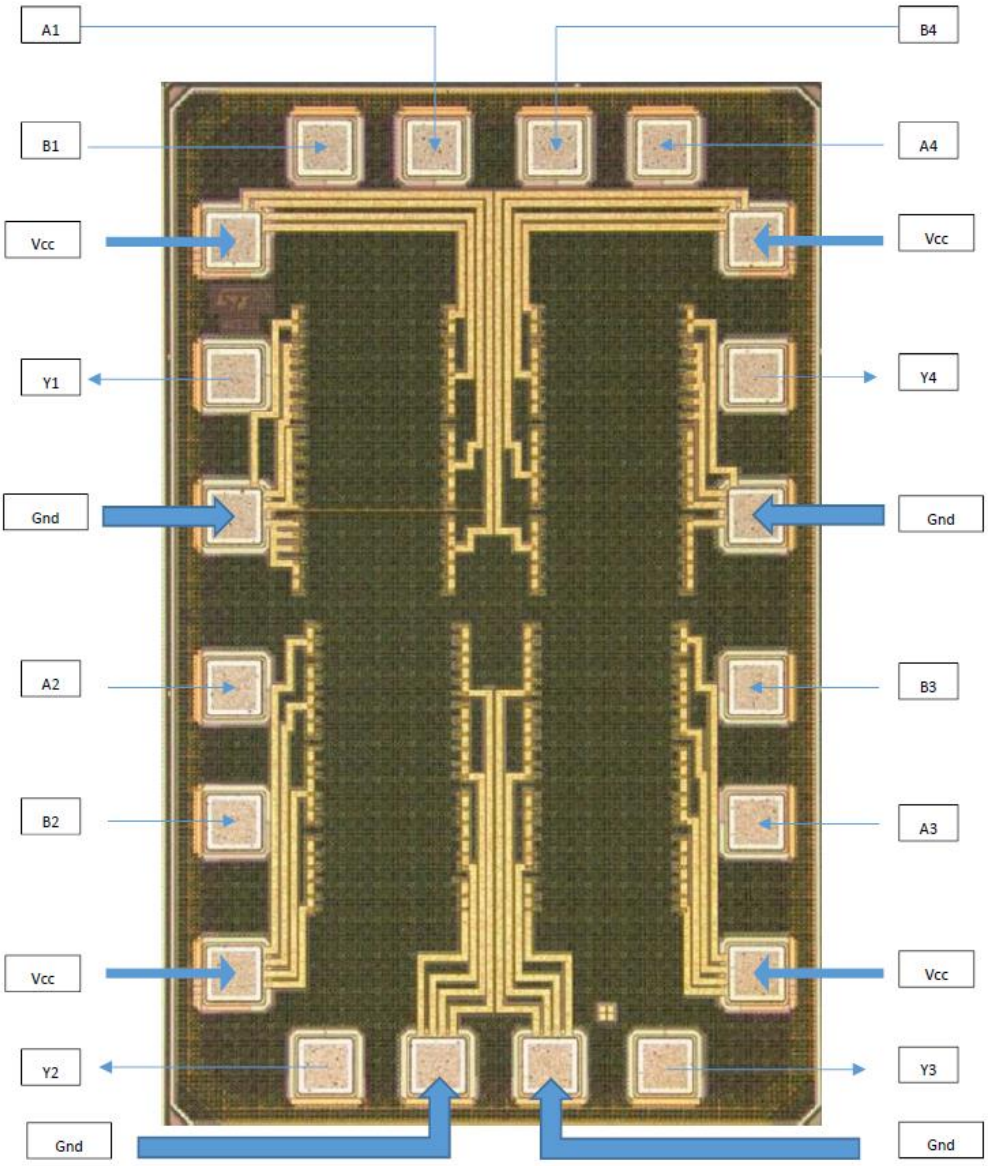
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, P.O. Box 3990, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA, and have agreed to this drawing.

APPENDIX A FORMS A PART OF SMD 5962-18202



Pad size: All pads are 99.8 x 99.8 μm

NOTE:
1. Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).
2. All VCC's pads have to be connected to the same voltage level.
3. All GND's pads have to be connected to the same voltage level.

FIGURE A-1.. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	1990 x 1280 μm
Die thickness:	280 ±25 μm

Interface materials.

Top metallization:	AlCu (TOP)
Thickness:	1.2 μm
Backside metallization:	None

Glassivation.

Type:	PSG/Nitride(SiN)
Thickness:	5000 Å / 6000Å
Substrate:	Silicon

Assembly related information.

Substrate potential:	V_{SS}/GND
Special assembly instructions:	None

FIGURE A-1.. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-09-24

Approved sources of supply for SMD 5962-18202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1820201VXA	F8859	RHFAHC00K02V
5962F1820201VXC	F8859	RHFAHC00K01V
5962F1820201V9A	F8859	RHFAHC00D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.