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Colibri iMX6ULL

Datasheet



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Revision History

Date	Doc. Rev.	Colibri iMX6ULL Version	Changes
05-May-2017	Rev. 0.9	V1.0	Initial Release
01-Dec-2017	Rev. 1.0	V1.0	Add front picture Section 1.2.2: Adding flash endurance remark Section 4.1: Update figure 3 Section 5.4: Correction of Wi-Fi antenna connector type Section 7: Update figure 8 Section 9.5: Remove DVFS feature Minor changes and corrections
13-Mar-2018	Rev. 1.1	V1.0	Section 5.4: Add Wi-Fi and Bluetooth certification information
14-May-2018	Rev. 1.2	V1.0	Section 1.2 Add Colibri iMX6ULL 512MB IT and Colibri iMX6ULL WB Section 9 Add Colibri iMX6ULL 512MB IT and Colibri iMX6ULL WB Section 9.2 Add typical power consumption Minor changes and corrections
02-Jul-2018	Rev. 1.3	V1.1	Update Wi-Fi module to the Azurewave AW-CM276NF Section 3: Update connection to Wi-Fi module Section 3: Add information to SNVS pins Section 5.1: Add information to switching VCC_BATT in power up Section 5.4: Update Wi-Fi module information Section 6.2: Add information to SNVS pin behavior Section 9.5 Increase storage temperature on modules with Wi-Fi
09-May-2019	Rev. 1.4	V1.1	Updated Bluetooth version to 5.0. Section 2: Added comment about additional interfaces
19-Jun-2019	Rev. 1.5	V1.1	Updated product picture Section 1.4.4: Updated link to Azurewave website
12-Oct-2021	Rev. 1.6	V1.1	Section 1.2: Adding Colibri iMX6ULL 1GB IT version Section 1.3: Updates for Colibri iMX6ULL 1GB IT version Section 2: Splitting up in different SKU Block diagrams Section 3: Add extra pins of Colibri iMX6ULL 1GB IT Section 4.4: Update function list for Colibri iMX6ULL 1GB IT Section 5.13: Update for Colibri iMX6ULL 1GB IT Section 9.2: Rename section and remove power consumption tables Section 9.3: New section added for power consumption Section 9.5: Insert table for Colibri iMX6ULL 1GB IT Minor changes and corrections

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1. Introduction

1.1 Hardware

The Colibri iMX6ULL is a computer module based on the NXP®/Freescale i.MX 6ULL embedded System on Chip (SoC). The SoC features a single-core ARM® Cortex®-A7 processor. The i.MX 6ULL SoC is part of the i.MX 6 family. It differentiates itself by the extremely low power consumption.

The Colibri iMX6ULL is also available as a version with a Dual-Band (2.4/5 GHz) Wi-Fi ac/a/b/g/n and Bluetooth v5.0/BLE interface. The Wi-Fi module features an MHF4 compatible connector for an external antenna. The module is pre-certified for FCC (US), CE (Europa), and IC (Canada).

The module targets a wide range of applications, including medical devices, navigation, industrial automation, HMIs, avionics, POS, data acquisition, robotics, and much more.

It offers a wide range of interfaces from simple GPIOs, industry-standard I2C, SPI, CAN, and UART buses to high-speed USB 2.0 interfaces. The Colibri iMX6ULL module features a Fast Ethernet PHY with IEEE1588 timestamping on the module. Additionally, the module allows connecting an additional Ethernet PHY on the customer carrier board by using the RMII interface.

The Colibri iMX6ULL module encapsulates the complexity of modern-day electronic design, such as high-speed impedance controlled layouts with high component density utilizing blind via technology. This allows the customer to create a simple carrier board, which provides his application-specific electronics. The module is compatible with a wide range of other computer modules within the Colibri family. This allows the customer to scale their product without building different carrier boards for each project.

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1.2 Main Features

1.2.1 CPU

	Colibri iMX6ULL 1GB IT	Colibri iMX6ULL 512MB WB IT	Colibri iMX6ULL 512MB WB	Colibri iMX6ULL 512MB IT	Colibri iMX6ULL 256MB
NXP SoC	MCIMX6Y2CVM08AB	MCIMX6Y2CVM08AB	MCIMX6Y2DVM09AB	MCIMX6Y2CVM08AB	MCIMX6Y2DVM05AB
SoC Family	i.MX 6ULL	i.MX 6ULL	i.MX 6ULL	i.MX 6ULL	i.MX 6ULL
ARM Cortex-A7 CPU Cores	1	1	1	1	1
L1 Instruction Cache (each core)	32KByte	32KByte	32KByte	32KByte	32KByte
L1 Data Cache (each core)	32KByte	32Kbyte	32KByte	32KByte	32KByte
L2 Cache (shared by A7 cores)	128KByte	128KByte	128KByte	128KByte	128KByte
NEON MPE	✓	✓	✓	✓	✓
Maximum CPU frequency	800MHz	800MHz	900MHz	800MHz	528MHz
ARM TrustZone	✓	✓	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓	✓	✓
Secure JTAG Controller	✓	✓	✓	✓	✓

1.2.2 Memory

	Colibri iMX6ULL 1GB IT	Colibri iMX6ULL 512MB WB IT	Colibri iMX6ULL 512MB WB	Colibri iMX6ULL 512MB IT	Colibri iMX6ULL 256MB
DDR3L RAM Size	1GByte	512MByte	512MByte	512MByte	256MByte
DDR3L RAM Speed	800MT/s	800MT/s	800MT/s	800MT/s	800MT/s
DDR3L RAM Memory Width	16-bit	16-bit	16-bit	16-bit	16-bit
SLC NAND Flash (8-bit)[1)]		512MByte	512MByte	512MByte	512MByte[3)]
eMMC Flash (8-bit) V5.0 [1) 2)]	4GByte				

[1)]As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear-leveling algorithm makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.
[2)]The eMMC used on the Colibri iMX6ULL 1GB IT is based on MLC NAND flash memory.
[3)]Early samples were released with 128MByte SLC NAND flash memory.

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1.2.3 Interfaces

	Colibri iMX6ULL 1GB IT	Colibri iMX6ULL 512MB WB IT	Colibri iMX6ULL 512MB WB	Colibri iMX6ULL 512MB IT	Colibri iMX6ULL 256MB
Wi-Fi IEEE 802.11 ac/a/b/g/n Dual-Band (2.4/5 GHz)	-	1	1	-	-
Bluetooth v5.0/BLE	-	1	1	-	-
LCD RGB (24-bit, 85MHz)	1	1	1	1	1
Resistive Touch Screen	4 Wire	4 Wire	4 Wire	4 Wire	4 Wire
Analog Audio Headphone out	-	-	-	-	-
Analog Audio Line in	-	-	-	-	-
Analog Audio Mic in	-	-	-	-	-
SAI (AC97/I^2S)	3* (Stereo)	3* (Stereo)	3* (Stereo)	3* (Stereo)	3* (Stereo)
SPDIF (input/output)	1*	1*	1*	1*	1*
Medium Quality Sound (MQS)	1*	1*	1*	1*	1*
Parallel Camera Interface	1*	1*	1*	1*	1*
I2C	1+2*	1+2*	1+2*	1+2*	1+2*
SPI	1+2*	1+1*	1+1*	1+2*	1+2*
UART	3+5*	3+5*	3+5*	3+5*	3+5*
SD/SDIO/MMC	1	1	1	1+1*	1+1*
GPIO	Up to 98	Up to 88	Up to 88	Up to 94	Up to 94
USB 2.0 OTG (host/device)	1	1	1	1	1
USB 2.0 host	1	1	1	1	1
10/100 MBit/s Ethernet	1	1	1	1	1
RMII/MII interface for 2nd Ethernet PHY on Baseboard	1	1	1	1	1
PWM	4+4*	4+4*	4+4*	4+4*	4+4*
Analog Inputs	4+4*	4+3*	4+3*	4+4*	4+4*
CAN	2*	2*	2*	2*	2*
External Memory Bus	16-bit*	-	-	16-bit*	16-bit*
QSPI	-	-	-	-	-
SIM	-	-	-	-	-

*These additional interfaces are available on pins that are not defined as standard interfaces in the Colibri architecture. They are alternate functions for pins that provide primary interfaces. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. For more information, please also check the list in section 4.4.1 and the description of the associated interface in section 5.

1.2.4 Supported Operating Systems

- ✓ Embedded Linux
- ✓ For other operating systems, please contact Toradex

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1.3 Interface Overview

The table in Figure 1 shows the interfaces that are supported on the Colibri iMX6ULL module and whether an interface is provided as a standard (primary) function or as an alternate function. The UART interface is an example of an interface that uses standard and alternate functions – three UART interfaces are provided as standard functions compatible with other Colibri modules. In comparison, five additional interfaces are available as alternate functions. Using alternate function UART interfaces limits the compatibility of the Colibri iMX6ULL module with other Colibri modules. The alternate function of a pin can only be used if the standard function is not used. Check section 4.1 for a list of all alternate functions of the SODIMM pins. The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Colibri iMX6ULL Module. The tool allows comparing the interfaces of different Colibri modules. More information on this tool can be found here: http://developer.toradex.com/knowledge-base/pinout-designer

Feature	Total	Standard	Alternate Function
4 Wire Resistive Touch	1	1	
Analog Inputs	8*	4	4*
Analog Audio (Line in/out, Mic in)			
Medium Quality Sound (MQS)	1		1
CAN	2		2
Fast Ethernet	1	1	
RMII/MII interface	1		1
GPIO	98*		98*
SAI (AC97/I^{2}S)	3		3
SPDIF (input/output)	1		1
I2C	3	1	2
Parallel Camera	1		1
Parallel LCD	1	1	
PWM	8	4	4
SD/SDIO/MMC	2*	1	1*
SPI	3*	1	2*
UART	8	3	5
USB 2.0 OTG (host/device)	1	1	
USB 2.0 host	1	1	
External Memory Bus 16-bit	1*		1*

Figure 1: Colibri iMX6ULL Module Interfaces

*Some of these interfaces are not available on all versions of the Colibri iMX6ULL module. Please see section 1.2 for more information.

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1.4 Reference Documents

1.4.1 NXP (Freescale) i.MX 6ULL

You find the details about i.MX 6ULL SoC in the Datasheet and Reference Manual provided by NXP.
http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors/i.mx-6-processors/i.mx-6ull-single-core-processor-with-arm-cortex-a7-core:i.MX6ULL

1.4.2 Ethernet Transceiver

Colibri iMX6ULL uses the Micrel KSZ8041NL Ethernet PHY:
http://www.microchip.com/wwwproducts/en/KSZ8041

1.4.3 Touch Screen Controller / ADC

Colibri iMX6ULL uses the Analog Device AD7879-1 Touchscreen Controller.
http://www.analog.com/en/products/analog-to-digital-converters/integrated-special-purpose-converters/capacitive-to-digital-and-touch-screen-controllers/ad7879.html

1.4.4 Wi-Fi and Bluetooth Module

Some of the Colibri iMX6ULL use the Azurewave AW-CM276NF wireless module.
http://wen.azurewave.com/wireless-modules

1.4.5 Toradex Developer Center

You can find additional information on the Toradex Developer Center, which is regularly updated with the latest product support information.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant for the Colibri iMX6ULL.
http://developer.toradex.com

1.4.6 Colibri Evaluation Board Schematics

We provide the complete schematics and the Altium project file (including library symbols and IPC-7351 compliant footprints for the Colibri Evaluation Board and other Carrier Boards). This is a great help when designing your own Carrier Board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.4.7 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows the comparison of the interfaces of different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

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2. Architecture Overview

The following block diagrams only contain the primary interfaces. Interfaces such as the second RGMII/MII Ethernet port, SAI, SPDIF, MQS, and additional instances of CAN, I2C, PWM, and UART are missing in this block diagram. These interfaces are available as alternate functions. Some interfaces cannot be used in combination with others since they share the same pins. More information can be found in section 4.1.

2.1 Colibri iMX6ULL 1GB IT

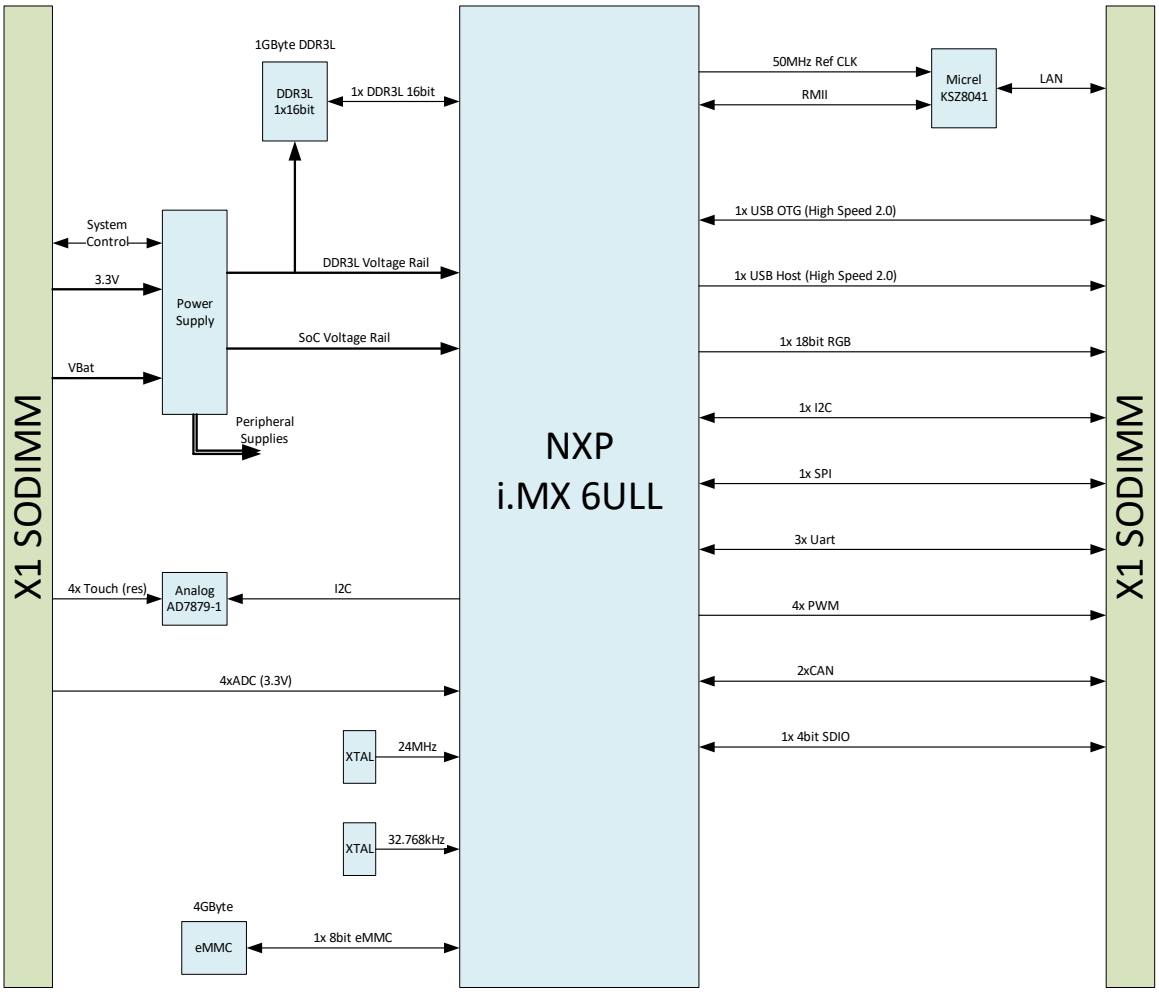


Figure 2 Colibri iMX6ULL 1GB IT Block Diagram

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2.2 Colibri iMX6ULL 512MB WB IT and Colibri iMX6ULL 512MB WB

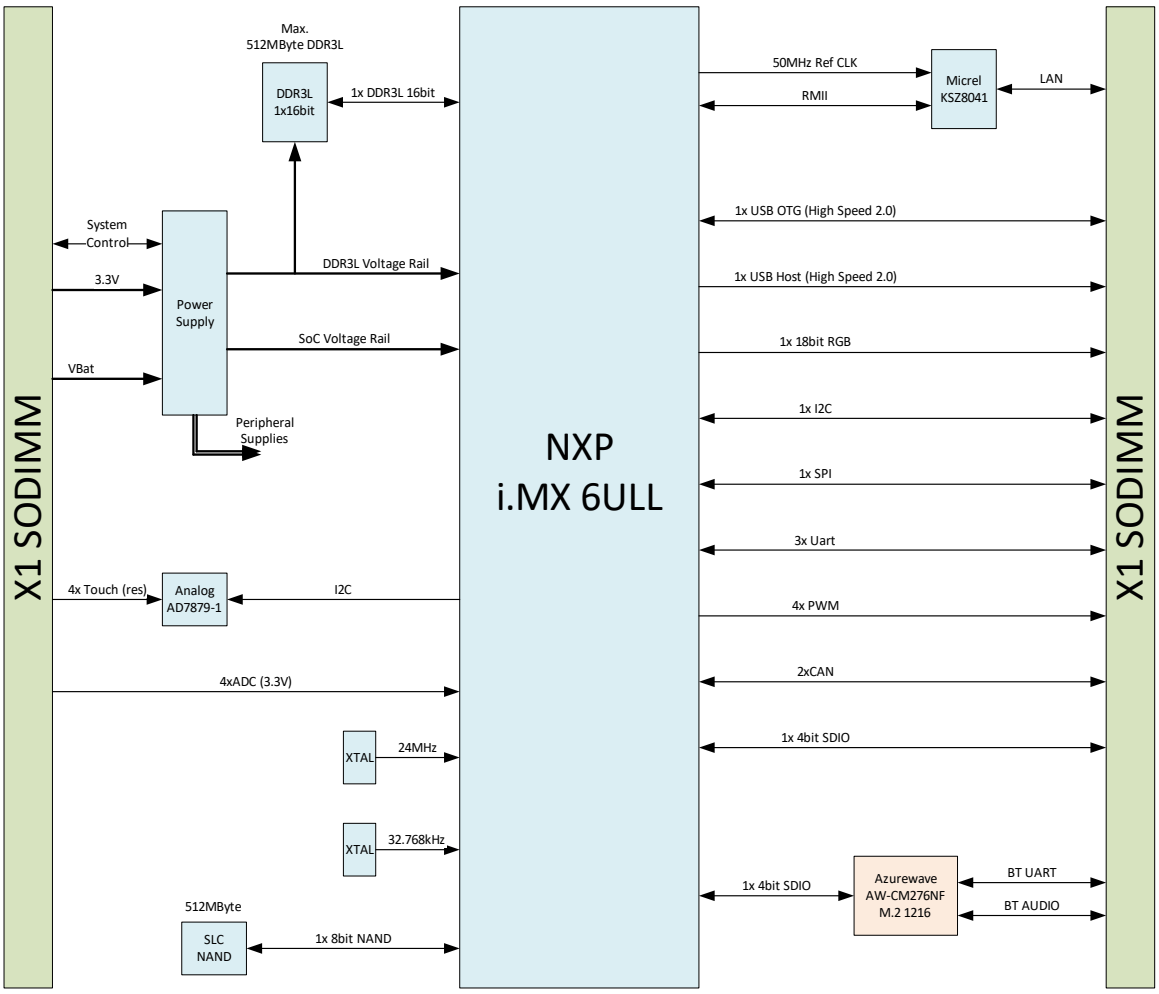


Figure 3 Colibri iMX6ULL 512MB WB and Colibri iMX6ULL 512MB WB IT Block Diagram

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2.3 Colibri iMX6ULL 512MB IT and Colibri iMX6ULL 256MB

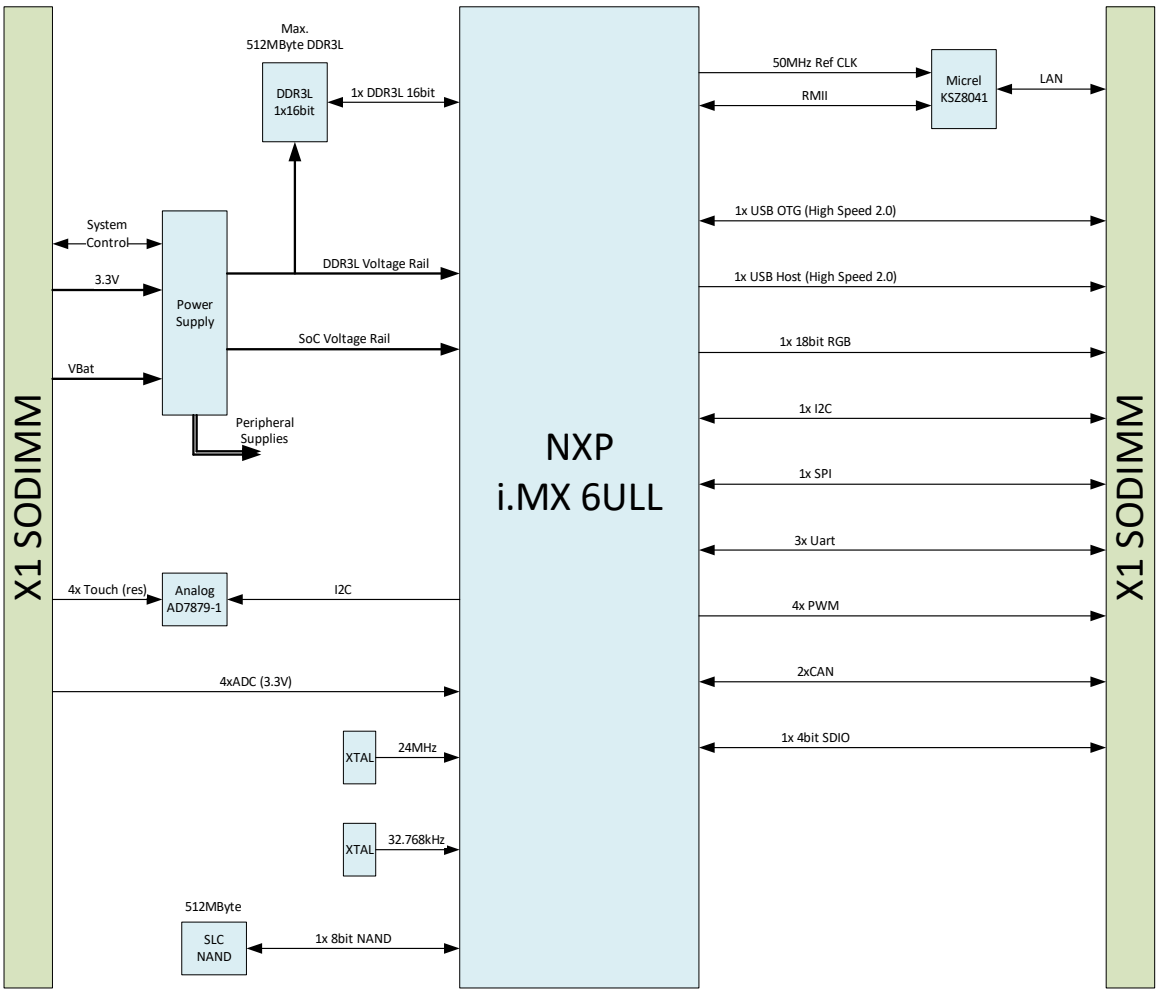


Figure 4 Colibri iMX6ULL 256MB and Colibri iMX6ULL 512MB IT Block Diagram

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3. Colibri iMX6ULL Connector

The Colibri iMX6ULL is equipped with a 200-Pin SODIMM edge connector (X1). The table below details the SODIMM 200-way connector pin functionality.

It should be noted that some of the pins are not available on some modules with Wi-Fi and Bluetooth. The signals are required for interfacing the wireless module. The module version with eMMC has additional pins available on the edge connector. Please check the availability of pins and functions with the help of the Pinout Designer tool.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Default Colibri function: The default function, which is compatible with all Colibri modules. IMPORTANT: There are a few limitations. You can find more information about pin compatibility in the "**Colibri Compatibility Guide**".
- i.MX 6ULL Ball: The name of the ball (a.k.a. pin) of the i.MX 6ULL SoC.
- Non i.MX 6ULL Ball: Peripheral functions which are not directly provided by the i.MX 6ULL SoC.
- Note: Additional information. Some pins are noted as "no standard function". These pins can provide only the GPIO functionality and the listed alternate function, but not the Colibri compatible function. Some of the Colibri compatible functions might be emulated by programmatically manipulating the GPIO.

Table 3-1 X1 Connector

X1 Pin	Default Colibri Function	i.MX 6ULL Ball	Non i.MX 6ULL Ball	Note
1	Audio Analog Microphone Input			no connection
3	Audio Analog Microphone GND			no connection
5	Audio Analog Line-In Left			no connection
7	Audio Analog Line-In Right			no connection
9	Audio_Analog GND		VSS_AUDIO	GND
11	Audio_Analog GND		VSS_AUDIO	GND
13	Audio Analog Headphone GND			no connection
15	Audio Analog Headphone Left			no connection
17	Audio Analog Headphone Right			no connection
19	UART_C RXD	GPIO1_IO04		
21	UART_C TXD	GPIO1_IO05		
23	UART_A DTR	JTAG_TDO		no standard function
25	UART_A CTS, Keypad_In<0>	UART1_CTS		
27	UART_A RTS	UART1_RTS		
29	UART_A DSR	LCD_DATA18		no standard function
31	UART_A DCD	JTAG_TDI		no standard function
33	UART_A RXD	UART1_TXD		
35	UART_A TXD	UART1_RXD		
37	UART_A RI, Keypad_In<4>	LCD_DATA19		no standard function
39	GND		GND	
41	GND		GND	
43	WAKEUP Source<0>,SDCard CardDetect	SNVS_TAMPER0		SNVS pin [2)] no standard function
45	WAKEUP Source<1>	SNVS_TAMPER1		SNVS pin [2)] no standard function

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X1 Pin	Default Colibri Function	i.MX 6ULL Ball	Non i.MX 6ULL Ball	Note
47	SDCard CLK	SD1_CLK [1)]		
49	SDCard DAT<1>	SD1_DATA1 [1)]		
51	SDCard DAT<2>	SD1_DATA2 [1)]		
53	SDCard DAT<3>	SD1_DATA3 [1)]		
55	PS2 SDA1	ENET1_RXD0		no standard function
57	LCD RGB Data<16>	LCD_DATA16		
59	PWM<A>,Camera Input Data<7>	NAND_WP_B		Only PWM supported, no camera input
61	LCD RGB Data<17>	LCD_DATA17		
63	PS2 SCL1	ENET1_RXD1		no standard function
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07		Only camera input supported
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK		Only PWM supported, no camera input
69	PS2 SCL2	CSI_DATA04		no standard function
71	Camera Input Data<0>,LCD Back-Light GPIO	JTAG_TMS		no standard function
73		ENET1_TXD1		
75	Camera Input MCLK	CSI_MCLK		
77		UART3_RXD		
79	Camera Input Data<4>	CSI_DATA02		**Pin not connected on modules with Wi-Fi**
81	Camera Input VSYNC	CSI_VSYNC		**Pin not connected on modules with Wi-Fi**
83	GND		GND	
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06		Only camera input supported
87	nReset Out		Reset IC output	
89	nWE	GPIO1_IO03		**Pin not connected on modules with Wi-Fi**
91	nOE	BOOT_MODE0#		Inverted BOOT_MODE0 signal for recovery
93	RDnWR	SNVS_TAMPER6		SNVS pin [2)] **Pin not connected on modules with Wi-Fi**
95	RDY	SNVS_TAMPER3		SNVS pin [2)] no standard function
97	Camera Input Data<5>	CSI_DATA03		**Pin not connected on modules with Wi-Fi**
99	nPWE	JTAG_TCK		no standard function
101	Camera Input Data<2>	CSI_DATA00		**Pin not connected on modules with Wi-Fi**
103	Camera Input Data<3>	CSI_DATA01		**Pin not connected on modules with Wi-Fi**
105	nCS0	BOOT_MODE0		no standard function make sure this pin is low during booting SNVS pin [2)]
107	nCS1	SNVS_TAMPER4		SNVS pin [2)] no standard function

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X1 Pin	Default Colibri Function	i.MX 6ULL Ball	Non i.MX 6ULL Ball	Note
109	GND		GND	
111	ADDRESS0		GPIO[8]/ UART_SOUT	AW-CM276NF Pin 55, Only on modules with Wi-Fi
113	ADDRESS1		GPIO[9]/ UART_SIN	AW-CM276NF Pin 56, Only on modules with Wi-Fi
115	ADDRESS2		GPIO[10]/ UART_CTSn	AW-CM276NF Pin 54, Only on modules with Wi-Fi
117	ADDRESS3		GPIO[11]/ UART_RTSn	AW-CM276NF Pin 57, Only on modules with Wi-Fi
119	ADDRESS4		GPIO[22]/ PCIE_W_DISABLEn	AW-CM276NF Pin 63, Only on modules with Wi-Fi
121	ADDRESS5		GPIO[14]/ TCK/ WLAN Wake Host	AW-CM276NF Pin 46, Only on modules with Wi-Fi
123	ADDRESS6		GPIO[13]/ BT IRQ(O)	AW-CM276NF Pin 28, Only on modules with Wi-Fi
125	ADDRESS7		GPIO[2]/ WLAN_LED	AW-CM276NF Pin 64, Only on modules with Wi-Fi
127		BOOT_MODE1		**Pin not connected for modules with Wi-Fi**, make sure this pin is low during booting SNVS pin [2]
129	USB Host Power Enable	GPIO1_IO02		
131	USB Host Over-Current Detect	SNVS_TAMPER5		SNVS pin [2]
133		NAND_CE1_B		no standard function
135	SPDIF_IN	UART3_TXD		no standard function
137	USB Client Cable Detect,SPDIF_OUT	SNVS_TAMPER2		SNVS pin [2]
139	USB Host DP	USB_OTG2_DP		
141	USB Host DM	USB_OTG2_DN		
143	USB Client DP	USB_OTG1_DP		
145	USB Client DM	USB_OTG1_DN		
147	GND		GND	
149	DATA0			no connection
151	DATA1			no connection
153	DATA2			no connection
155	DATA3			no connection
157	DATA4			no connection
159	DATA5			no connection
161	DATA6			no connection
163	DATA7			no connection
165	DATA8			no connection
167	DATA9			no connection
169	DATA10			no connection
171	DATA11			no connection
173	DATA12			no connection
175	DATA13			no connection
177	DATA14			no connection

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X1 Pin	Default Colibri Function	i.MX 6ULL Ball	Non i.MX 6ULL Ball	Note
179	DATA15			no connection
181	GND		GND	
183	Ethernet Link/Activity Status		LINK_AKT	KSZ8041 LED0
185	Ethernet Speed Status		SPEED100	KSZ8041 LED1
187	Ethernet TXO-		TXO-	KSZ8041 Pin 6
189	Ethernet TXO+		TXO+	KSZ8041 Pin 7
191	Ethernet GND		AGND_LAN	
193	Ethernet RXI-		RXI-	KSZ8041 Pin 4
195	Ethernet RXI+		RXI+	KSZ8041 Pin 5
197	GND		GND	
199	GND		GND	
2	Analog Input <3>	GPIO1_IO09		ADC Input
4	Analog Input <2>	GPIO1_IO08		ADC Input
6	Analog Input <1>	GPIO1_IO01		ADC Input
8	Analog Input <0>	GPIO1_IO00		ADC Input
10	Audio_Analog VDD		AVDD_AUDIO	3.3V Supply for ADC
12	Audio_Analog VDD		AVDD_AUDIO	3.3V Supply for ADC
14	Resistive Touch PX		TSPX	AD7819 Ball A3
16	Resistive Touch MX		TSMX	AD7819 Ball C3
18	Resistive Touch PY		TSPY	AD7819 Ball B3
20	Resistive Touch MY		TSMY	AD7819 Ball D3
22	VDD Fault Detect			no connection
24	Battery Fault Detect			no connection
26	nReset In		Reset IC input	
28	PWM<B>	NAND_DQS		
30	PWM<C>	ENET1_TXEN		
32	UART_B CTS	UART2_CTS		
34	UART_B RTS	UART2_RTS		
36	UART_B RXD	UART2_TXD		
38	UART_B TXD	UART2_RXD		
40	VCC_BATT		VCC_BATT	RTC supply
42	3V3		3V3	
44	LCD RGB DE	LCD_ENABLE		
46	LCD RGB Data<7>	LCD_DATA07		
48	LCD RGB Data<9>	LCD_DATA09		
50	LCD RGB Data<11>	LCD_DATA11		
52	LCD RGB Data<12>	LCD_DATA12		
54	LCD RGB Data<13>	LCD_DATA13		
56	LCD RGB PCLK	LCD_CLK		
58	LCD RGB Data<3>	LCD_DATA03		
60	LCD RGB Data<2>	LCD_DATA02		
62	LCD RGB Data<8>	LCD_DATA08		
64	LCD RGB Data<15>	LCD_DATA15		

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X1 Pin	Default Colibri Function	i.MX 6ULL Ball	Non i.MX 6ULL Ball	Note
66	LCD RGB Data<14>	LCD_DATA14		
68	LCD RGB HSYNC	LCD_HSYNC		
70	LCD RGB Data<1>	LCD_DATA01		
72	LCD RGB Data<5>	LCD_DATA05		
74	LCD RGB Data<10>	LCD_DATA10		
76	LCD RGB Data<0>	LCD_DATA00		
78	LCD RGB Data<4>	LCD_DATA04		
80	LCD RGB Data<6>	LCD_DATA06		
82	LCD RGB VSYNC	LCD_VSYNC		
84	3V3		3V3	
86	SPI CS	LCD_DATA21		
88	SPI CLK	LCD_DATA20		
90	SPI RXD	LCD_DATA23		
92	SPI TXD	LCD_DATA22		
94	Camera Input HSYNC	CSI_HSYNC		**Pin not connected on modules with Wi-Fi**
96	Camera Input PCLK	CSI_PIXCLK		
98	Camera Input Data<1>	CSI_DATA05		no standard function
100	Keypad_Out<1>	UART3_CTS		no standard function
102		JTAG_TRST_B		no standard function
104		ENET1_RXER		no standard function
106	nCS2	JTAG_MOD		no standard function, 10k pull down on the module
108	3V3		3V3	
110	ADDRESS8			no connection
112	ADDRESS9		GPIO[6]/ PCM_CLK	AW-CM276NF Pin 61 Only on modules with Wi-Fi
114	ADDRESS10		GPIO[7]/ PCM_SYNC	AW-CM276NF Pin 58, Only on modules with Wi-Fi
116	ADDRESS11		GPIO[4]/ PCM_IN	AW-CM276NF Pin 59, Only on modules with Wi-Fi
118	ADDRESS12		GPIO[5]/ PCM_OUT	AW-CM276NF Pin 60, Only on modules with Wi-Fi
120	ADDRESS13		GPIO[15]/ TMS/ Host Wake WLAN	AW-CM276NF Pin 66, Only on modules with Wi-Fi
122	ADDRESS14		GPIO[12]/ UART Host Wake BT	AW-CM276NF Pin 53, Only on modules with Wi-Fi
124	ADDRESS15	USB_OTG1_CHDn		
126	DQM0		GPIO3/ BT_LED	AW-CM276NF Pin 65, Only on modules with Wi-Fi
128	DQM1			no connection
130	DQM2			no connection
132	DQM3			no connection
134	ADDRESS25			no connection
136	ADDRESS24			no connection

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X1 Pin	Default Colibri Function	i.MX 6ULL Ball	Non i.MX 6ULL Ball	Note
138	ADDRESS23	SNVS_TAMPER8		SNVS pin [2] **Pin not connected on modules with Wi-Fi**
140	ADDRESS22	NAND_ALE		**Only available on Colibri iMX6ULL 1GB IT**
142	ADDRESS21	NAND_READY_B		**Only available on Colibri iMX6ULL 1GB IT**
144	ADDRESS20	NAND_CE0_B		**Only available on Colibri iMX6ULL 1GB IT**
146	ADDRESS19	NAND_CLE		**Only available on Colibri iMX6ULL 1GB IT**
148	3V3		3V3	
150	DATA16			no connection
152	DATA17			no connection
154	DATA18			no connection
156	DATA19			no connection
158	DATA20			no connection
160	DATA21			no connection
162	DATA22			no connection
164	DATA23			no connection
166	DATA24			no connection
168	DATA25			no connection
170	DATA26			no connection
172	DATA27			no connection
174	DATA28			no connection
176	DATA29			no connection
178	DATA30	ENET1_CRS_DV		no standard function
180	DATA31	GPIO1_IO06		no standard function
182	3V3		3V3	
184	ADDRESS18	GPIO1_IO07		no standard function
186	ADDRESS17	UART3_RTS		no standard function
188	ADDRESS16	ENET1_TXD0		no standard function
190	SDCard CMD	SD1_CMD [1]		
192	SDCard DAT<0>	SD1_DATA0 [1]		
194	I2C SDA	UART4_RXD		
196	I2C SCL	UART4_TXD		
198	3V3		3V3	
200	3V3		3V3	

[1] It is possible to change the IO voltage of the main SD interface from 3.3V (default) to 1.8V to support SD UHS-I speeds. Please note that the voltage can only be changed for all the pins simultaneously and not individually. Therefore, use these pins with care. More information can be found in section 5.13.
[2] These pins are in the SNVS power block of the SoC. This means the pins remain powered in the “RTC Only” power mode by the VCC_BATT rail. Make sure there is no backfeeding on this pin. Otherwise, a high RTC battery consumption can be caused. More information can be found in sections 5.1 and 6.2.

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4. I/O Pins

4.1 Function Multiplexing

Each NXP i.MX 6ULL SoC I/O pin can be configured to one of the up to ten alternate functions. Most of the pins can also be used as "normal" GPIOs (General Purpose I/O, sometimes referred to as Digital I/O). For example, the i.MX 6ULL signal pin on the SODIMM pin 33 has the primary function uart1.TX (Colibri standard function UART_A_RXD), but can also provide the following alternate functions: enet1.RDATA[2] (RMII), i2c3.SCL (I2C), csi.DATA[2] (camera input), gpt1.COMPARE1 (timer), gpio1.IO[16] (GPIO), anatop.USBPHY1_TSTI_TX_LS_MODE (USB test), ecspi4.TESTER_TRIGGER (SPI), spdif.OUT (SPDIF), and uart5.TX (UART)

The default setting for this pin is the primary function uart1.TX. It is strongly recommended that whenever it is possible, use the primary interfaces before using any alternate interfaces. This ensures the best compatibility between the Toradex standard software, operating systems/BSPs, and other modules in the Colibri family.

Most of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the table in section 4.4.1, you find a list of all pins, which have alternate functions. There you can find which alternate functions are available for each individual pin.

Special care must be taken with the BOOT_MODE0 (SODIMM pin 105) and BOOT_MODE1 (SODIMM pin 127). The BOOT_MODE1 signal is only available on SODIMM pin 127 for the modules without Wi-Fi. These two pins are used to strap the boot mode of the module. To boot the module normally, make sure these two pins are kept low during the release of the reset. The pins have an on module 10kΩ pull-down resistors which allows leaving them unconnected. An additional circuit on the BOOT_MODE0 pin allows using the SODIMM pin 91 for strapping the module into recovery mode. More details on the recovery mode can be found in section 7 of this document.

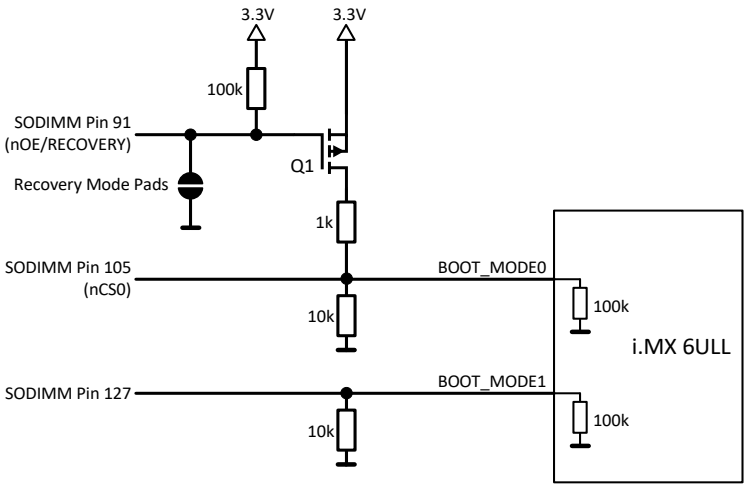


Figure 5: Recovery Mode Glue Logic

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4.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be configured (some settings might not be available for certain pins). The register is called IOMUXC_SW_MUX_CTL_PAD_x, where x is the name of the i.MX 6ULL pin. More information about the available register settings can be found in the i.MX 6ULL Reference Manual.

Table 4-1 Pad Mux Register

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enabled	Force the selected mux mode input path
3-0	MUX_MODE	0000 Select mux mode: ALT0 mux port 0001 Select mux mode: ALT1 mux port 0010 Select mux mode: ALT2 mux port 0011 Select mux mode: ALT3 mux port 0100 Select mux mode: ALT4 mux port 0101 Select mux mode: ALT5 mux port (GPIO) 0110 Select mux mode: ALT6 mux port 0111 Select mux mode: ALT7 mux port 1000 Select mux mode: ALT8 mux port 1001 Select mux mode: ALT9 mux port	Check section 0 for the available alternate function of the pin

The pins have an additional register that allows the configuration of pull up/down resistors, drive strength, and other settings. The register is called IOMUXC_SW_PAD_CTL_PAD_x, where x is the name of the i.MX 6ULL pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX 6ULL Reference Manual.

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Table 4-2 Pad Control Register

Bit	Field	Description	Remarks
31-17	Reserved		
16	HYS	0 CMOS input 1 Schmitt trigger input	
15-14	PUS	00 100 kOhm Pull Down 01 47 kOhm Pull Up 10 100 kOhm Pull Up 11 22 kOhm Pull Up	
13	PUE	0 Keeper enable 1 Pull enable	Selection between keeper and pull up/down function
12	PKE	0 Pull/Keeper Disabled 1 Pull/Keeper Enabled	Enable keeper or pull up/down function
11	ODE	0 Output is CMOS 1 Output is open drain	
10-8	Reserved		
7-6	SPEED	00 Low (50 MHz) 01 Medium (100 MHz) 10 Medium (100 MHz) 11 High (200 MHz)	
5-3	DSE	000 output driver disabled (Hi Z) 001 260 Ohm 010 130 Ohm 011 87 Ohm 100 65 Ohm 101 52 Ohm 110 43 Ohm 111 37 Ohm	If possible, decrease the drive strength by increasing the resistance to reduce EMC problems
2-1	Reserved		
0	SRE	0 Slow Slew Rate 1 Fast Slew Rate	Use a slow slew rate if possible for reducing EMC problems

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC_x_SELECT_INPUT, where x is the name of the input function. More information about this register can be found in the i.MX 6ULL Reference Manual.

4.3 Pin Reset Status

After a reset, the pins can be at any of the different modes. Most of them are configured as GPIO input with a 100k pull-down resistor enabled. Please check the table in section 4.4.1 for the reset states for each of the pins. For pins that are not configured as GPIO by default, please check the i.MX 6ULL Reference Manual for the corresponding default configuration state. As soon as the bootloader is executing, it is possible to reconfigure the pins and their states.

Please be aware. The pin reset status is only guaranteed during the release of the reset signal. During the power-up sequence, the states of the pins might be undefined until the IO bank voltage is enabled on the module.

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4.4 Functions List

Below is a list of all the i.MX 6ULL pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT5 function. The alternate functions used to provide the primary interfaces to ensure the best compatibility with other Colibri modules are highlighted.

Please note: not all pins are available on the module with Wi-Fi. Check the available pins in Table 3-1 or use the Toradex Pinout Designer.

Function Short Forms

ADC:	Analog-Digital Convert input
CAN:	Controller Area Network
CCM:	Clock Control Module
CSI:	Camera Sensor Interface
ECSPI:	Enhanced Configurable Serial Peripheral Interface Bus
ENET:	Ethernet MAC interface
EPDC:	Electrophoretic Display Controller (Electronic Paper Display)
ESAI:	Enhanced Serial Audio Interface
GPIO:	General Purpose Input Output
GPT:	General Purpose Timer
I2C:	Inter Integrated Circuit
KPP:	Keypad Port
LCDIF:	LCD Interface
MQS:	Medium Quality Sound
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
RAWNAND:	Interface for NAND Flash
SAI:	Serial Interface for Audio (I2S and AC97)
SIM:	Subscriber Identification Module
SJC:	JTAG Debug Interface
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
WDOG:	Watchdog Timer
WEIM:	External Interface Module (External Memory Bus)

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4.4.1 SODIMM 200

X1 Pin	i.MX 6ULL Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ADC	Reset State	Pull
19	GPIO1_IO04	anatop.ENET_REF_CLK1	pwm3.OUT	usb.OTG1_PWR	anatop.24M_OUT	usdhc1.RESET_B	gpio1.IO[4]	enet2.1588_EVENT0_IN	ccm.PLL2_BYP	uart5.TX		ADCx_IN4	ALT5	Keeper
21	GPIO1_IO05	anatop.ENET_REF_CLK2	pwm4.OUT	anatop.OTG2_ID	csi.FIELD	usdhc1.VSELECT	gpio1.IO[5]	enet2.1588_EVENT0_OUT	ccm.PLL3_BYP	uart5.RX		ADCx_IN5	ALT5	Keeper
23	JTAG_TDO	sjc.TDO	gpt2.CAPTURE2	sai2.TX_SYNC	ccm.CLKO2	ccm.STOP	gpio1.IO[12]	mqs.RIGHT		epit2.OUT			ALT0	100K PU
25	UART1_CTS	uart1.CTS_B	enet1.RX_CLK	usdhc1.WP	csi.DATA[4]	enet2.1588_EVENT1_IN	gpio1.IO[18]	anatop.USBPHY1_TSTI_TX_DN	usdhc2.TESTER_TRIGGER [2]	usdhc2.WP [2]	uart5.CTS_B		ALT5	Keeper
27	UART1_RTS	uart1.RTS_B	enet1.TX_ER	usdhc1.CD_B	csi.DATA[5]	enet2.1588_EVENT1_OUT	gpio1.IO[19]	anatop.USBPHY1_TSTO_RX_SQUELCH	qspi.TESTER_TRIGGER	usdhc2.CD_B [2]	uart5.RTS_B		ALT5	Keeper
29	LCD_DATA18	lcdif.DATA[18]	pwm5.OUT	ca7_platform.EVENTO	csi.DATA[10]	weim.DATA[10]	gpio3.IO[23]	src.BT_CFG[26]	tpsmp.CLK	usdhc2.CMD [2]	epdc.BDR[1]		ALT5	100K PD
31	JTAG_TDI	sjc.TDI	gpt2.COMPARE1	sai2.TX_BCLK	ccm.OUT0	pwm6.OUT	gpio1.IO[13]	mqs.LEFT					ALT0	47K PU
33	UART1_TXD	uart1.TX	enet1.RDATA[2]	i2c3.SCL	csi.DATA[2]	gpt1.COMPARE1	gpio1.IO[16]	anatop.USBPHY1_TSTI_TX_LS_MODE	ecspi4.TESTER_TRIGGER	spdif.OUT	uart5.TX		ALT5	Keeper
35	UART1_RXD	uart1.RX	enet1.RDATA[3]	i2c3.SDA	csi.DATA[3]	gpt1.CLK	gpio1.IO[17]	anatop.USBPHY1_TSTI_TX_HS_MODE	usdhc1.TESTER_TRIGGER	spdif.IN	uart5.RX		ALT5	Keeper
37	LCD_DATA19	lcdif.DATA[19]	pwm6.OUT	global wdog	csi.DATA[11]	weim.DATA[11]	gpio3.IO[24]	src.BT_CFG[27]	tpsmp.HDATA_DIR	usdhc2.CLK [2]	epdc.VCOM[0]		ALT5	100K PD
43	SNVS_TAMPER0	snvs_lp_wrapper.TAMPER[0]					gpio5.IO[0]						ALT0	Keeper
45	SNVS_TAMPER1	snvs_lp_wrapper.TAMPER[1]					gpio5.IO[1]						ALT0	Keeper
47	SD1_CLK	usdhc1.CLK	gpt2.COMPARE2	sai2.MCLK	spdif.IN	weim.ADDR[20]	gpio2.IO[17]	ccm.OUT0	observe_mux.OUT[0]	usb.OTG1_OC			ALT5	Keeper
49	SD1_DATA1	usdhc1.DATA1	gpt2.CLK	sai2.TX_BCLK	can1.RX	weim.ADDR[22]	gpio2.IO[19]	ccm.OUT2	observe_mux.OUT[2]	usb.OTG2_PWR			ALT5	Keeper
51	SD1_DATA2	usdhc1.DATA2	gpt2.CAPTURE1	sai2.RX_DATA	can2.TX	weim.ADDR[23]	gpio2.IO[20]	ccm.CLKO1	observe_mux.OUT[3]	usb.OTG2_OC			ALT5	Keeper
53	SD1_DATA3	usdhc1.DATA3	gpt2.CAPTURE2	sai2.TX_DATA	can2.RX	weim.ADDR[24]	gpio2.IO[21]	ccm.CLKO2	observe_mux.OUT[4]	anatop.OTG2_ID			ALT5	Keeper
55	ENET1_RXD0	enet1.RDATA[0]	uart4.RTS_B	pwm1.OUT	csi.DATA[16]	can1.TX	gpio2.IO[0]	kpp.ROW[0]	sim_m.HADDR[7]	usdhc1.LCTL	epdc.SDCE[4]		ALT5	Keeper
57	LCD_DATA16	lcdif.DATA[16]	uart7.TX	ca7_platform.TRACE_CLK	csi.DATA[1]	weim.DATA[8]	gpio3.IO[21]	src.BT_CFG[24]	sim_m.HSIZE[2]	usdhc2.DATA6 [2]	epdc.GDCLK		ALT5	100K PD
59	NAND_WP_B	rawnand.WP_B	usdhc1.RESET_B	qspiA_SCLK	pwm4.OUT	weim.BCLK	gpio4.IO[11]	anatop.TESTO[11]	tpsmp.HDATA[13]	ecspi3.RDY			ALT5	Keeper
61	LCD_DATA17	lcdif.DATA[17]	uart7.RX	ca7_platform.TRACE_CTL	csi.DATA[0]	weim.DATA[9]	gpio3.IO[22]	src.BT_CFG[25]	sim_m.HWRITE	usdhc2.DATA7 [2]	epdc.GDSP		ALT5	100K PD
63	ENET1_RXD1	enet1.RDATA[1]	uart4.CTS_B	pwm2.OUT	csi.DATA[17]	can1.RX	gpio2.IO[1]	kpp.COL[0]	sim_m.HADDR[8]	usdhc2.LCTL [2]	epdc.SDCE[5]		ALT5	Keeper
65	CSI_DATA07	csi.DATA[9]	usdhc2.DATA7 [2]		ecspi1.MISO	weim.AD[7]	gpio4.IO[28]	sai1.TX_DATA	tpsmp.HDATA[31]	usdhc1.VSELECT	esai.TX0		ALT5	Keeper
67	ENET1_TXCLK	enet1.TX_CLK	uart7.CTS_B	pwm7.OUT	csi.DATA[22]	anatop.ENET_REF_CLK1	gpio2.IO[6]	kpp.ROW[3]	sim_m.HADDR[13]	gpt1.CLK	epdc.SDOED		ALT5	Keeper
69	CSI_DATA04	csi.DATA[6]	usdhc2.DATA4 [2]		ecspi1.SCLK	weim.AD[4]	gpio4.IO[25]	sai1.TX_SYNC	tpsmp.HDATA[28]	usdhc1.WP	esai.TX_FS		ALT5	Keeper
71	JTAG_TMS	sjc.TMS	gpt2.CAPTURE1	sai2.MCLK	ccm.CLKO1	ccm.WAIT	gpio1.IO[11]	sdma.EXT_EVENT[1]		epit1.OUT			ALT0	47K PU

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X1 Pin	i.MX 6ULL Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ADC	Reset State	Pull
73	ENET1_TXD1	enet1.TDATA[1]	uart6.CTS_B	pwm5.OUT	csi.DATA[20]	enet2.MDIO	gpio2.IO[4]	kpp.ROW[2]	sim_m.HADDR[11]	wdog1.WDOG_RST_B_DEB	epdc.SDCE[8]		ALT5	Keeper
75	CSI_MCLK	csi.MCLK	usdhc2.CD_B [2])	rawnand.CE2_B	i2c1.SDA	weim.CS0_B	gpio4.IO[17]	snvs_hp_wrapper.VIO_5_CTL	tpsmp.HDATA[20]	uart6.TX	esai.TX3_RX2		ALT5	Keeper
77	UART3_RXD	uart3.RX	enet2.RDATA[3]		csi.DATA[0]	uart2.RTS_B	gpio1.IO[25]	anatop.USBPHY1_TSTI_TX_EN	sim_m.HADDR[0]	epit1.OUT			ALT5	Keeper
79	CSI_DATA02 [1])	csi.DATA[4]	usdhc2.DATA2 [2])		ecspi2.MOSI	weim.AD[2]	gpio4.IO[23]	sai1.RX_SYNC	tpsmp.HDATA[26]	uart5.RTS_B	esai.RX_FS		ALT5	Keeper
81	CSI_VSYNC [1])	csi.VSYNC	usdhc2.CLK [2])		i2c2.SDA	weim.RW	gpio4.IO[19]	pwm7.OUT	tpsmp.HDATA[22]	uart6.RTS_B	esai.TX4_RX1		ALT5	Keeper
85	CSI_DATA06	csi.DATA[8]	usdhc2.DATA6		ecspi1.MOSI	weim.AD[6]	gpio4.IO[27]	sai1.RX_DATA	tpsmp.HDATA[30]	usdhc1.RESET_B	esai.TX5_RX0		ALT5	Keeper
89	GPIO1_IO03 [1])	i2c1.SDA	gpt1.COMPARE3	usb.OTG2_OC	osc32k.32K_OUT	usdhc1.CD_B	gpio1.IO[3]	ccm.DI0_EXT_CLK	src.TESTER_ACK	uart1.RX		ADCx_IN3	ALT5	100K PD
93	SNVS_TAMPER6 [1])	snvs_lp_wrapper.TAMPER[6]					gpio5.IO[6]						ALT0	Keeper
95	SNVS_TAMPER3	snvs_lp_wrapper.TAMPER[3]					gpio5.IO[3]						ALT0	Keeper
97	CSI_DATA03 [1])	csi.DATA[5]	usdhc2.DATA3 [2])		ecspi2.MISO	weim.AD[3]	gpio4.IO[24]	sai1.RX_BCLK	tpsmp.HDATA[27]	uart5.CTS_B	esai.RX_CLK		ALT5	Keeper
99	JTAG_TCK	sjc.TCK	gpt2.COMPARE2	sai2.RX_DATA	ccm.OUT1	pwm7.OUT	gpio1.IO[14]	osc32k.32K_OUT					ALT0	47K PU
101	CSI_DATA00 [1])	csi.DATA[2]	usdhc2.DATA0 [2])		ecspi2.SCLK	weim.AD[0]	gpio4.IO[21]	src.INT_BOOT	tpsmp.HDATA[24]	uart5.TX	esai.TX_HF_CLK		ALT5	Keeper
103	CSI_DATA01 [1])	csi.DATA[3]	usdhc2.DATA1 [2])		ecspi2.SS0	weim.AD[1]	gpio4.IO[22]	sai1.MCLK	tpsmp.HDATA[25]	uart5.RX	esai.RX_HF_CLK		ALT5	Keeper
105	BOOT_MODE0	src.BOOT_MODE[0]					gpio5.IO[10]						ALT0	100K PD
107	SNVS_TAMPER4	snvs_lp_wrapper.TAMPER[4]					gpio5.IO[4]						ALT0	Keeper
127	BOOT_MODE1 [1])	src.BOOT_MODE[1]					gpio5.IO[11]						ALT0	100K PD
129	GPIO1_IO02	i2c1.SCL	gpt1.COMPARE2	usb.OTG2_PWR	anatop.ENET_REF_CLK_25M	usdhc1.WP	gpio1.IO[2]	sdma.EXT_EVENT[0]	src.ANY_PU_RESET	uart1.TX		ADCx_IN2	ALT5	Keeper
131	SNVS_TAMPER5	snvs_lp_wrapper.TAMPER[5]					gpio5.IO[5]						ALT0	Keeper
133	NAND_CE1_B	rawnand.CE1_B	usdhc1.DATA6	qspiA_DATA[2]	ecspi3.MOSI	weim.ADDR[18]	gpio4.IO[14]	anatop.TESTO[14]	tpsmp.HDATA[16]	uart3.CTS_B			ALT5	Keeper
135	UART3_TXD	uart3.TX	enet2.RDATA[2]		csi.DATA[1]	uart2.CTS_B	gpio1.IO[24]	anatop.USBPHY1_TSTI_TX_DP	sjc.JTAG_ACT	anatop.OTG1_ID			ALT5	0
137	SNVS_TAMPER2	snvs_lp_wrapper.TAMPER[2]					gpio5.IO[2]						ALT0	Keeper
2	GPIO1_IO09	pwm2.OUT	global wdog	spdif.IN	csi.HSYNC	usdhc2.RESET_B [2])	gpio1.IO[9]	usdhc1.RESET_B	ecspi3.TESTER_TRIGGER	uart5.CTS_B		ADCx_IN9	ALT5	Keeper
4	GPIO1_IO08	pwm1.OUT	wdog1.WDOG_B	spdif.OUT	csi.VSYNC	usdhc2.VSELECT [2])	gpio1.IO[8]	ccm.PMIC_RDY	ecspi2.TESTER_TRIGGER	uart5.RTS_B		ADCx_IN8	ALT5	Keeper
6	GPIO1_IO01	i2c2.SDA	gpt1.COMPARE1	usb.OTG1_OC	anatop.ENET_REF_CLK2	mqs.LEFT	gpio1.IO[1]	enet1.1588_EVENT0_OUT	src.EARLY_RESET	wdog1.WDOG_B		ADCx_IN1	ALT5	Keeper
8	GPIO1_IO00	i2c2.SCL	gpt1.CAPTURE1	anatop.OTG1_ID	anatop.ENET_REF_CLK1	mqs.RIGHT	gpio1.IO[0]	enet1.1588_EVENT0_IN	src.SYSTEM_RESET	wdog3.WDOG_B		ADCx_IN0	ALT5	Keeper
28	NAND_DQS	rawnand.DQS	csi.FIELD	qspiA_SS0_B	pwm5.OUT	weim.WAIT	gpio4.IO[16]	sdma.EXT_EVENT[1]	tpsmp.HDATA[17]	spdif.EXT_CLK			ALT5	Keeper
30	ENET1_TXEN	enet1.TX_EN	uart6.RTS_B	pwm6.OUT	csi.DATA[21]	enet2.MDC	gpio2.IO[5]	kpp.COL[2]	sim_m.HADDR[12]	wdog2.WDOG_RST_B_DEB	epdc.SDCE[9]		ALT5	Keeper
32	UART2_CTS	uart2.CTS_B	enet1.CRS	can2.TX	csi.DATA[8]	gpt1.COMPARE2	gpio1.IO[22]	anatop.USBPHY2_TSTO_RX_FS_RXD	sjc.DE_B	ecspi3.MOSI			ALT5	Keeper

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X1 Pin	i.MX 6ULL Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ADC	Reset State	Pull
34	UART2_RTS	uart2.RTS_B	enet1.COL	can2.RX	csi.DATA[9]	gpt1.COMPARE3	gpio1.IO[23]	anatop.USBPHY1_TSTO_RX_FS_RXD	sjc.FAIL	ecspi3.MISO			ALT5	Keeper
36	UART2_TXD	uart2.TX	enet1.TDATA[2]	i2c4.SCL	csi.DATA[6]	gpt1.CAPTURE1	gpio1.IO[20]	anatop.USBPHY1_TSTO_RX_DISCON_DET	rawnand.TESTER_TRIGGER	ecspi3.SS0			ALT5	Keeper
38	UART2_RXD	uart2.RX	enet1.TDATA[3]	i2c4.SDA	csi.DATA[7]	gpt1.CAPTURE2	gpio1.IO[21]	anatop.USBPHY1_TSTO_RX_HS_RXD	sjc.DONE	ecspi3.SCLK			ALT5	Keeper
44	LCD_ENABLE	lcdif.ENABLE	lcdif.RD_E	uart4.RX	sai3.TX_SYNC	weim.CS3_B	gpio3.IO[1]	anatop.TESTI[0]	sim_m.HADDR[24]	ecspi2.RDY	epdc.SDLE		ALT5	100K PD
46	LCD_DATA07	lcdif.DATA[7]	uart7.RTS_B	ca7_platform.TRACE[7]	enet2.1588_EVENT3_OUT	spdif.EXT_CLK	gpio3.IO[12]	src.BT_CFG[7]	sim_m.HMASTLOCK	ecspi1.SS3	epdc.SDDO[7]		ALT5	100K PD
48	LCD_DATA09	lcdif.DATA[9]	sai3.MCLK	ca7_platform.TRACE[9]	csi.DATA[17]	weim.DATA[1]	gpio3.IO[14]	src.BT_CFG[9]	sim_m.HPROT[1]	can1.RX	epdc.PWRWAKE		ALT5	100K PD
50	LCD_DATA11	lcdif.DATA[11]	sai3.RX_BCLK	ca7_platform.TRACE[11]	csi.DATA[19]	weim.DATA[3]	gpio3.IO[16]	src.BT_CFG[11]	sim_m.HPROT[3]	can2.RX	epdc.PWRSTAT		ALT5	100K PD
52	LCD_DATA12	lcdif.DATA[12]	sai3.TX_SYNC	ca7_platform.TRACE[12]	csi.DATA[20]	weim.DATA[4]	gpio3.IO[17]	src.BT_CFG[12]	sim_m.HREADYOUT	ecspi1.RDY	epdc.PWRCTRL[0]		ALT5	100K PD
54	LCD_DATA13	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[18]	src.BT_CFG[13]	sim_m.HRESP	usdhc2.RESET_B [2)]	epdc.BDR[0]		ALT5	100K PD
56	LCD_CLK	lcdif.CLK	lcdif.WR_RWN	uart4.TX	sai3.MCLK	weim.CS2_B	gpio3.IO[0]	ocotp_ctrl_wrapper.FUSE_LATCHED	sim_m.HADDR[23]	wdog1.WDOG_RST_B_DEB	epdc.SDCLK		ALT5	100K PD
58	LCD_DATA03	lcdif.DATA[3]	pwm4.OUT	ca7_platform.TRACE[3]	enet1.1588_EVENT3_OUT	i2c4.SCL	gpio3.IO[8]	src.BT_CFG[3]	sim_m.HADDR[31]	sai1.RX_DATA	epdc.SDDO[3]		ALT5	100K PD
60	LCD_DATA02	lcdif.DATA[2]	pwm3.OUT	ca7_platform.TRACE[2]	enet1.1588_EVENT3_IN	i2c4.SDA	gpio3.IO[7]	src.BT_CFG[2]	sim_m.HADDR[30]	sai1.TX_BCLK	epdc.SDDO[2]		ALT5	100K PD
62	LCD_DATA08	lcdif.DATA[8]	spdif.IN	ca7_platform.TRACE[8]	csi.DATA[16]	weim.DATA[0]	gpio3.IO[13]	src.BT_CFG[8]	sim_m.HPROT[0]	can1.TX	epdc.PWRIRQ		ALT5	100K PD
64	LCD_DATA15	lcdif.DATA[15]	sai3.TX_DATA	ca7_platform.TRACE[15]	csi.DATA[23]	weim.DATA[7]	gpio3.IO[20]	src.BT_CFG[15]	sim_m.HSIZE[1]	usdhc2.DATA5 [2)]	epdc.GDRL		ALT5	100K PD
66	LCD_DATA14	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[19]	src.BT_CFG[14]	sim_m.HSIZE[0]	usdhc2.DATA4 [2)]	epdc.SDSHR		ALT5	100K PD
68	LCD_HSYNC	lcdif.HSYNC	lcdif.RS	uart4.CTS_B	sai3.TX_BCLK	wdog3.WDOG_RST_B_DEB	gpio3.IO[2]	anatop.TESTI[1]	sim_m.HADDR[25]	ecspi2.SS1	epdc.SDOE		ALT5	100K PD
70	LCD_DATA01	lcdif.DATA[1]	pwm2.OUT	ca7_platform.TRACE[1]	enet1.1588_EVENT2_OUT	i2c3.SCL	gpio3.IO[6]	src.BT_CFG[1]	sim_m.HADDR[29]	sai1.TX_SYNC	epdc.SDDO[1]		ALT5	100K PD
72	LCD_DATA05	lcdif.DATA[5]	uart8.RTS_B	ca7_platform.TRACE[5]	enet2.1588_EVENT2_OUT	spdif.OUT	gpio3.IO[10]	src.BT_CFG[5]	sim_m.HBURST[1]	ecspi1.SS1	epdc.SDDO[5]		ALT5	100K PD
74	LCD_DATA10	lcdif.DATA[10]	sai3.RX_SYNC	ca7_platform.TRACE[10]	csi.DATA[18]	weim.DATA[2]	gpio3.IO[15]	src.BT_CFG[10]	sim_m.HPROT[2]	can2.TX	epdc.PWRCOM		ALT5	100K PD
76	LCD_DATA00	lcdif.DATA[0]	pwm1.OUT	ca7_platform.TRACE[0]	enet1.1588_EVENT2_IN	i2c3.SDA	gpio3.IO[5]	src.BT_CFG[0]	sim_m.HADDR[28]	sai1.MCLK	epdc.SDDO[0]		ALT5	100K PD
78	LCD_DATA04	lcdif.DATA[4]	uart8.CTS_B	ca7_platform.TRACE[4]	enet2.1588_EVENT2_IN	spdif.SR_CLK	gpio3.IO[9]	src.BT_CFG[4]	sim_m.HBURST[0]	sai1.TX_DATA	epdc.SDDO[4]		ALT5	100K PD
80	LCD_DATA06	lcdif.DATA[6]	uart7.CTS_B	ca7_platform.TRACE[6]	enet2.1588_EVENT3_IN	spdif.LOCK	gpio3.IO[11]	src.BT_CFG[6]	sim_m.HBURST[2]	ecspi1.SS2	epdc.SDDO[6]		ALT5	100K PD
82	LCD_VSYNC	lcdif.VSYNC	lcdif.BUSY	uart4.RTS_B	sai3.RX_DATA	wdog2.WDOG_B	gpio3.IO[3]	anatop.TESTI[2]	sim_m.HADDR[26]	ecspi2.SS2	epdc.SDCE[0]		ALT5	100K PD
86	LCD_DATA21	lcdif.DATA[21]	uart8.RX	ecspi1.SS0	csi.DATA[13]	weim.DATA[13]	gpio3.IO[26]	src.BT_CFG[29]	tpsmp.HTRANS[1]	usdhc2.DATA1 [2)]	epdc.SDCE[1]		ALT5	100K PD
88	LCD_DATA20	lcdif.DATA[20]	uart8.TX	ecspi1.SCLK	csi.DATA[12]	weim.DATA[12]	gpio3.IO[25]	src.BT_CFG[28]	tpsmp.HTRANS[0]	usdhc2.DATA0 [2)]	epdc.VCOM[1]		ALT5	100K PD
90	LCD_DATA23	lcdif.DATA[23]	mqs.LEFT	ecspi1.MISO	csi.DATA[15]	weim.DATA[15]	gpio3.IO[28]	src.BT_CFG[31]	tpsmp.HDATA[1]	usdhc2.DATA3 [2)]	epdc.SDCE[3]		ALT5	100K PD

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X1 Pin	i.MX 6ULL Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ADC	Reset State	Pull
92	LCD_DATA22	lcdif.DATA[22]	mqs.RIGHT	ecspi1.MOSI	csi.DATA[14]	weim.DATA[14]	gpio3.IO[27]	src.BT_CFG[30]	tpsmp.HDATA[0]	usdhc2.DATA2 [2])	epdc.SDCE[2]		ALT5	100K PD
94	CSI_HSYNC [1])	csi.HSYNC	usdhc2.CMD [2])		i2c2.SCL	weim.LBA_B	gpio4.IO[20]	pwm8.OUT	tpsmp.HDATA[23]	uart6.CTS_B	esai.TX1		ALT5	Keeper
96	CSI_PIXCLK	csi.PIXCLK	usdhc2.WP [2])	rawnand.CE3_B	i2c1.SCL	weim.OE	gpio4.IO[18]	snvs_hp_wrapper.VIO_5	tpsmp.HDATA[21]	uart6.RX	esai.TX2_RX3		ALT5	Keeper
98	CSI_DATA05	csi.DATA[7]	usdhc2.DATA5 [2])		ecspi1.SS0	weim.AD[5]	gpio4.IO[26]	sai1.TX_BCLK	tpsmp.HDATA[29]	usdhc1.CD_B	esai.TX_CLK		ALT5	Keeper
100	UART3_CTS	uart3.CTS_B	enet2.RX_CLK	can1.TX	csi.DATA[10]	enet1.1588_EVENT1_IN	gpio1.IO[26]	anatop.USBPHY1_TSTI_TX_HIZ	sim_m.HADDR[1]	epit2.OUT			ALT5	Keeper
102	JTAG_TRST_B	sjc.TRSTB	gpt2.COMPARE3	sai2.TX_DATA	ccm.OUT2	pwm8.OUT	gpio1.IO[15]	anatop.24M_OUT					ALT0	47K PU
104	ENET1_RXER	enet1.RX_ER	uart7.RTS_B	pwm8.OUT	csi.DATA[23]	weim.CRE	gpio2.IO[7]	kpp.COL[3]	sim_m.HADDR[14]	gpt1.CAPTURE2	epdc.SDOEZ		ALT5	Keeper
106	JTAG_MOD	sjc.MOD	gpt2.CLK	spdif.OUT	anatop.ENET_REF_CLK_25M	ccm.PMIC_RDY	gpio1.IO[10]	sdma.EXT_EVENT[0]					ALT0	10K PD
138	SNVS_TAMPER8 [1])	snvs_lp_wrapper.TAMPER[8]					gpio5.IO[8]						ALT0	Keeper
140	NAND_ALE [3])	rawnand.ALE	usdhc2.RESET_B [2])	qspiA_DQS	pwm3.OUT	weim.ADDR[17]	gpio4.IO[10]	anatop.TESTO[10]	tpsmp.HDATA[12]	ecspi3.SS1			ALT5	Keeper
142	NAND_READY_B [3])	rawnand.READY_B	usdhc1.DATA4	qspiA_DATA[0]	ecspi3.SS0	weim.CS1_B	gpio4.IO[12]	anatop.TESTO[12]	tpsmp.HDATA[14]	uart3.TX			ALT5	Keeper
144	NAND_CE0_B [3])	rawnand.CE0_B	usdhc1.DATA5	qspiA_DATA[1]	ecspi3.SCLK	weim.DTACK_B	gpio4.IO[13]	anatop.TESTO[13]	tpsmp.HDATA[15]	uart3.RX			ALT5	Keeper
148	NAND_CLE [3])	rawnand.CLE	usdhc1.DATA7	qspiA_DATA[3]	ecspi3.MISO	weim.ADDR[16]	gpio4.IO[15]	anatop.TESTO[15]	tpsmp.HDATA[19]	uart3.RTS_B			ALT5	Keeper
178	ENET1_CRS_DV	enet1.RX_EN	uart5.RTS_B	osc32k.32K_OUT	csi.DATA[18]	can2.TX	gpio2.IO[2]	kpp.ROW[1]	sim_m.HADDR[9]	usdhc1.VSELECT	epdc.SDCE[6]		ALT5	Keeper
180	GPIO1_IO06	enet1.MDIO	enet2.MDIO	usb.OTG_PWR_WAKE	csi.MCLK	usdhc2.WP [2])	gpio1.IO[6]	ccm.WAIT	ccm.REF_EN_B	uart1.CTS_B		ADCx_IN6	ALT5	Keeper
184	GPIO1_IO07	enet1.MDC	enet2.MDC	usb.OTG_HOST_MODE	csi.PIXCLK	usdhc2.CD_B [2])	gpio1.IO[7]	ccm.STOP	ecspi1.TESTER_TRIGGER	uart1.RTS_B		ADCx_IN7	ALT5	Keeper
186	UART3_RTS	uart3.RTS_B	enet2.TX_ER	can1.RX	csi.DATA[11]	enet1.1588_EVENT1_OUT	gpio1.IO[27]	anatop.USBPHY2_TSTO_RX_HS_RXD	sim_m.HADDR[2]	wdog1.WDOG_B			ALT5	Keeper
188	ENET1_TXD0	enet1.TDATA[0]	uart5.CTS_B	anatop.24M_OUT	csi.DATA[19]	can2.RX	gpio2.IO[3]	kpp.COL[1]	sim_m.HADDR[10]	usdhc2.VSELECT [2])	epdc.SDCE[7]		ALT5	Keeper
190	SD1_CMD	usdhc1.CMD	gpt2.COMPARE1	sai2.RX_SYNC	spdif.OUT	weim.ADDR[19]	gpio2.IO[16]	sdma.EXT_EVENT[0]	tpsmp.HDATA[18]	usb.OTG1_PWR			ALT5	Keeper
192	SD1_DATA0	usdhc1.DATA0	gpt2.COMPARE3	sai2.TX_SYNC	can1.TX	weim.ADDR[21]	gpio2.IO[18]	ccm.OUT1	observe_mux.OUT[1]	anatop.OTG1_ID			ALT5	Keeper
194	UART4_RXD	uart4.RX	enet2.TDATA[3]	i2c1.SDA	csi.DATA[13]	csu.CSU_ALARM_AUT[1]	gpio1.IO[29]	anatop.USBPHY2_TSTO_PLL_CLK20DIV	sim_m.HADDR[4]	ecspi2.SS0	epdc.PWRCTRL[1]		ALT5	Keeper
196	UART4_TXD	uart4.TX	enet2.TDATA[2]	i2c1.SCL	csi.DATA[12]	csu.CSU_ALARM_AUT[2]	gpio1.IO[28]	anatop.USBPHY1_TSTO_PLL_CLK20DIV	sim_m.HADDR[3]	ecspi2.SCLK			ALT5	Keeper

[1]) This pin is not available on modules with Wi-Fi.
[2]) The USDHC2 function is not available on the Colibri iMX6ULL 1GB IT since the interface is used for the on-module eMMC
[3]) This pin is only available on the Colibri iMX6ULL 1GB IT
The Tamper function is not supported since it requires a different fusing of the SoC.

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5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
42, 84,108, 148,182,198, 200	3V3	I	3.3V main power supply	Use decoupling capacitors on all pins.
39, 41, 83, 109,147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I	RTC Power supply can be connected to a backup battery.	Connect this pin to 3.3V even if the internal RTC is not used.

The VCC_BATT input of the module (pin 40) powers the SNVS rail of the SoC. Besides the RTC and power management function, the i.MX 6ULL SoC uses this rail also as IO rail for the pins in the SNVS block (SNVS pins). Some of these interface pins are available on the SODIMM connector as regular GPIOs (SODIMM pin 43, 45, 93, 95, 105, 107, 127, 131, 137, and 138). Since the VCC_BATT on the Colibri standard is meant to be used as RTC battery input and not for powering IO rails, a power rail switch is added to the module. If the module is powered up, the VCC_BATT rail is connected to the 3.3V rail. Even though there is a diode between the VCC_BATT and the 3.3V rail, which makes sure the SNVS rail is also available if the module is not powered up, we highly recommend keeping the same circuit on the carrier board for the VCC_BATT as recommended in the Colibri Design Guide. This makes sure the carrier board is compatible with other Colibri modules.

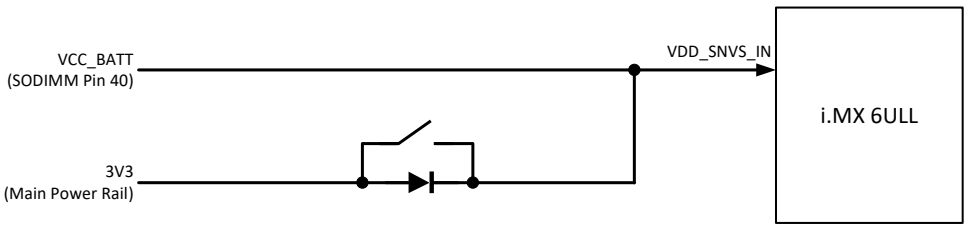


Figure 6: VCC_BATT Switching Circuit

5.1.2 Analog Supply

Table 5-2 Analog Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V Analog supply for ADC	Connect this pin **to a 3.3V supply**. For better ADC accuracy, we recommend filtering this supply separately from the digital supply. This pin is only connected to the ADC supply and the ADC reference input of the SoC. If ADC is not used, connect these pins to the regular 3V3 input supply.
9, 11	VSS_AUDIO	I	Analog Ground	Connect this pin to GND. This pin is connected to Digital GND on the Colibri iMX6ULL.

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5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
26	nRESET_EXT	I	Reset Input	This pin is active low and resets the Colibri module. There is a 100k Ohm pull-up on this pin.
87	nRESET_OUT	O	Reset Output	This pin is active low. This pin is driven low at boot up. This signal is an open-drain output which a 10k Ohm pull-up on the module. This reset is also connected to the SoC and peripheral reset inputs on the module.

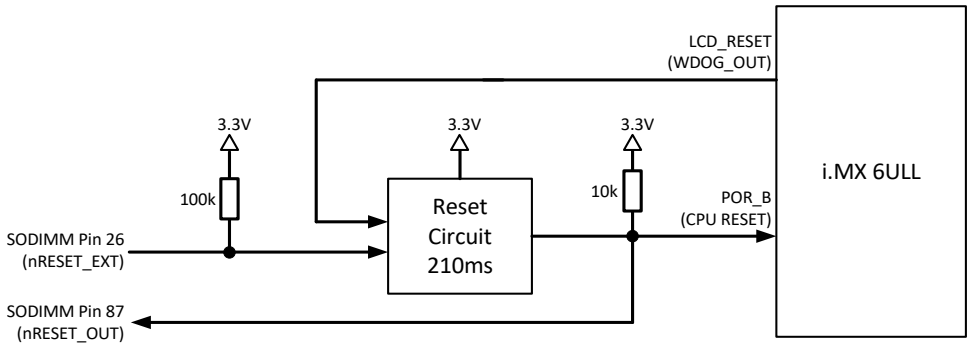


Figure 7: Reset Circuit

The i.MX 6ULL SoC features an integrated power management unit (PMU). There is no external power management IC (PMIC) on the module like on other Colibri modules. However, there is a reset circuit on the module, which handles the correct reset timings. The reset circuit has three different reset sources:

- Main power supply level: The reset circuit has a threshold of 2.93V (+/-2.5%). Below this threshold, the reset output is kept low. Rising above the threshold releases the reset after a timeout of typical 210ms
- nRESET_EXT: with the module edge connector pin 26, a reset cycle can be initiated. The reset is released after a timeout of 210ms
- SoC watchdog output: The SoC pin LCD_RESET is connected to the reset circuit. This pin is by default configured as watchdog output (global wdog). This allows using the internal watchdog to reset the system. To prevent system lock-ups, the maximum reset time is protected. The reset is released after around 300ms, even if the LCD_RESET signal is still kept low.

The typical reset time is 210ms (140ms – 280ms over the whole temperature range). The output of the circuit is an open drain with a 10k pull-up resistor on the module. The output goes to the power-on reset (POR_B) of the SoC and the peripheral devices on the module. The reset output signal is also available on the SODIMM pin 87 for the peripherals on the carrier board.

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. The GPIO functionality is configured by selecting the correct alternate function ALT5. All GPIO pins can be used as an interrupt source.

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5.2.1 Wakeup Source

The Colibri iMX6ULL uses different sleep modes. In principle, all GPIOs can be used to wake up the Colibri module from the System Idle, Low Power Idle, and Suspend state. More information about the different sleep modes can be found in section 6.

Even though there are many pins available with the wake functionally, it is recommended that, whenever possible, use pin 43 (WAKEUP Source<0>) and 45 (WAKEUP Source<1>). This ensures that the design is compatible with other Colibri modules.

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	Remarks
43	WAKEUP Source<0>, SDCard CardDetect	SNVS_TAMPER0	Preferred wakeup source
45	WAKEUP Source<1>	SNVS_TAMPER1	Preferred wakeup source

5.3 Ethernet

The Colibri iMX6ULL features a 10/100 Mbit/s Ethernet interface with Medium Dependent Interface (MDI). The PHY of this interface is located on the module. Therefore, only the magnetics and the connector are needed on the carrier board. The module features the Micrel KSZ8041 Fast Ethernet Transceiver as PHY, which is connected over RMII with the MAC in the NXP i.MX 6ULL. The MAC in the SoC features an accurate IEEE 1588 compliant timer for clock synchronization, which is commonly used in industrial automation applications.

Table 5-4 Ethernet Pins

X1 Pin#	Colibri STD Function	PHY Signal Name	I/O	Description
189	TXO+	TX+	O	100BASE-TX: Transmit + (Auto MDIX: Receive +)
187	TXO-	TX-	O	100BASE-TX: Transmit - (Auto MDIX: Receive -)
195	RXI+	RX+	I	100BASE-TX: Receive + (Auto MDIX: Transmit +)
193	RXI-	RX-	I	100BASE-TX: Receive - (Auto MDIX: Transmit -)
191	AGND_LAN	GND		Ethernet ground, on the module connected to common GND
183	LINK_AKT	LED0	O	Link activity indication LED
185	SPEED100	LED1	O	100Mbit/s indication LED

The Colibri iMX6ULL features a second Ethernet port. If this port is required, an additional PHY needs to be implemented on the carrier board. Since the MDIO configuration port signals are shared between the on-module and external Ethernet PHY, it is crucial to ensure that the two PHYs are not strapped to the same address. The MDIO interface of the Ethernet PHY on the module uses the address 00010. We recommend using the address 00001 for the external PHY.
The second MAC in the SoC can provide two different interface standards for the connection with the PHY:

- RMII: Reduced Media Independent Interface. This is the preferred mode for interfacing a 10/100 Mbit/s Ethernet PHY such as the KSZ8041.
- MII: Media Independent Interface. This is the second option for interfacing a 10/100 Mbit/s Ethernet PHY. This mode requires more data pins than the RMII, with the advantage of a more relaxed interface routing due to lower operating frequency.

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Table 5-5 RMII signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
55	PS2 SDA1	ENET1_RXD0	enet1.RDATA[0]	I	RMII_RXD0
63	PS2 SCL1	ENET1_RXD1	enet1.RDATA[1]	I	RMII_RXD1
104		ENET1_RXER	enet1.RX_ER	I	RMII_RXER
188	ADDRESS16	ENET1_TXD0	enet1.TDATA[0]	O	RMII_TXD0
73		ENET1_TXD1	enet1.TDATA[1]	O	RMII_TXD1
30	PWM<C>	ENET1_TXEN	enet1.TX_EN	O	RMII_TXEN
178	DATA30	ENET1_CRS_DV	enet1.RX_EN	O	RMII_TXEN
184	ADDRESS18	GPIO1_IO07;GPIO1_IO07	enet1.MDC;enet2.MDC	O	RMII_MDC **shared with PHY on the module**
180	DATA31	GPIO1_IO06;GPIO1_IO06	enet1.MDIO;enet2.MDIO	I/O	RMII_MDIO **shared with PHY on the module**
19	UART_C RXD	GPIO1_IO04	anatop.ENET_REF_CLK1	I/O	50MHz Reference clock that is provided from the MAC to the PHY or from the PHY to the MAC
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK			
8	Analog Input <0>	GPIO1_IO00			

Table 5-6 MII signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
34	UART_B RTS	UART2_RTS	enet1.COL	I	MII_COL
32	UART_B CTS	UART2_CTS	enet1.CRS	I	MII_CRS
55	PS2 SDA1	ENET1_RXD0	enet1.RDATA[0]	I	MII_RD0
63	PS2 SCL1	ENET1_RXD1	enet1.RDATA[1]	I	MII_RD1
33	UART_A RXD	UART1_TXD	enet1.RDATA[2]	I	MII_RD2
35	UART_A TXD	UART1_RXD	enet1.RDATA[3]	I	MII_RD3
25	UART_A CTS, Keypad_In<0>	UART1_CTS	enet1.RX_CLK	I	MII_RX_CLK
178	DATA30	ENET1_CRS_DV	enet1.RX_EN	I	MII_RX_DV
104		ENET1_RXER	enet1.RX_ER	I	MII_RX_ER
188	ADDRESS16	ENET1_TXD0	enet1.TDATA[0]	O	MII_TD0
73		ENET1_TXD1	enet1.TDATA[1]	O	MII_TD1
36	UART_B RXD	UART2_TXD	enet1.TDATA[2]	O	MII_TD2
38	UART_B TXD	UART2_RXD	enet1.TDATA[3]	O	MII_TD3
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK	enet1.TX_CLK	O	MII_TX_CLK
30	PWM<C>	ENET1_TXEN	enet1.TX_EN	O	MII_TX_EN
27	UART_A RTS	UART1_RTS	enet1.TX_ER	O	MII_TX_ER
184	ADDRESS18	GPIO1_IO07;GPIO1_IO07	enet1.MDC;enet2.MDC	O	MII_MDC **shared with PHY on the module**
180	DATA31	GPIO1_IO06;GPIO1_IO06	enet1.MDIO;enet2.MDIO	I/O	MII_MDIO **shared with PHY on the module**

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Each Ethernet MAC features a 4-channel IEEE 1588 timer. Each timer supports input capture and output comparison. The pins are available on the SODIMM module edge connector, but they are not compatible with other Colibri modules.

Table 5-7 IEEE 1588 timer signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
19	UART_C RXD	GPIO1_IO04	enet2.1588_EVENT0_IN	I	IEEE 1588 input capture signal for the on-module Ethernet PHY
25	UART_A CTS, Keypad_In<0>	UART1_CTS	enet2.1588_EVENT1_IN		
78	LCD RGB Data<4>	LCD_DATA04	enet2.1588_EVENT2_IN		
80	LCD RGB Data<6>	LCD_DATA06	enet2.1588_EVENT3_IN		
21	UART_C TXD	GPIO1_IO05	enet2.1588_EVENT0_OUT	O	IEEE 1588 output compare signal for the on-module Ethernet PHY
27	UART_A RTS	UART1_RTS	enet2.1588_EVENT1_OUT		
72	LCD RGB Data<5>	LCD_DATA05	enet2.1588_EVENT2_OUT		
46	LCD RGB Data<7>	LCD_DATA07	enet2.1588_EVENT3_OUT		
8	Analog Input <0>	GPIO1_IO00	enet1.1588_EVENT0_IN	I	IEEE 1588 input capture signal for the external Ethernet PHY
100	Keypad_Out<1>	UART3_CTS	enet1.1588_EVENT1_IN		
76	LCD RGB Data<0>	LCD_DATA00	enet1.1588_EVENT2_IN		
60	LCD RGB Data<2>	LCD_DATA02	enet1.1588_EVENT3_IN		
6	Analog Input <1>	GPIO1_IO01	enet1.1588_EVENT0_OUT	O	IEEE 1588 output compare signal for the external Ethernet PHY
186	ADDRESS17	UART3_RTS	enet1.1588_EVENT1_OUT		
70	LCD RGB Data<1>	LCD_DATA01	enet1.1588_EVENT2_OUT		
58	LCD RGB Data<3>	LCD_DATA03	enet1.1588_EVENT3_OUT		

5.4 Wi-Fi and Bluetooth

The Colibri iMX6ULL is available as a version with on-module Wi-Fi and Bluetooth interface. The additional "WB" in the product name indicates that this version features Wi-Fi and Bluetooth. These Colibri module versions are making use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from Azurewave.

Features:

- Wi-Fi 802.11ac/a/b/g/n
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps (theoretical maximum speed of Wi-Fi module, actual speed is limited by SDIO interface)
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5.0 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for the dual external antennas in 2x2 configuration, compatible with IPX/IPEX connector MHF4 series.
- Pre-certified for CE (Europe), FCC (United States), and IC (Canada)

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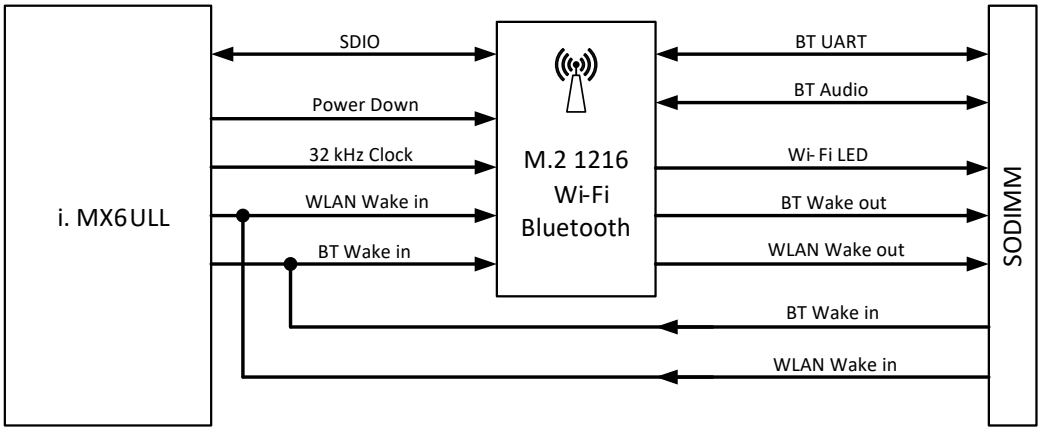


Figure 8: Wi-Fi and Bluetooth block diagram

The Wi-Fi and Bluetooth module is connected over a 4-bit SDIO interface with the i.MX 6ULL SoC. It uses the USDHC2 instance of the SoC. Therefore, this interface is not available on the module edge connector for modules with Wi-Fi/Bluetooth functions. On the Colibri iMX6ULL, the interface supports only a 3.3V logic level. 1.8V is not supported.

Table 5-8 Signal Pins between AW-CM276NF and i.MX 6ULL

AW-CM276NF Pin Name	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
SD_CMD	CSI_HSYNC	usdhc2.CMD	I/O	4-bit SDIO interface for Wi-Fi and Bluetooth
SD_DAT[0]	CSI_DATA00	usdhc2.DATA0	I/O	
SD_DAT[1]	CSI_DATA01	usdhc2.DATA1	I/O	
SD_DAT[2]	CSI_DATA02	usdhc2.DATA2	I/O	
SD_DAT[3]	CSI_DATA03	usdhc2.DATA3	I/O	
SD_CLK	CSI_VSYNC	usdhc2.CLK	I	
PDn	BOOT_MODE1	gpio5.IO[11]	I	0 = full power-down, 1 = normal mode
SLP_CLK	GPIO1_IO03	osc32k.32K_OUT	I	32.768kHz sleep clock input for low power operation
GPIO[15]/ TMS/ Host Wake WLAN	SNVS_TAMPER8	gpio5.IO[8]	I	HOST_WKUP_WLAN: SoC to AW-CM276NF Wi-Fi Wakeup, the signal is also available on the SODIMM connector
GPIO[12]/ UART Host Wake BT	SNVS_TAMPER6	gpio5.IO[6]	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup, the signal is also available on the SODIMM connector

The AW-CM276NF features four wake signals. Two are input signals (one for the Wi-Fi and one for Bluetooth), allowing for waking up the radio. These wake signals are connected to the SoC but are also available on the module edge connector. The Wi-Fi and Bluetooth receiver can use the additional two output signals to wake up the system. These signals are only available at the module edge connector. If the SoC needs to be woken up, route these pins back to the regular wake input signals of the Colibri module.

Besides the SDIO interface for Wi-Fi and Bluetooth communication, the AW-CM276NF also features a dedicated UART and digital audio (I2S) interface for the Bluetooth protocol. The interface pins are available on the module edge connector. However, the AW-CM276NF is strapped for using only the SDIO interface. If you are planning to use the UART or I2S interface, please contact your local Toradex sales team

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Table 5-9 SODIMM Signal Pins of the AW-CM276NF

X1 Pin#	Colibri STD Function	AW-CM276NF Pin Name	I/O	Description
111	ADDRESS0	GPIO[8]/UART_SOUT	O	BT UART mode: TX data
113	ADDRESS1	GPIO[9]/UART_SIN	I	BT UART mode: RX data
115	ADDRESS2	GPIO[10]/UART_CTSn	I	BT UART mode: Clear to send
117	ADDRESS3	GPIO[11]/UART_RTSn	O	BT UART mode: Request to send
119	ADDRESS4	GPIO[22]/PCIE_W_DISABLEn	I	PCIE Wireless Disable Input (active low)
121	ADDRESS5	GPIO[14]/TCK/ WLAN Wake Host	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output
123	ADDRESS6	GPIO[13]/BT IRQ(O)	O	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output
125	ADDRESS7	GPIO[2]/WLAN_LED	O	Wi-Fi activity LED
112	ADDRESS9	GPIO[6]/PCM_CLK	I/O	PCM clock signal for audio interface
114	ADDRESS10	GPIO[7]/PCM_SYNC	I/O	PCM sync signal for audio interface
116	ADDRESS11	GPIO[4]/PCM_DIN	I	PCM data input for audio interface
118	ADDRESS12	GPIO[5]/PCM_DOUT	O	PCM data output for audio interface
120	ADDRESS13	GPIO[15]/ TMS/ Host Wake WLAN	I	HOST_WKUP_WLAN: SoC to AW-CM276NF Wi-Fi Wakeup, the signal is also connected to SoC
122	ADDRESS14	GPIO[12]/ UART Host Wake BT	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup, the signal is also connected to SoC
126	DQM0	GPIO3/BT_LED	O	Bluetooth activity LED

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. Please get in touch with Toradex about certifying the Colibri iMX6ULL WB: Contact your local sales office or support@toradex.com.

5.5 USB

The Colibri iMX6ULL provides two USB 2.0 High-Speed (480 Mbit/s). Even though the two ports are identical and could be both used as host and client, it is recommended to use only the USBC port as a dual-use interface. The USBH port should be used as a host-only in order to be compatible with other Colibri modules. The USBC controller is also used for the serial loader mode (recovery mode). For more information, see section 6.

5.5.1 USB Data Signal

Table 5-10 USB Data Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	I/O	Description
143	USBC_P	USB_OTG1_DP	I/O	Differential Signal for the shared USB Host / Client port
145	USBC_N	USB_OTG1_DN	I/O	
139	USBH_P	USB_OTG2_DP	I/O	Differential Signal for USB Host port
141	USBH_N	USB_OTG2_DN	I/O	

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5.5.2 USB Control Signals

Table 5-11 USB OTG Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
135	SPDIF_IN	UART3_TXD	anatop.OTG1_ID	I	USB OTG ID
8	Analog Input <0>	GPIO1_IO00			Alternative instances of ID pin, incompatible with other Colibri modules.
192	SDCard DAT<0>	SD1_DATA0			
137	USB Client Cable Detect,SPDIF_OUT	SNVS_TAMPER2	gpio5.IO[2]	I	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant Even though this is just a regular GPIO, it is recommended to use this one to be compatible with the Toradex BSP

The Colibri iMX6ULL module does not support true OTG, but the interface can be configured as host or client. Due to compatibility with other Colibri modules, the current evaluation board and the other Toradex carrier board do not use the USB OTG ID pin to detect whether a Type A or Type B cable is plugged in. Instead, the VBUS is used for detecting the Host or Client mode. We recommend implementing the same circuit on the evaluation board to ensure the design is compatible with the provided Toradex OS images (BSP).

If you use the USB Host function, you need to generate the 5V USB supply voltage on your carrier board. The Colibri iMX6ULL provides two optional signals for USB power supply control. However, the use of these signals is not mandatory. We recommend using the following pins to ensure the best possible compatibility.

Table 5-12 USB Power Control Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
129	USB Host Power Enable	GPIO1_IO02	usb.OTG2_PWR	O	This pin enables the external USB voltage supply
131	USB Host Over-Current Detect	SNVS_TAMPER5	gpio5.IO[5]	I	USB overcurrent, this pin can Signal an overcurrent condition in the USB supply

5.6 Display

5.6.1 Parallel RGB LCD interface

The Colibri iMX6ULL provides one parallel LCD interface on the SODIMM connector. It supports up to 24-bit color per pixel. Only the 18-bit mode is ensured to be compatible with other Colibri modules. The additional signals required for the 24-bit interface are located as an alternate function of the SPI interface. These pins can only be used if the standard function (SPI) is not used. We recommend using the LCD interface of the Colibri iMX6ULL only in the 18-bit mode.

Features:
- Up to 1366x768 resolution at 60Hz
- Up to 24-bit color (18-bit recommended)
- Supports parallel TTL displays and smart displays
- Max pixel clock 85MHz

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Table 5-13 Standard Parallel RGB LCD Interface Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	I/O	24-bit RGB Interface	18-bit RGB Interface	16-bit RGB Interface
76	LCD RGB Data<0>	LCD_DAT0	O	B0	B0	B0
70	LCD RGB Data<1>	LCD_DAT1	O	B1	B1	B1
60	LCD RGB Data<2>	LCD_DAT2	O	B2	B2	B2
58	LCD RGB Data<3>	LCD_DAT3	O	B3	B3	B3
78	LCD RGB Data<4>	LCD_DAT4	O	B4	B4	B4
72	LCD RGB Data<5>	LCD_DAT5	O	B5	B5	G0
80	LCD RGB Data<6>	LCD_DAT6	O	B6	G0	G1
46	LCD RGB Data<7>	LCD_DAT7	O	B7	G1	G2
62	LCD RGB Data<8>	LCD_DAT8	O	G0	G2	G3
48	LCD RGB Data<9>	LCD_DAT9	O	G1	G3	G4
74	LCD RGB Data<10>	LCD_DAT10	O	G2	G4	G5
50	LCD RGB Data<11>	LCD_DAT11	O	G3	G5	R0
52	LCD RGB Data<12>	LCD_DAT12	O	G4	R0	R1
54	LCD RGB Data<13>	LCD_DAT13	O	G5	R1	R2
66	LCD RGB Data<14>	LCD_DAT14	O	G6	R2	R3
64	LCD RGB Data<15>	LCD_DAT15	O	G7	R3	R4
57	LCD RGB Data<16>	LCD_DAT16	O	R0	R4	
61	LCD RGB Data<17>	LCD_DAT17	O	R1	R5	
29	UART_A DSR	LCD_DAT18	O	R2		
37	UART_A RI, Keypad_In<4>	LCD_DAT19	O	R3		
88	SPI CLK	LCD_DAT20	O	R4		
86	SPI CS	LCD_DAT21	O	R5		
92	SPI TXD	LCD_DAT22	O	R6		
90	SPI RXD	LCD_DAT23	O	R7		
44	LCD RGB DE	LCD_ENABLE	O	Data Enable (other names: Output Enable, L_BIAS)		
68	LCD RGB HSYNC	LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL)		
82	LCD RGB VSYNC	LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)		
56	LCD RGB PCLK	LCD_CLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		

Many applications also require some signals to control the backlight or display enabling. You can use any of the free GPIOs for these functions. However, we recommend using the same signals as used on our standard carrier boards to ensure minimal software configuration overhead. PWM capable signals can be used to control the backlight brightness on many display panels - see section 5.11.

5.6.2 Electrophoretic Display Controller (EPDC)

The i.MX 6ULL SoC versions used on the regular Colibri iMX6ULL modules do not feature an EDPC interface.

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5.6.3 LVDS

The Colibri iMX6ULL does not have a native LVDS interface. However, it is possible to use the parallel LCD port with an LVDS transmitter. The Colibri Evaluation board provides a reference design for an LVDS interface implementation.

5.6.4 HDMI

The Colibri iMX6ULL does not have a native HDMI interface. However, it is possible to implement a parallel RGB to HDMI converter on the carrier board.

5.6.5 Analog VGA

The Colibri iMX6ULL does not have a native Analog VGA interface. However, it is possible to implement a VGA interface on the carrier board using a VGA DAC. The Colibri Evaluation board features a reference design for such a VGA DAC.

5.7 External Memory Bus

The Colibri iMX6ULL features an external memory bus. NXP refers to this bus in its documentation as the "External Interface Module" EIM. No internal devices are connected to the external memory bus; hence, the memory bus configuration can be optimized for any application-specific requirement without restrictions. The external memory bus is typically used to connect high-speed devices like FPGAs, DSPs, secondary Ethernet controllers, CAN controllers, etc.

The External Memory Bus on the Colibri iMX6ULL is not compatible with any other Colibri module since the required interface pins are not located at the standard Colibri position. The bus is only available as alternate functions of other interfaces such as the parallel RGB LCD, the SD card, and the camera interface. Some bus signals are not available on the module edge connector since they are located at the NAND interface, which is used to boot the module.

Features:
- 16-bit or 8-bit data width (not multiplexed with address lines)
- Up to 15-bit address bus width (non-consecutive: A0 to A7 and A18 to A24)
- Asynchronous and burst mode
- Maximum main clock frequency of 133 MHz
- Up to 3 chip select signals

Table 5-14 Non-Multiplexed Signal Mapping

Peripheral Signals	8-Bit		16-Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001
A[7:0]	weim.AD[7:0]	weim.AD[7:0]	weim.AD[7:0]
A[26:18]	weim.ADDR[24:18]	weim.ADDR[24:18]	weim.ADDR[24:18]
D[7:0]	weim.DATA[7:0]	weim.DATA[15:8]	weim.DATA[7:0]
D[15:8]			weim.DATA[15:8]

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5.7.1 Memory Bus Signals

Table 5-15 Memory Bus Signals

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
101	Camera Input Data<2>	CSI_DATA00	weim.AD[0]	O	Address and data bits 3 to 0 **not connected on modules with Wi-Fi**
103	Camera Input Data<3>	CSI_DATA01	weim.AD[1]	O	
79	Camera Input Data<4>	CSI_DATA02	weim.AD[2]	O	
97	Camera Input Data<5>	CSI_DATA03	weim.AD[3]	O	
69	PS2 SCL2	CSI_DATA04	weim.AD[4]	O	Address and data bits 7 to 3
98	Camera Input Data<1>	CSI_DATA05	weim.AD[5]	O	
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06	weim.AD[6]	O	
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07	weim.AD[7]	O	
133		NAND_CE1_B	weim.ADDR[18]	O	Address and data bits 24 to 18
190	SDCard CMD	SD1_CMD	weim.ADDR[19]	O	
47	SDCard CLK	SD1_CLK	weim.ADDR[20]	O	
192	SDCard DAT<0>	SD1_DATA0	weim.ADDR[21]	O	
49	SDCard DAT<1>	SD1_DATA1	weim.ADDR[22]	O	
51	SDCard DAT<2>	SD1_DATA2	weim.ADDR[23]	O	
53	SDCard DAT<3>	SD1_DATA3	weim.ADDR[24]	O	
62	LCD RGB Data<8>	LCD_DATA08	weim.DATA[0]	I/O	Data bits 15 to 0
48	LCD RGB Data<9>	LCD_DATA09	weim.DATA[1]	I/O	
74	LCD RGB Data<10>	LCD_DATA10	weim.DATA[2]	I/O	
50	LCD RGB Data<11>	LCD_DATA11	weim.DATA[3]	I/O	
52	LCD RGB Data<12>	LCD_DATA12	weim.DATA[4]	I/O	
54	LCD RGB Data<13>	LCD_DATA13	weim.DATA[5]	I/O	
66	LCD RGB Data<14>	LCD_DATA14	weim.DATA[6]	I/O	
64	LCD RGB Data<15>	LCD_DATA15	weim.DATA[7]	I/O	
57	LCD RGB Data<16>	LCD_DATA16	weim.DATA[8]	I/O	
61	LCD RGB Data<17>	LCD_DATA17	weim.DATA[9]	I/O	
29	UART_A DSR	LCD_DATA18	weim.DATA[10]	I/O	
37	UART_A RI, Keypad_In<4>	LCD_DATA19	weim.DATA[11]	I/O	
88	SPI CLK	LCD_DATA20	weim.DATA[12]	I/O	
86	SPI CS	LCD_DATA21	weim.DATA[13]	I/O	
92	SPI TXD	LCD_DATA22	weim.DATA[14]	I/O	
90	SPI RXD	LCD_DATA23	weim.DATA[15]	I/O	
59	PWM<A>,Camera Input Data<7>	NAND_WP_B	weim.BCLK	O	Burst Clock
104		ENET1_RXER	weim.CRE	O	CRE/PS signal for CellularRAM memory

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X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
75	Camera Input MCLK	CSI_MCLK	weim.CS0_B	O	Chip select signals
56	LCD RGB PCLK	LCD_CLK	weim.CS2_B	O	
44	LCD RGB DE	LCD_ENABLE	weim.CS3_B	O	
96	Camera Input PCLK	CSI_PIXCLK	weim.OE	O	Output Enable
81	Camera Input VSYNC	CSI_VSYNC	weim.RW	O	Write Enable **not connected on modules with Wi-Fi**
28	PWM<B>	NAND_DQS	weim.WAIT	I	Ready/Busy/Wait signal

5.8 I²C

The NXP i.MX 6ULL SoC features four I²C controllers, up to three of which can be used externally. They implement the I²C V2.1 specification. All of them can be used in master or slave mode. The port i2c2 is used for the touch controller on the module and is therefore not available externally. Port i2c1 is available as standard I²C on the module connector. The ports i2c3 and i2c4 are only available as alternate functions.

Features:
- Supports 100kbit/s and fast mode 400kbit/s data transfer
- Multi-master operation
- Software-selectable acknowledge bit
- Interrupt driven, byte-by-byte data transfer
- Start and stop signal generation and detection
- Repeated start signal generation
- Acknowledge bit generation and detection
- Bus-busy detection
- Calling address identification interrupts

Many low-speed devices use I²C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I²C Bus can also be used to communicate with SMB (System Management Bus) devices.

Table 5-16 I²C Signals (Colibri family compatible interface)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
194	I2C SDA	UART4_RXD	i2c1.SDA	I/O	Open Drain Data Signal Port 1
196	I2C SCL	UART4_TXD	i2c1.SCL	I/O	Clock Signal Port 1

Table 5-17 Alternate I²C Signals (additional and incompatible with other Colibri family modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
75	Camera Input MCLK	CSI_MCLK	i2c1.SDA	I/O	Alternate Open Drain Data Signal Port 1
89	nWE	GPIO1_IO03			Alternate Open Drain Data Signal Port 1, **not connected on modules with Wi-Fi**
129	USB Host Power Enable	GPIO1_IO02	i2c1.SCL	I/O	Alternate Clock Signal Port 1
96	Camera Input PCLK	CSI_PIXCLK			
35	UART_A TXD	UART1_RXD	i2c3.SDA	I/O	Open Drain Data Signal Port 3
76	LCD RGB Data<0>	LCD_DATA00			

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X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
33	UART_A RXD	UART1_TXD	i2c3.SCL	I/O	Clock Signal Port 3
70	LCD RGB Data<1>	LCD_DATA01			
38	UART_B TXD	UART2_RXD	i2c4.SDA	I/O	Open Drain Data Signal Port 4
60	LCD RGB Data<2>	LCD_DATA02			
36	UART_B RXD	UART2_TXD	i2c4.SCL	I/O	Clock Signal Port 4
58	LCD RGB Data<3>	LCD_DATA03			

5.8.1 Real-Time Clock (RTC) recommendation

The Colibri iMX6ULL module features an RTC circuit, which is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. The RTC is sourced from the VCC_BATT (pin 40) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found on the developer page https://developer.toradex.com/knowledge-base/imx6ull-power-consumption). Therefore, a standard lithium coin cell battery can be drained faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the module's standard I²C interface (pin 194/196) and source the VCC_BACKUP pin from the 3.3V rail that also sources the main module rail. A suitable reference schematic can be found in the schematic diagram of the Colibri evaluation board. See also section 6.2.

5.9 UART

The Colibri iMX6ULL provides up to eight serial UART interfaces. Three of them are available on dedicated UART pins, which are compatible with other Colibri modules. The other five UARTs are only available as an alternate function. These UARTs are incompatible with other Colibri modules. Therefore, the additional five UARTs should only be used if compatibility with other Colibri modules is not required and more than the three UARTs are required.

The UART_A interface of the Colibri is defined as a full-featured UART. Unfortunately, the NXP i.MX 6ULL SoC does not feature the DTR, DSR, DCD, and RI as dedicated signals. Regular GPIO pins are located on these SODIMM pins.

The UART_A is used as a standard debug interface for the Toradex Embedded Linux and Windows Embedded Compact operating systems. It is recommended that at least this port's RXD and TXD lines are kept accessible for system debugging.

The UARTs of the i.MX 6ULL can be configured either in the DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode changes the direction of all UART pins (data and all control signals). To ensure compatibility with the entire Colibri family, UARTs need to be configured in DTE mode.

Attention should be paid to the names of the i.MX 6ULL data signals. In DTE mode, the UARTx_RX_DATA port transmits data from the SoC while the UARTx_TX_DATA port receives it. Therefore, the RX and TX signals need to be swapped. In the following signal descriptions, the port direction is always described for DTE mode.

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UART Features:
- High-speed TIA/EIA-232F compatible (up to 5 Mbit/s)
- IrDA-compatible (up to 115.2kbit/s)
- 7 or 8 data bits (9 bit for RS485)
- 1 or 2 stop bits
- Optional parity bit (even or odd)
- Hardware flow control
- Auto-detect baud rate (up to 115.2kbit/s)
- 32 entries FIFO for receiving and transmitting

Table 5-18 UART_A Signal Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
33	UART_A RXD	UART1_TXD	uart1.TX	I	Received Data
35	UART_A TXD	UART1_RXD	uart1.RX	O	Transmitted Data
27	UART_A RTS	UART1_RTS	uart1.RTS_B	O	Request to Send
25	UART_A CTS, Keypad_In<0>	UART1_CTS	uart1.CTS_B	I	Clear to Send
23	UART_A DTR	JTAG_TDO	gpio1.IO[12]	O	GPIO only, DTR needs to be emulated
29	UART_A DSR	LCD_DATA18	gpio3.IO[23]	I	GPIO only, DSR needs to be emulated
31	UART_A DCD	JTAG_TDI	gpio1.IO[13]	I	GPIO only, DCD needs to be emulated
37	UART_A RI, Keypad_In<4>	LCD_DATA19	gpio3.IO[24]	I	GPIO only, RI needs to be emulated

Table 5-19 UART_B Signal Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
36	UART_B RXD	UART2_TXD	uart2.TX	I	Received Data
38	UART_B TXD	UART2_RXD	uart2.RX	O	Transmitted Data
34	UART_B RTS	UART2_RTS	uart2.RTS_B	O	Request to Send
32	UART_B CTS	UART2_CTS	uart2.CTS_B	I	Clear to Send

Table 5-20 UART_C Signal Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
19	UART_C RXD	GPIO1_IO04	uart5.TX	I	Received Data
21	UART_C TXD	GPIO1_IO05	uart5.RX	O	Transmitted Data

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Table 5-21 Signal Pins of additional UART Ports

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
135	SPDIF_IN	UART3_TXD	uart3.TX	I	Received Data
77		UART3_RXD	uart3.RX	O	Transmitted Data
186	ADDRESS17	UART3_RTS	uart3.RTS_B	O	Request to Send
100	Keypad_Out<1>	UART3_CTS	uart3.CTS_B	I	Clear to Send
133		NAND_CE1_B			
56	LCD RGB PCLK	LCD_CLK	uart4.TX	I	Received Data
196	I2C SCL	UART4_TXD			
44	LCD RGB DE	LCD_ENABLE	uart4.RX	O	Transmitted Data
194	I2C SDA	UART4_RXD			
55	PS2 SDA1	ENET1_RXD0	uart4.RTS_B	O	Request to Send
82	LCD RGB VSYNC	LCD_VSYNC			
63	PS2 SCL1	ENET1_RXD1	uart4.CTS_B	I	Clear to Send
68	LCD RGB HSYNC	LCD_HSYNC			
75	Camera Input MCLK	CSI_MCLK	uart6.TX	I	Received Data
96	Camera Input PCLK	CSI_PIXCLK	uart6.RX	O	Transmitted Data
30	PWM<C>	ENET1_TXEN	uart6.RTS_B	O	Request to Send
81	Camera Input VSYNC	CSI_VSYNC			Request to Send **not connected on modules with Wi-Fi**
73		ENET1_TXD1	uart6.CTS_B	I	Clear to Send
94	Camera Input HSYNC	CSI_HSYNC			Clear to Send **not connected on modules with Wi-Fi**
57	LCD RGB Data<16>	LCD_DATA16	uart7.TX	I	Received Data
61	LCD RGB Data<17>	LCD_DATA17	uart7.RX	O	Transmitted Data
46	LCD RGB Data<7>	LCD_DATA07	uart7.RTS_B	O	Request to Send
104		ENET1_RXER			
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK	uart7.CTS_B	I	Clear to Send
80	LCD RGB Data<6>	LCD_DATA06			
88	SPI CLK	LCD_DATA20	uart8.TX	I	Received Data
86	SPI CS	LCD_DATA21	uart8.RX	O	Transmitted Data
72	LCD RGB Data<5>	LCD_DATA05	uart8.RTS_B	O	Request to Send
78	LCD RGB Data<4>	LCD_DATA04	uart8.CTS_B	I	Clear to Send

These UART ports are only available as alternate functions. Compatibility with other Colibri modules cannot be guaranteed, as they are not standard Colibri module interfaces.

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Table 5-22 Alternate UART Signals (additional and incompatible with other Colibri family modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
129	USB Host Power Enable	GPIO1_IO02	uart1.TX	I	Alternate Received Data for UART_A
89	nWE	GPIO1_IO03	uart1.RX	O	Alternate Transmitted Data for UART_A **not connected on modules with Wi-Fi**
77		UART3_RXD	uart2.RTS_B	O	Alternate Request to Send for UART_B
135	SPDIF_IN	UART3_TXD	uart2.CTS_B	I	Alternate Clear to Send for UART_B
33	UART_A RXD	UART1_TXD	uart5.TX	I	Alternate Received Data for UART_C
101	Camera Input Data<2>	CSI_DATA00			Alternate Received Data for UART_C **not connected on modules with Wi-Fi**
35	UART_A TXD	UART1_RXD	uart5.RX	O	Alternate Transmitted Data for UART_C
103	Camera Input Data<3>	CSI_DATA01			Alternate Transmitted Data for UART_C **not connected on modules with Wi-Fi**
4	Analog Input <2>	GPIO1_IO08	uart5.RTS_B	O	Request to Send for UART_C
27	UART_A RTS	UART1_RTS			
178	DATA30	ENET1_CRS_DV			
79	Camera Input Data<4>	CSI_DATA02			Request to Send for UART_C **not connected on modules with Wi-Fi**
2	Analog Input <3>	GPIO1_IO09	uart5.CTS_B	I	Clear to Send for UART_C
25	UART_A CTS, Keypad_In<0>	UART1_CTS			
188	ADDRESS16	ENET1_TXD0			
97	Camera Input Data<5>	CSI_DATA03			Clear to Send for UART_C **not connected on modules with Wi-Fi**

5.10 SPI

The i.MX 6ULL provides four SPI controllers (which are called Enhanced Configurable SPI, ECSPI in the reference manual), of which only three are available on the module edge connector. The module with Wi-Fi features only two SPI interfaces on the edge connector.

One SPI interface is available as the standard Colibri module interface. This interface is compatible with other Colibri modules. The other SPI interfaces are available as alternate functions. These interfaces are incompatible with other Colibri modules. Please use the standard Colibri SPI interface first before using others.

The SPI ports operate at up to 52 Mbps and provide full-duplex, synchronous, serial communication between the Colibri module and internal or external peripheral devices. Each SPI port consists of four signals; clock, chip select (frame), data in, and data out. There are additional chip select signals available as alternate functions to support multiple peripherals.

Features:
- Up to 52 Mbps
- 32-bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable
- Simultaneous receive and transmit
- DMA support

Each SPI channel supports four different modes of the SPI protocol:

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Table 5-23 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock is positive polarity, and the data is latched on the positive edge of the SCK
1	0	1	The clock is positive polarity, and the data is latched on the negative edge of the SCK
2	1	0	The clock is negative polarity, and the data is latched on the positive edge of the SCK
4	1	1	The clock is negative polarity, and the data is latched on the negative edge of the SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCDs require configuration over SPI before being driven via the RGB or LVDS interface.

Table 5-24 SPI Signals (Colibri family compatible interface)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
92	SPI TXD	LCD_DATA22	ecspi1.MOSI	O	Master Output, Slave Input
90	SPI RXD	LCD_DATA23	ecspi1.MISO	I	Master Input, Slave Output
86	SPI CS	LCD_DATA21	ecspi1.SS0	O	Slave Select
88	SPI CLK	LCD_DATA20	ecspi1.SCLK	O	Serial Clock

Table 5-25 SPI Signals (additional and incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
133		NAND_CE1_B	ecspi3.MOSI	O	Master Output, Slave Input
32	UART_B CTS	UART2_CTS			
34	UART_B RTS	UART2_RTS	ecspi3.MISO	I	Master Input, Slave Output
36	UART_B RXD	UART2_TXD	ecspi3.SS0	O	Slave Select 0
38	UART_B TXD	UART2_RXD	ecspi3.SCLK	O	Serial Clock
59	PWM<A>,Camera Input Data<7>	NAND_WP_B	ecspi3.RDY	I	Data ready signal
79	Camera Input Data<4>	CSI_DATA02	ecspi2.MOSI	O	Master Output, Slave Input **not connected on modules with Wi-Fi**
97	Camera Input Data<5>	CSI_DATA03	ecspi2.MISO	I	Master Input, Slave Output **not connected on modules with Wi-Fi**
103	Camera Input Data<3>	CSI_DATA01	ecspi2.SS0	O	Slave Select 0 **not connected on modules with Wi-Fi**
194	I2C SDA	UART4_RXD			Slave Select 0
68	LCD RGB HSYNC	LCD_HSYNC	ecspi2.SS1	O	Slave Select 1
82	LCD RGB VSYNC	LCD_VSYNC	ecspi2.SS2	O	Slave Select 2
101	Camera Input Data<2>	CSI_DATA00	ecspi2.SCLK	O	Serial Clock **not connected on modules with Wi-Fi**
196	I2C SCL	UART4_TXD			Serial Clock
44	LCD RGB DE	LCD_ENABLE	ecspi2.RDY	I	Data ready signal

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Table 5-26 Alternate Signals of main SPI (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06	ecspi1.MOSI	O	Alternate Master Output, Slave Input
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07	ecspi1.MISO	I	Alternate Master Input, Slave Output
98	Camera Input Data<1>	CSI_DATA05	ecspi1.SS0	O	Alternate Slave Select 0
72	LCD RGB Data<5>	LCD_DATA05	ecspi1.SS1	O	Additional Slave Select 1
80	LCD RGB Data<6>	LCD_DATA06	ecspi1.SS2	O	Additional Slave Select 2
46	LCD RGB Data<7>	LCD_DATA07	ecspi1.SS3	O	Additional Slave Select 3
69	PS2 SCL2	CSI_DATA04	ecspi1.SCLK	O	Alternate Serial Clock
52	LCD RGB Data<12>	LCD_DATA12	ecspi1.RDY	I	Additional Data ready signal

5.11 PWM (Pulse Width Modulation)

The Colibri iMX6ULL features a dedicated Pulse Width Modulator (PWM) with eight channels. Four of these eight channels are located as standard Colibri interface. For compatibility reasons, please use these pins first. Each PWM channel features a 16-bit up-counter with clock source selection. There is a 16-bit 4 level deep FIFO available to minimize the interrupt overhead. There is a 12-bit prescaler available for dividing the clock.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights, or servo motors.

Table 5-27 PWM Interface Signals

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Remarks
59	PWM<A>,Camera Input Data<7>	NAND_WP_B	pwm4.OUT	O	PWM Output 1
28	PWM<B>	NAND_DQS	pwm5.OUT	O	PWM Output 2
30	PWM<C>	ENET1_TXEN	pwm6.OUT	O	PWM Output 3
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK	pwm7.OUT	O	PWM Output 4

Table 5-28 Locations of additional PWM Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Remarks
102		JTAG_TRST_B	pwm8.OUT	O	Additional PWM Output
104		ENET1_RXER			
94	Camera Input HSYNC	CSI_HSYNC			Additional PWM Output **not connected on modules with Wi-Fi**
4	Analog Input <2>	GPIO1_IO08	pwm1.OUT	O	Additional PWM Output
55	PS2 SDA1	ENET1_RXD0			
76	LCD RGB Data<0>	LCD_DATA00			

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X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Remarks
2	Analog Input <3>	GPIO1_IO09	pwm2.OUT	O	Additional PWM Output
63	PS2 SCL1	ENET1_RXD1			
70	LCD RGB Data<1>	LCD_DATA01			
19	UART_C RXD	GPIO1_IO04	pwm3.OUT	O	Additional PWM Output
60	LCD RGB Data<2>	LCD_DATA02			

Table 5-29 Alternate Locations of main PWM Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Remarks
21	UART_C TXD	GPIO1_IO05	pwm4.OUT	O	Alternate Pin for PWM Output 1
58	LCD RGB Data<3>	LCD_DATA03			
29	UART_A DSR	LCD_DATA18	pwm5.OUT	O	Alternate Pin for PWM Output 2
73		ENET1_TXD1			
31	UART_A DCD	JTAG_TDI	pwm6.OUT	O	Alternate Pin for PWM Output 3
37	UART_A RI, Keypad_In<4>	LCD_DATA19			
99	nPWE	JTAG_TCK	pwm7.OUT	O	Alternate Pin for PWM Output 4
81	Camera Input VSYNC	CSI_VSYNC			Alternate Pin for PWM Output 4 **not connected on modules with Wi-Fi**

5.12 OWR (One-Wire)

The Colibri iMX6ULL does not feature a One-Wire interface.

5.13 SD/MMC

The i.MX 6ULL SoC Dual provides two SDIO interfaces. One interface is available as a standard interface, which is compatible with other Colibri modules. The second interface (USDHC2) is used for the Wi-Fi/Bluetooth module or the eMMC on the Colibri iMX6ULL 1GB IT. On modules without Wi-Fi and eMMC, the second SDIO interface is also available on the module edge connector pins. Since this interface is provided as an alternate function, it is not compatible with other modules belonging to different Colibri product groups. This secondary interface can be used with up to 8 data bits, while the standard interface is only available with 4-bit.

For modules with Wi-Fi and Bluetooth interface, there is no second SDIO port available since it is used for interfacing the Wi-Fi/Bluetooth card with the SoC.

The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards, and eMMC devices. The controllers can act as both master and slave simultaneously.

The Colibri iMX6ULL supports UHS-I, which allows up to 104 Mbyte/s transfer speed on its standard SD card interface. However, UHS-I requires a 1.8V IO level, which is not in the Colibri module specification. Since the 1.8V capability is not mandatory in the Colibri module specification, other modules may support only the 3.3V logic level. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interface is used in the 1.8V mode, removing the pull-up resistors on the carrier board is recommended. The i.MX 6ULL features internal pull-up resistors, which can be used instead.

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Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MByte/s	3.3V	Colibri Standard
High Speed	50 MHz	25 MByte/s	3.3V	
SDR12	25 MHz	12.5 MByte/s	1.8V	UHS-I May not be compatible with other modules
SDR25	50 MHz	25 MByte/s	1.8V	
DDR50	50 MHz	50 MByte/s	1.8V	
SDR50	100 MHz	50 MByte/s	1.8V	
SDR104	208 MHz	104 MByte/s	1.8V	

Features:
- Supports SD Memory Card Specification 3.0
- Supports SDIO Card Specification Version 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, 4.41, and 4.5
- Supports addressing larger capacity SD 3.0 or SDXC cards up to 2 TByte
- Supports SPI mode
- Supports SD UHS-I mode (up to 208MHz) with 1.8V IO voltage level (only standard SD port).

i.MX 6ULL SDIO interface	Max Bus Width	Description
USDHC1	4-bit	Colibri Standard SD/MMC interface
USDHC2	8-bit	Available as an alternate function, incompatible with the Colibri standard. Not available for modules with Wi-Fi and Bluetooth or the Colibri iMX6ULL 1GB IT with eMMC.

Table 5-30 Colibri SD/MMC Signal Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
190	SDCard CMD	SD1_CMD	usdhc1.CMD	I/O	Command
192	SDCard DAT<0>	SD1_DATA0	usdhc1.DATA0	I/O	Serial Data 0
49	SDCard DAT<1>	SD1_DATA1	usdhc1.DATA1	I/O	Serial Data 1
51	SDCard DAT<2>	SD1_DATA2	usdhc1.DATA2	I/O	Serial Data 2
53	SDCard DAT<3>	SD1_DATA3	usdhc1.DATA3	I/O	Serial Data 3
47	SDCard CLK	SD1_CLK	usdhc1.CLK	O	Serial Clock
43	WAKEUP Source<0>,SDCard CardDetect	SNVS_TAMPER0	gpio5.IO[0]	I	Card Detect (regular GPIO)

The additional SD/MMC signals allow the SD/MMC interface to be used as an 8-bit interface. This interface is only available on modules without Wi-Fi/Bluetooth and eMMC. The pins are incompatible with other Colibri modules, as they are not part of the specifications.

Table 5-31 Additional SD/MMC interface (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
94	Camera Input HSYNC	CSI_HSYNC	usdhc2.CMD	I/O	Command
29	UART_A DSR	LCD_DATA18			
101	Camera Input Data<2>	CSI_DATA00	usdhc2.DATA0	I/O	Serial Data 0
88	SPI CLK	LCD_DATA20			
103	Camera Input Data<3>	CSI_DATA01	usdhc2.DATA1	I/O	Serial Data 1

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X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
86	SPI CS	LCD_DATA21			
79	Camera Input Data<4>	CSI_DATA02	usdhc2.DATA2	I/O	Serial Data 2
92	SPI TXD	LCD_DATA22			
97	Camera Input Data<5>	CSI_DATA03	usdhc2.DATA3	I/O	Serial Data 3
90	SPI RXD	LCD_DATA23			
69	PS2 SCL2	CSI_DATA04	usdhc2.DATA4	I/O	Serial Data 4 (only for 8-bit MMC)
66	LCD RGB Data<14>	LCD_DATA14			
98	Camera Input Data<1>	CSI_DATA05	usdhc2.DATA5	I/O	Serial Data 5 (only for 8-bit MMC)
64	LCD RGB Data<15>	LCD_DATA15			
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06	usdhc2.DATA6	I/O	Serial Data 6 (only for 8-bit MMC)
57	LCD RGB Data<16>	LCD_DATA16			
61	LCD RGB Data<17>	LCD_DATA17	usdhc2.DATA7	I/O	Serial Data 7 (only for 8-bit MMC)
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07			
81	Camera Input VSYNC	CSI_VSYNC	usdhc2.CLK	O	Serial Clock
37	UART_A RI, Keypad_In<4>	LCD_DATA19			
75	Camera Input MCLK	CSI_MCLK	usdhc2.CD_B	O	Dedicated Card Detect (Regular GPIO could be used instead)
27	UART_A RTS	UART1_RTS			

5.14 Analog Audio

The Colibri iMX6ULL does not feature an audio codec on the module. Therefore, the analog audio interface pins (MIC, HEADPHONE, and LINE_IN) are left unconnected. However, for simple audio reproduction, there is a medium-quality sound (MQS) interface available. See chapter 5.16. For higher-quality audio, an external audio codec can be placed on the carrier board.

5.15 Audio Codec Interface

The Colibri module does not feature an audio codec interface as standard. Nevertheless, it is possible to access all three synchronous audio interfaces (SAI) of the i.MX 6ULL SoC at the module edge connector as alternate functions. The interfaces can be used as Intel® Audio Codec '97 (also known as AC'97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound, or IIS). The interfaces can be used to connect an external audio codec.

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Table 5-32 Synchronous Serial Interface (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
60	LCD RGB Data<2>	LCD_DATA02	sai1.TX_BCLK	I/O	Transmit Clock
98	Camera Input Data<1>	CSI_DATA05			
69	PS2 SCL2	CSI_DATA04	sai1.TX_SYNC	I/O	Transmit Frame Sync
70	LCD RGB Data<1>	LCD_DATA01			
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07	sai1.TX_DATA	O	Data Transmit
78	LCD RGB Data<4>	LCD_DATA04			
97	Camera Input Data<5>	CSI_DATA03	sai1.RX_BCLK	I/O	Receive Clock **not connected on modules with Wi-Fi**
79	Camera Input Data<4>	CSI_DATA02	sai1.RX_SYNC	I/O	Receive Frame Sync **not connected on modules with Wi-Fi**
58	LCD RGB Data<3>	LCD_DATA03	sai1.RX_DATA	I	Data Receive
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06			
76	LCD RGB Data<0>	LCD_DATA00	sai1.MCLK	I/O	Master Clock
103	Camera Input Data<3>	CSI_DATA01			Master Clock **not connected on modules with Wi-Fi**
31	UART_A DCD	JTAG_TDI	sai2.TX_BCLK	I/O	Transmit Clock
49	SDCard DAT<1>	SD1_DATA1			
23	UART_A DTR	JTAG_TDO	sai2.TX_SYNC	I/O	Transmit Frame Sync
192	SDCard DAT<0>	SD1_DATA0			
53	SDCard DAT<3>	SD1_DATA3	sai2.TX_DATA	O	Data Transmit
102		JTAG_TRST_B			
190	SDCard CMD	SD1_CMD	sai2.RX_SYNC	I/O	Receive Frame Sync
51	SDCard DAT<2>	SD1_DATA2	sai2.RX_DATA	I	Data Receive
99	nPWE	JTAG_TCK			
47	SDCard CLK	SD1_CLK	sai2.MCLK	I/O	Master Clock
71	Camera Input Data<0>,LCD Back-Light GPIO	JTAG_TMS			
54	LCD RGB Data<13>	LCD_DATA13	sai3.TX_BCLK	I/O	Transmit Clock
68	LCD RGB HSYNC	LCD_HSYNC			
44	LCD RGB DE	LCD_ENABLE	sai3.TX_SYNC	I/O	Transmit Frame Sync
52	LCD RGB Data<12>	LCD_DATA12			
64	LCD RGB Data<15>	LCD_DATA15	sai3.TX_DATA	O	Data Transmit
50	LCD RGB Data<11>	LCD_DATA11	sai3.RX_BCLK	I/O	Receive Clock
74	LCD RGB Data<10>	LCD_DATA10	sai3.RX_SYNC	I/O	Receive Frame Sync
66	LCD RGB Data<14>	LCD_DATA14	sai3.RX_DATA	I	Data Receive
82	LCD RGB VSYNC	LCD_VSYNC			
48	LCD RGB Data<9>	LCD_DATA09	sai3.MCLK	I/O	Master Clock
56	LCD RGB PCLK	LCD_CLK			

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5.15.1 Digital Audio Port used as I²S

The following signals are used for the I²S interface:

Table 5-33 Digital Audio port used as Master I²S

iMX6ULL Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6ULL)	Description
TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 6ULL SoC
RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 6ULL SoC
TX_SYNC	WS	O	Word Select, also known as Field Select or LRCLK
TX_BCLK	SCK	O	Serial Continuous Clock

Table 5-34 Digital Audio port used as Slave I²S

iMX6ULL Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6ULL)	Description
RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 6ULL SoC
TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 6ULL SoC
TX_SYNC	WS	I	Word Select, also known as Field Select or LRCLK
TX_BCLK	SCK	I	Serial Continuous Clock

The audio codecs require a master clock input and often an I²C interface for control. Any of the available I²C interfaces can be used (see section 5.8). Every SAI channel has a dedicated master clock signal that can be configured as input or output according to the need of the codec.

5.15.2 Digital Audio Port used as AC'97

The SAI interface can be configured as an AC'97 compatible interface. The AC'97 Audio interface does not require an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97 Audio codec requires a master reference clock. Since every SAI has a dedicated master clock output, this clock signal can be used. However, it is also possible to use a separate crystal/oscillator. Please take care with the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals connected to the host (e.g., i.MX 6ULL SoC) and not to the signal direction.

Table 5-35 Digital Audio port used as AC'97

iMX6ULL Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6ULL)	Description
RX_DATA[0]	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 6ULL
TX_DATA[0]	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 6ULL
TX_SYNC	SYNC	O	AC'97 Audio Sync
TX_BCLK	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

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5.16 Medium Quality Sound (MQS)

The medium-quality sound interface can be used to generate medium-quality audio via a standard GPIO. The PWM output signal does not require an external DAC or codec chip. It is possible to use a simple switching power amplifier circuit (Class-D amplifier).

SAI1 sources the MQS with a 2 channel 16-bit 44.1 kHz or 48 kHz audio signal, which is basically an I²S signal. Since the SAI source can only be used once, it is impossible to use MQS simultaneously with the external SAI1. The signal-to-noise ratio (SNR) is expected to be no more than 20 dB for signals below 10 kHz. For signals with higher frequencies, the SNR is even worse.

Table 5-36 MQS Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
6	Analog Input <1>	GPIO1_IO01			
31	UART_A DCD	JTAG_TDI	mqs.LEFT	O	Left MQS Channel
90	SPI RXD	LCD_DATA23			
8	Analog Input <0>	GPIO1_IO00			
23	UART_A DTR	JTAG_TDO	mqs.RIGHT	O	Right MQS Channel
92	SPI TXD	LCD_DATA22			

5.17 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for communication with various serial audio devices, including industry-standard codecs, S/PDIF transceivers, and other DSPs. The interface is only available as an alternate function as it is not part of the Colibri module standard.

Features:
- Independent (asynchronous) mode or shared (synchronous) mode of the transmitter and receiver
- Master or slave mode
- Up to 6 transmitters and up to 4 receivers at the module edge connector are available
- Programmable data interface modes (I2S, LSB aligned, MSB aligned)
- Programmable word length (8, 12, 16, 20, or 24-bit)
- AC97 support
- 128word FIFO shared by all transmitters
- 128word FIFO shared by all receivers

Table 5-37 ESAI Signal Pins (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
98	Camera Input Data<1>	CSI_DATA05	esai.TX_CLK	I/O	TX serial bit clock
69	PS2 SCL2	CSI_DATA04	esai.TX_FS	I/O	Frame sync for transmitters and receivers in the synchronous mode and the transmitters only in asynchronous mode
101	Camera Input Data<2>	CSI_DATA00	esai.TX_HF_CLK	I/O	TX high frequency clock **not connected on modules with Wi-Fi**
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07	esai.TX0	I/O	TX data 0
94	Camera Input HSYNC	CSI_HSYNC	esai.TX1	I/O	TX data 1 **not connected on modules with Wi-Fi**

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X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
96	Camera Input PCLK	CSI_PIXCLK	esai.TX2_RX3	I/O	TX data 2 or RX data 3
75	Camera Input MCLK	CSI_MCLK	esai.TX3_RX2	I/O	TX data 3 or RX data 2
81	Camera Input VSYNC	CSI_VSYNC	esai.TX4_RX1	I/O	TX data 4 or RX data 1 **not connected on modules with Wi-Fi**
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06	esai.TX5_RX0	I/O	TX data 5 or RX data 0
97	Camera Input Data<5>	CSI_DATA03	esai.RX_CLK	I/O	RX serial bit clock **not connected on modules with Wi-Fi**
79	Camera Input Data<4>	CSI_DATA02	esai.RX_FS	I/O	RX frame sync signal in asynchronous mode **not connected on modules with Wi-Fi**
103	Camera Input Data<3>	CSI_DATA01	esai.RX_HF_CLK	I/O	RX high frequency clock **not connected on modules with Wi-Fi**

5.18 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format data. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard. The S/PDIF signals are only available as an alternate function. Therefore the interface is not compatible with other modules.

Features:
- Internal data width: 24-bit
- Left and right channel 16x24-bit FIFO (receive and transmit)

Table 5-38 S/PDIF Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
4	Analog Input <2>	GPIO1_IO08	spdif.OUT	O	Serial data output
33	UART_A RXD	UART1_TXD			
72	LCD RGB Data<5>	LCD_DATA05			
106	nCS2	JTAG_MOD			
190	SDCard CMD	SD1_CMD			
2	Analog Input <3>	GPIO1_IO09	spdif.IN	I	Serial data input
35	UART_A TXD	UART1_RXD			
47	SDCard CLK	SD1_CLK			
62	LCD RGB Data<8>	LCD_DATA08			

5.19 Touch Panel Interface

The Colibri iMX6ULL provides a 4-wire resistive touch interface using the Analog Device AD7879-1 Touchscreen Controller. It is connected with the i.MX 6ULL SoC via the second I^2C interface (i2c2). The AD7879-1 does not support 5-wire operation mode. Please consult the Analog Device AD7879-1 documentation for more information.

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Table 5-39 Touch Interface Pins

X1 Pin#	Colibri STD Function	AD7879 Pin#	AD7879 Pin Name	I/O	Description
14	TSPX	A3	X+	I/O	X+ (4-wire)
16	TSMX	C3	X-	I/O	X- (4-wire)
18	TSPY	B3	Y+	I/O	Y+ (4-wire)
20	TSMY	D3	Y-	I/O	Y- (4-wire)

5.20 Analog Inputs

The analog inputs are provided by the NXP i.MX 6ULL SoC itself. The SoC features two ADCs with both 10 channel inputs. The two ADCs share the 10 input signals on the same pins. This means the SoC has only 10 ADC input pins in a total of which only 8 are available on the module edge connector. 4 out of these 8 ADC input pins are located as Colibri standard ADC input. This means only these signals are compatible with other modules and should be used first.

Since the two ACD share the same IO pins, it is possible to allocate the two ADC completely independently between the 8 available input pins.

Features:
- 12-bit ADC (8-bit and 10-bit mode supported)
- Linear successive approximation algorithm with 10/11-bit accuracy
- 0 to 3.3V (full scale)
- Sample rate up to 1MHz
- Single or continuous conversion
- DMA support
- Conversion complete and hardware average complete interrupt
- Automatic compare for less than, greater than, equal to, within range, or out of range

Table 5-40 Analog Inputs Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Function	I/O	Description
8	Analog Input <0>	GPIO1_IO00	ADCx_IN0	I	Standard analog input 1
6	Analog Input <1>	GPIO1_IO01	ADCx_IN1	I	Standard analog input 2
4	Analog Input <2>	GPIO1_IO08	ADCx_IN8	I	Standard analog input 3
2	Analog Input <3>	GPIO1_IO09	ADCx_IN9	I	Standard analog input 4
129	USB Host Power Enable	GPIO1_IO02	ADCx_IN2	I	Additional analog input
89	nWE	GPIO1_IO03	ADCx_IN3	I	Additional analog input **not connected on modules with Wi-Fi**
19	UART_C RXD	GPIO1_IO04	ADCx_IN4	I	Additional analog input
21	UART_C TXD	GPIO1_IO05	ADCx_IN5	I	Additional analog input

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5.21 Camera Interface

The i.MX 6ULL SoC itself features one parallel camera interface called CMOS sensor interface (CSI). It is important not to confuse this name with the interface standard MIPI/CSI-2, which is a serial camera interface. Even though the Colibri standard features an 8-bit camera interface, the interface on the Colibri iMX6ULL is not compatible with other Colibri modules. Some of the pins are not located at the compatible position.

Features:
- Raw (Bayer), RGB, YUV, YCbCr input
- Support for CCIR656 (BT.656)
- Maximum pixel clock frequency 133 MHz
- 8/10/16/24-bit parallel video interface
- Dedicated synchronization signals (VSYNC, HSYNC) or embedded in the data stream (BT.656)

Table 5-41 Parallel Camera Interface Pins (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
61	LCD RGB Data<17>	LCD_DATA17	csi.DATA[0]	I	Camera pixel data
77		UART3_RXD			
135	SPDIF_IN	UART3_TXD	csi.DATA[1]	I	Camera pixel data
57	LCD RGB Data<16>	LCD_DATA16			
33	UART_A RXD	UART1_TXD	csi.DATA[2]	I	Camera pixel data
101	Camera Input Data<2>	CSI_DATA00			Camera pixel data **not connected on modules with Wi-Fi**
35	UART_A TXD	UART1_RXD	csi.DATA[3]	I	Camera pixel data
103	Camera Input Data<3>	CSI_DATA01			Camera pixel data **not connected on modules with Wi-Fi**
25	UART_A CTS, Keypad_In<0>	UART1_CTS	csi.DATA[4]	I	Camera pixel data
79	Camera Input Data<4>	CSI_DATA02			Camera pixel data **not connected on modules with Wi-Fi**
27	UART_A RTS	UART1_RTS	csi.DATA[5]	I	Camera pixel data
97	Camera Input Data<5>	CSI_DATA03			Camera pixel data **not connected on modules with Wi-Fi**
36	UART_B RXD	UART2_TXD	csi.DATA[6]	I	Camera pixel data
69	PS2 SCL2	CSI_DATA04			
38	UART_B TXD	UART2_RXD	csi.DATA[7]	I	Camera pixel data
98	Camera Input Data<1>	CSI_DATA05			
32	UART_B CTS	UART2_CTS	csi.DATA[8]	I	Camera pixel data
85	Camera Input Data<8>, Keypad_Out<4>	CSI_DATA06			
34	UART_B RTS	UART2_RTS	csi.DATA[9]	I	Camera pixel data
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_DATA07			
29	UART_A DSR	LCD_DATA18	csi.DATA[10]	I	Camera pixel data
100	Keypad_Out<1>	UART3_CTS			

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X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
37	UART_A RI, Keypad_In<4>	LCD_DATA19	csi.DATA[11]	I	Camera pixel data
186	ADDRESS17	UART3_RTS			
88	SPI CLK	LCD_DATA20	csi.DATA[12]	I	Camera pixel data
196	I2C SCL	UART4_TXD			
86	SPI CS	LCD_DATA21	csi.DATA[13]	I	Camera pixel data
194	I2C SDA	UART4_RXD			
92	SPI TXD	LCD_DATA22	csi.DATA[14]	I	Camera pixel data
90	SPI RXD	LCD_DATA23	csi.DATA[15]	I	Camera pixel data
55	PS2 SDA1	ENET1_RXD0	csi.DATA[16]	I	Camera pixel data
62	LCD RGB Data<8>	LCD_DATA08			
48	LCD RGB Data<9>	LCD_DATA09	csi.DATA[17]	I	Camera pixel data
63	PS2 SCL1	ENET1_RXD1			
74	LCD RGB Data<10>	LCD_DATA10	csi.DATA[18]	I	Camera pixel data
178	DATA30	ENET1_CRS_DV			
50	LCD RGB Data<11>	LCD_DATA11	csi.DATA[19]	I	Camera pixel data
188	ADDRESS16	ENET1_TXD0			
52	LCD RGB Data<12>	LCD_DATA12	csi.DATA[20]	I	Camera pixel data
73		ENET1_TXD1			
30	PWM<C>	ENET1_TXEN	csi.DATA[21]	I	Camera pixel data
54	LCD RGB Data<13>	LCD_DATA13			
66	LCD RGB Data<14>	LCD_DATA14	csi.DATA[22]	I	Camera pixel data
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK			
64	LCD RGB Data<15>	LCD_DATA15	csi.DATA[23]	I	Camera pixel data
104		ENET1_RXER			
96	Camera Input PCLK	CSI_PIXCLK	csi.PIXCLK	I	Camera pixel clock
2	Analog Input <3>	GPIO1_IO09	csi.HSYNC	I	Camera horizontal sync
94	Camera Input HSYNC	CSI_HSYNC			Camera horizontal sync **not connected on modules with Wi-Fi**
4	Analog Input <2>	GPIO1_IO08	csi.VSYNC	I	Camera vertical sync
81	Camera Input VSYNC	CSI_VSYNC			Camera vertical sync **not connected on modules with Wi-Fi**
75	Camera Input MCLK	CSI_MCLK	csi.MCLK	O	Camera reference clock output
21	UART_C TXD	GPIO1_IO05	csi.FIELD	I	Field Identification (optional, identification of the upper or lower field for interlaced input formats)
28	PWM<B>	NAND_DQS			

The camera modules often require an additional I²C interface for control purposes. Any available I²C interface can be used (see section 5.8).

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Table 5-42 Camera Interface Color Pin Mapping

iMX6ULL Port Name	Bayer 10bit Generic	BT656/ YUV 8bit/ CCIR656	RGB888 8bit 3 cycle	YCbCr 8bit 2 cycle	RGB565 16bit 1 cycle	YCbCr 16bit 1 cycle	RGB666 18bit 1 cycle	RGB888 24bit 1 cycle	YCbCr 24bit 1 cycle
csi1.DATA[0]	D0				B0	C0	B4	B0	Cr0
csi1.DATA[1]	D1				B1	C1	B5	B1	Cr1
csi1.DATA[2]	D2	Y/C0	R/G/B0	Y/C0	B2	C2	B0	B2	Cr2
csi1.DATA[3]	D3	Y/C1	R/G/B1	Y/C1	B3	C3	B1	B3	Cr3
csi1.DATA[4]	D4	Y/C2	R/G/B2	Y/C2	B4	C4	B2	B4	Cr4
csi1.DATA[5]	D5	Y/C3	R/G/B3	Y/C3	G0	C5	B3	B5	Cr5
csi1.DATA[6]	D6	Y/C4	R/G/B4	Y/C4	G1	C6	B4	B6	Cr6
csi1.DATA[7]	D7	Y/C5	R/G/B5	Y/C5	G2	C7	B5	B7	Cr7
csi1.DATA[8]	D8	Y/C6	R/G/B6	Y/C6	G3	Y0	G4	G0	Cb0
csi1.DATA[9]	D9	Y/C7	R/G/B7	Y/C7	G4	Y1	G5	G1	Cb1
csi1.DATA[10]					G5	Y2	G0	G2	Cb2
csi1.DATA[11]					R0	Y3	G1	G3	Cb3
csi1.DATA[12]					R1	Y4	G2	G4	Cb4
csi1.DATA[13]					R2	Y5	G3	G5	Cb5
csi1.DATA[14]					R3	Y6	G4	G6	Cb6
csi1.DATA[15]					R4	Y7	G5	G7	Cb7
csi1.DATA[16]							R4	R0	Y0
csi1.DATA[17]							R5	R1	Y1
csi1.DATA[18]							R0	R2	Y2
csi1.DATA[19]							R1	R3	Y3
csi1.DATA[20]							R2	R4	Y4
csi1.DATA[21]							R3	R5	Y5
csi1.DATA[22]							R4	R6	Y6
csi1.DATA[23]							R5	R7	Y7

5.22 Clock Output

The i.MX 6ULL SoC has two general-purpose clock output channels (CLKO1 and CLKO2) available on different SoC pins. Since the SAI (audio), CSI (camera), as well as RMII (Ethernet) interfaces feature dedicated reference clock outputs, the general-purpose clock outputs are not reserved for the internal Ethernet PHY.

Table 5-43 External Clock Signal Pins (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
51	SDCard DAT<2>	SD1_DATA2	ccm.CLKO1	O	General Purpose Clock Output 1
71	Camera Input Data<0>,LCD Back-Light GPIO	JTAG_TMS			
23	UART_A DTR	JTAG_TDO	ccm.CLKO2	O	General Purpose Clock Output 2
53	SDCard DAT<3>	SD1_DATA3			

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5.23 Keypad

You can use any free GPIOs to realize a matrix keypad interface. Such a software solution does not come with any additional hardware support. This is the preferred solution if a carrier board needs to be compatible with different Colibri modules.

Additionally, the i.MX 6ULL SoC features a keyboard controller with hardware support. As the keyboard controller is only available as an alternate function, this interface is incompatible with other Colibri modules. It can only be used if the required pins are being used for their primary function.

The keyboard controller eliminates the requirement for de-bounce capacitors and pull-up resistors. It can handle up to two buttons being pressed without the need for de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 4 by 4.

Features:
- Open drain design
- Glitch suppression circuit
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- 2-point, as well as a 3-point key matrix, supported

Table 5-44 Keyboard Matrix Interface Signals

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
63	PS2 SCL1	ENET1_RXD1	kpp.COL[0]	O	Keyboard column 0
188	ADDRESS16	ENET1_TXD0	kpp.COL[1]	O	Keyboard column 1
30	PWM<C>	ENET1_TXEN	kpp.COL[2]	O	Keyboard column 2
104		ENET1_RXER	kpp.COL[3]	O	Keyboard column 3
55	PS2 SDA1	ENET1_RXD0	kpp.ROW[0]	I	Keyboard row 0
178	DATA30	ENET1_CRS_DV	kpp.ROW[1]	I	Keyboard row 1
73		ENET1_TXD1	kpp.ROW[2]	I	Keyboard row 2
67	PWM<D>,Camera Input Data<6>	ENET1_TXCLK	kpp.ROW[3]	I	Keyboard row 3

5.24 Controller Area Network (CAN)

The NXP i.MX 6ULL SoC Flexible Controller Area Network (FlexCAN) peripheral implements the CAN protocol according to the CAN 2.0B specifications. It features a buffer for up to 64 messages and supports both standard and extended message frames. The CAN interface is not part of the standard Colibri interfaces, and therefore, it is incompatible with the complete Colibri module family. However, the CAN interface located at pin 63/55 is compatible with the Colibri iMX6, the Colibri iMX7, and the Colibri VFxx modules. Therefore, whenever only one CAN interface is required, it is recommended to use the one available at pin 63/55.

Additionally, the CAN interface on pin 178/188 is compatible with the Colibri iMX6 and the Colibri iMX7 but not with the VFxx. For more information, check the Toradex Pinout Designer Tool.

Features:
- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of eight-byte data length (configurable as RX or TX)

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- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free-running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-45 CAN Signal Pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
63	PS2 SCL1	ENET1_RXD1	can1.RX	I	CAN receive pin, compatible with Colibri iMX6, iMX7, and VFxx
48	LCD RGB Data<9>	LCD_DATA09			Alternate CAN receive pin
49	SDCard DAT<1>	SD1_DATA1			
186	ADDRESS17	UART3_RTS			
55	PS2 SDA1	ENET1_RXD0	can1.TX	O	CAN transmit pin, compatible with Colibri iMX6, iMX7, and VFxx
62	LCD RGB Data<8>	LCD_DATA08			Alternate CAN transmit pin
100	Keypad_Out<1>	UART3_CTS			
192	SDCard DAT<0>	SD1_DATA0			
188	ADDRESS16	ENET1_TXD0	can2.RX	I	CAN receive pin, compatible with Colibri iMX6 and iMX7
34	UART_B RTS	UART2_RTS			Alternate CAN receive pin
50	LCD RGB Data<11>	LCD_DATA11			
53	SDCard DAT<3>	SD1_DATA3			
178	DATA30	ENET1_CRS_DV	can2.TX	O	CAN transmit pin, compatible with Colibri iMX6 and iMX7
32	UART_B CTS	UART2_CTS			Alternate CAN transmit pin
51	SDCard DAT<2>	SD1_DATA2			
74	LCD RGB Data<10>	LCD_DATA10			

5.25 Quad Serial Peripheral Interface (QuadSPI)

The i.MX 6ULL SoC features Quad Serial Peripheral Interface. Since the interface is located on the pins of the NAND flash, it is not possible to use the QuadSPI on the Colibri iMX6ULL.

5.26 JTAG

The JTAG interface is not generally required for software development with the Colibri iMX6ULL. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and for debug reasons, it is strongly recommended that the USBC (USB_OTG1) interface is accessible even if not needed in the production system. Additionally, UART_A (UART1) should also be accessible.

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The JTAG interface is located on test points on the bottom side of the module. The location is the same for all modules in the Colibri family. On the Evaluation Board 3.1, the signals are accessible through pogo pins. The interface voltage is 3.3V. Hence, jumper JP 29 must be in position 2-3. Since on the i.MX 6ULL SoC the JTAG pins are regular IO pins with multiple functions, the pins are also available on the module edge connector. Please make sure no peripheral devices are connected to these pins while the JTAG interface is in use.

Table 5-46 JTAG Signal Pins on SODIMM connector

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	I/O	Description
31	UART_A DCD	JTAG_TDI	sjc.TDI	I	Test Data Input
23	UART_A DTR	JTAG_TDO	sjc.TDO	O	Test Data Output
99	nPWE	JTAG_TCK	sjc.TCK	I	Test Clock
71	Camera Input Data<0>,LCD Back-Light GPIO	JTAG_TMS	sjc.TMS	I	Test Mode Select
102		JTAG_TRST_B	sjc.TRSTB	I	Test Reset
106	nCS2	JTAG_MOD	sjc.MOD	I	Strapping: 0: Debug Mode (default, 10k pull down on module) 1: Boundary Scan Mode (overdrive it externally)
32	UART_B CTS	UART2_CTS	sjc.DE_B	I/O	Debug request/acknowledge

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6. Power Management

The Colibri iMX6ULL has been designed for low power consumption. To achieve a minimum consumption, the module features different run and sleep states. Depending on the operating system, it may be that the software support of some of the sleep states, which are presented in this section, is limited. Please check the latest state of the provided OS images on the developer website.

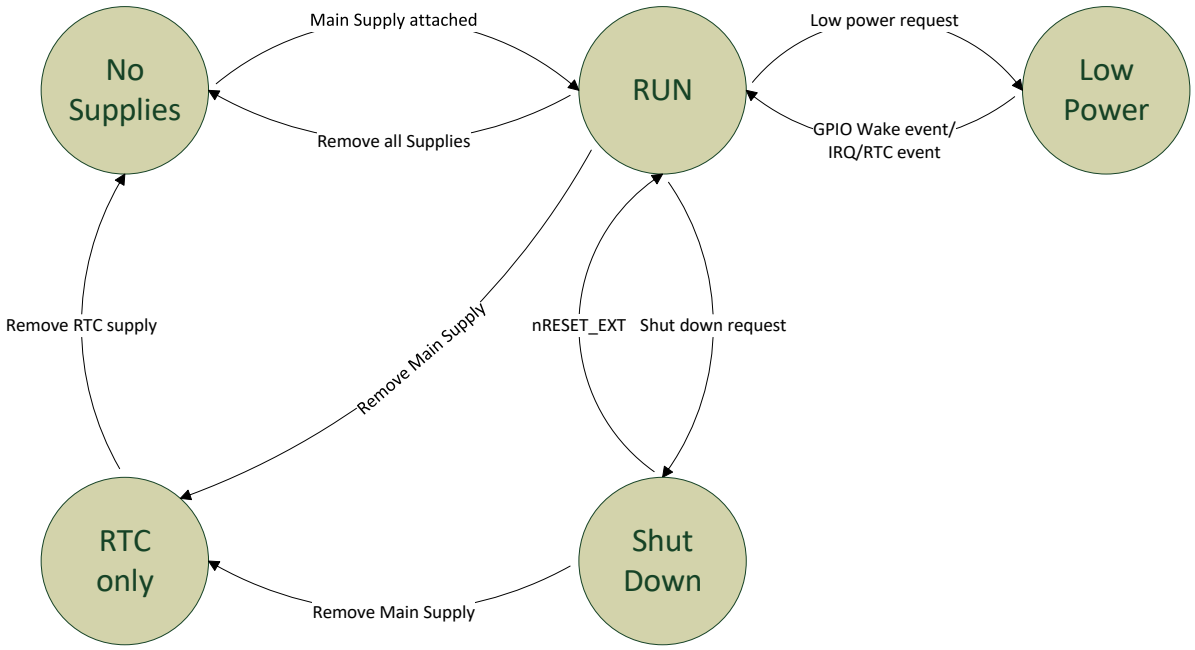


Figure 9: Run and Sleep States

Table 6-1 1.1 Power States

Power Rail	No Supply	RTC Only	Shut Down	RUN	Low Power
VCC_BATT (RTC Supply)	OFF	ON	ON	ON	ON
3V3 (Module Main Supply)	OFF	OFF	ON	ON	ON
VDD_SOC	OFF	OFF	OFF	ON	ON
VDD_DRAM	OFF	OFF	OFF	ON	ON
On module Peripheral 3.3V	OFF	OFF	ON	ON	ON
nRESET_OUT	Undefined	Undefined	HIGH	HIGH	HIGH

6.1 No Supply

All power rails are removed from the module.

6.2 RTC Only

All power rails are removed from the module, except the VCC_BATT is provided to the module. The RTC on the module is kept running for keeping the time. The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found on the developer page https://developer.toradex.com/knowledge-base/imx6ull-power-consumption). Therefore, a standard lithium coin cell battery can drain faster than required for certain designs. If a

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rechargeable RTC battery is not a suitable solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, do not provide the VCC_BATT voltage rail at pin 40 during the RTC state. Nevertheless, the VCC_BATT voltage is required in RUN, Low Power, and LPSR states but can be sourced from the same rail as the 3V3 main supply of the module. A suitable reference schematic can be found in the schematic diagram of the Colibri evaluation board.

Besides the RTC and power management function, the i.MX 6ULL SoC uses the VCC_BATT rail also as IO rail for the SNVS pins. The following SNVS pins are available on the SODIMM connector as regular GPIOs:

Table 6-2 SNVS pins

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	Remarks
43	WAKEUP Source<0>,SDCard CardDetect	SNVS_TAMPER0	gpio5.IO[0]	
45	WAKEUP Source<1>	SNVS_TAMPER1	gpio5.IO[1]	
93	RDnWR	SNVS_TAMPER6	gpio5.IO[6]	Not available on modules with Wi-Fi
95	RDY	SNVS_TAMPER3	gpio5.IO[3]	
105	nCS0	BOOT_MODE0	gpio5.IO[10]	
107	nCS1	SNVS_TAMPER4	gpio5.IO[4]	
127		BOOT_MODE1	gpio5.IO[11]	Not available on modules with Wi-Fi
131	USB Host Over-Current Detect	SNVS_TAMPER5	gpio5.IO[5]	
137	USB Client Cable Detect, SPDIF_OUT	SNVS_TAMPER2	gpio5.IO[2]	
138	ADDRESS23	SNVS_TAMPER8	gpio5.IO[8]	Not available on modules with Wi-Fi

In the “RUN” and “Low Power” states, the module bridges the VCC_BATT rail to the main 3.3V input rail to prevent high current draws on the VCC_BATT rail (see also section 5.1). However, in all other states, the SNVS pins are powered from the VCC_BATT rail. The pins keep their level since this rail is also available in the “RTC Only” state. If there is any load on such a pin, this could cause a higher current draw on the VCC_BATT rail. To prevent that, make sure that SNVS pins with any attached load are set to 0 before entering the “RTC Only” state.

6.3 Shut Down

The module has been shut down. Only the software can put the module in a shutdown state. All ‘On’ module rails are switched ‘Off’, but the carrier board still provides the 3V3 main supply as well as the VCC_BATT. The ‘On’ module RTC is kept running to keep the time. The system can be reactivated from the Shut-Down state by pressing the reset button (this option is not available on all Colibri modules) or removing and reapplying the 3V3 main supply voltage rail.

The nRESET_OUT is not active in this mode. This means the reset is kept high. Since there is either a primary supply power cycle or a reset button press needed for exiting this state, there is a nRESET_OUT cycle while leaving this state.

6.4 RUN

The system is up and running. The CPU is active, and the peripheral modules are enabled. In this mode, the VDD_ARM voltage might be adjusted according to the CPU frequency to save energy.

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6.5 Low Power

When the CPU is not running, the processor can enter the low power mode (sleep mode). The Colibri iMX6ULL supports different levels of low power modes:

- System Idle: The CPU can enter this mode automatically if there is no thread running anymore. All peripherals can be kept working. The CPU state is retained so that the interrupt response can be very short.
- Low Power Idle: Some of the peripherals are kept still alive while others are shut off. The interrupt response in this state is longer than in the System Idle, but the power consumption is much lower.
- Suspend: All clocks, unused peripherals, and PHYs are off. The DDR3L RAM stays in Self-Refresh mode. The exit time from this mode is much longer. All power rails are still available on the module.

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7. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Colibri iMX6ULL even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in recovery mode, the USBC (USB_OTG1) interface is used to connect it to a host computer. You find additional information at our Developer Center: http://developer.toradex.com.

To enter the recovery mode, connect the recovery mode pads on the front of the module together (see picture below) or pull SODIMM pin 91 to GND with a 10 kΩ resistor while power up the module. If the Colibri Evaluation Board V3.x is used, the SW9 button can be pressed during switching on the power supply for the module.

Important: make sure that there is no bootable SD card plugged into the slot. Otherwise, the module tries to boot from the external SD card instead of the USB serial loader.

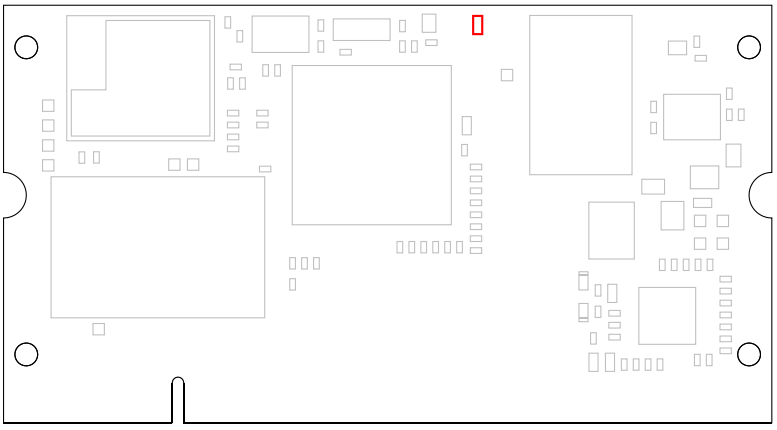


Figure 10: Location of recovery mode pads

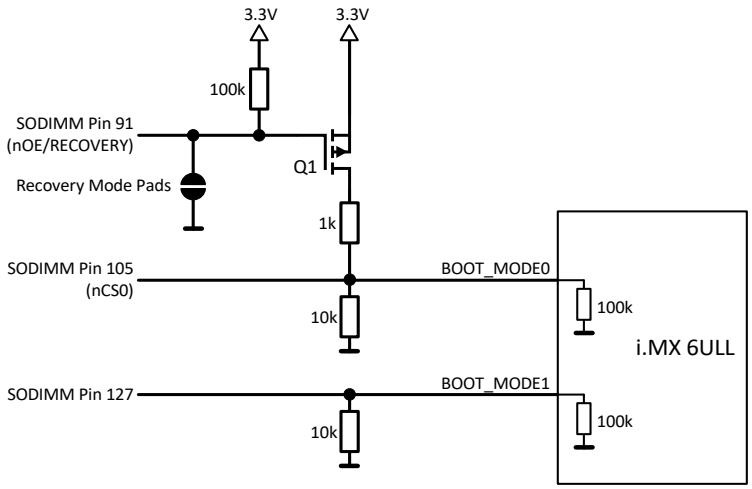


Figure 11: Recovery Mode Glue Logic

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8. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded on our website at:

http://developer.toradex.com/products/colibri-iMX6ULL#errata

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9. Technical Specifications

9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_3V3	Main power supply	-0.3	3.6	V
Vmax_AVDD	Analog power supply	-0.3	3.6	V
Vmax_VCC_BATT	RTC power supply	-0.3	3.6	V
Vmax_IO	IO pins with GPIO function	-0.5	3.6	V

9.2 Recommended Operation Conditions

Table 9-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
3V3	Main power supply*	3.135	3.3	3.465	V
AVDD	Analog power supply	3.0	3.3	3.6	V
VCC_BATT	RTC power supply	2.4	3.3	3.6	V

* The limiting device is the KSZ8041 Ethernet PHY. All other devices on the module work from 3.0V to 3.6V. The reset circuit threshold voltage is at 2.93V (+/- 2.5%). Make sure the main power supply voltage rail never drops below this value. Otherwise, the module is reset.

9.3 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Colibri product family. Following those recommendations ensures that the carrier board being designed will be compatible with all existing and future Colibri modules. For details, please refer to the Colibri Carrier Board Design Guide.

For designing carrier boards for a particular Colibri module only, please consult our Developer Website for module-specific power consumption information https://developer.toradex.com/knowledge-base/imx6ull-power-consumption. However, please note that scaling the carrier board power supplies for a particular module only may cause compatibility issues with other existing and future modules within the Colibri family.

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9.4 Mechanical Characteristics

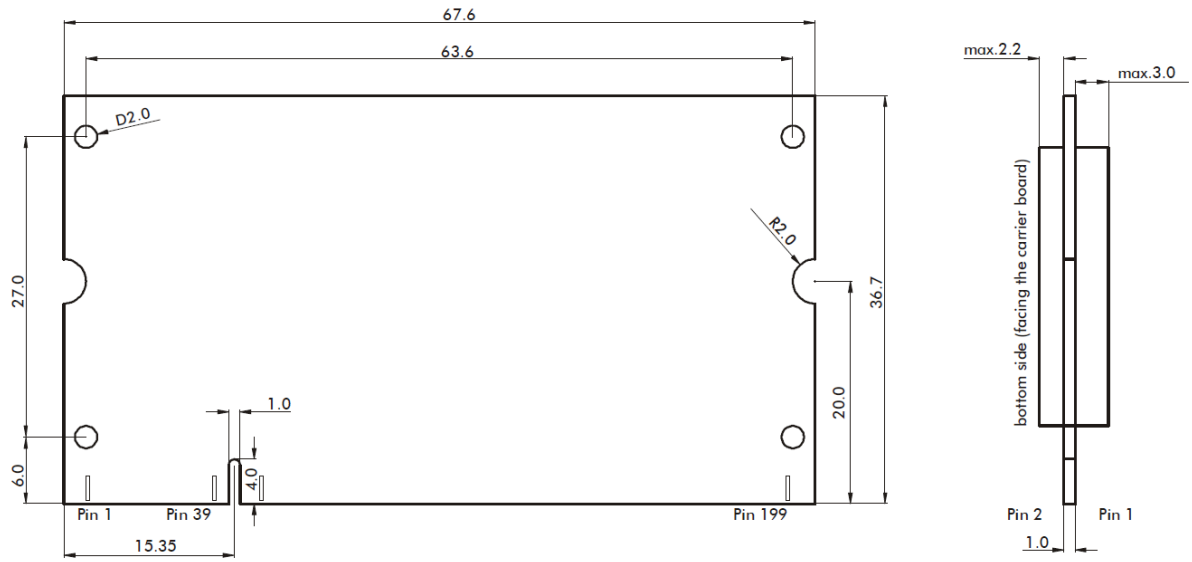


Figure 12 Mechanical dimensions of the Colibri module (top view)
Tolerance for all measures: +/- 0.1mm

9.4.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket.
A selection of SODIMM200 socket manufacturers is detailed below:

AUK Connectors:	http://www.aukconnector.com
CONCRAFT:	http://www.concraft.com.tw
Morethanall Co Ltd.:	http://www.morethanall.com
Tyco Electronics (AMP):	http://www.te.com
NEXUS COMPONENTS GmbH	http://www.nexus-de.com

9.5 Thermal Specification

The NXP i.MX 6ULL SoC has an integrated temperature sensor for monitoring the temperature of the CPU.

Here are some general considerations:

- Suppose you only use the peak performance for a short time. In that case, heat dissipation is less of a problem because advanced power management reduces power consumption when full performance is not required.
- A lower die temperature also lowers the power consumption due to smaller leakage currents.

Since the overall power consumption of the Colibri iMX6ULL is dramatically lower than, for example, the Colibri iMX6, there is no need for a cooling solution for most of the applications.

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Table 9-3 Thermal Specification Colibri iMX6ULL 256MB

Description	Min	Typ	Max	Unit
Operating temperature range	0		70[1]	°C
Storage Temperature	-40		100	°C
Junction temperature SoC	0		95	°C
Thermal Resistance Junction-to-Ambient, i.MX 6ULL only. (Theta-JA)[2]		36.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 6ULL chip case. (Psi-JCtop)[2]		0.6		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer board defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

Table 9-4 Thermal Specification Colibri iMX6ULL 512MB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40		85[1]	°C
Storage Temperature	-40		100	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 6ULL only. (Theta-JA)[2]		36.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 6ULL chip case. (Psi-JCtop)[2]		0.6		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer board defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

Table 9-5 Thermal Specification Colibri iMX6ULL 1GB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 6ULL only. (Theta-JA)[2]		36.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 6ULL chip case. (Psi-JCtop)[2]		0.6		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer board defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

Table 9-6 Thermal Specification Colibri iMX6ULL 512MB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-30[3]		85[1]	°C
Storage Temperature	-40		100	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 6ULL only. (Theta-JA)[2]		36.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 6ULL chip case. (Psi-JCtop)[2]		0.6		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer board defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.
[3] The Wi-Fi module is limiting the minimum operating temperature. The rest of the components are capable of running until -40°C

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Table 9-7 Thermal Specification Colibri iMX6ULL 512MB WB

Description	Min	Typ	Max	Unit
Operating temperature range	0		70[1]	°C
Storage Temperature	-40		100	°C
Junction temperature SoC	0		95	°C
Thermal Resistance Junction-to-Ambient, i.MX 6ULL only. (Theta-JA)[2]		36.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 6ULL chip case. (Psi-JCtop)[2]		0.6		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer board defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.
[3] The Wi-Fi module is limiting the minimum operating temperature. The rest of the components are capable of running until -40°C

9.6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at: http://www.toradex.com/support/product-compliance

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