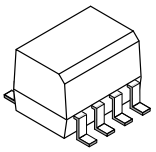
Logic Gate Optocoupler, High CMR, Bi-Directional

FOD8012A



SOIC8
CASE 751DZ

Description

The FOD8012A is a half duplex, bi−directional, high−speed logic gate Optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes **onsemi**'s patented coplanar packaging technology, OPTOPLANAR®, and optimized IC design to achieve minimum 20 kV/μs Common Mode Noise Rejection (CMR) rating.

This high−speed logic gate optocoupler is highly integrated with 2 optically coupled channels arranged in bi−directional configuration, and housed in a compact 8−pin small outline package. Each optocoupler channel consists of a high−speed AlGaAs LED driven by a CMOS buffer IC coupled to a CMOS detector IC. The detector IC comprises of an integrated photodiode, a high−speed trans−impedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled to the high efficiency of the LED achieves low power consumption as well as very high speed (60 ns propagation delay, 15 ns pulse width distortion).

Features

- Half Duplex, Bi−Directional
- 20 kV/μs Minimum Common Mode Rejection
- High Speed:
  - 15 Mbit/s Date Rate (NRZ)
  - 60 ns Maximum Propagation Delay
  - 15 ns Maximum Pulse Width Distortion
  - 30 ns Maximum Propagation Delay Skew
- 3.3 V and 5 V CMOS Compatibility
- Extended Industrial Temperate Range, −40 to +110°C Temperature Range
- Safety and Regulatory Approvals:
  - UL1577, 3750 VAC_{RMS} for 1 min.
  - DIN EN/IEC60747−5−5 (approval pending)

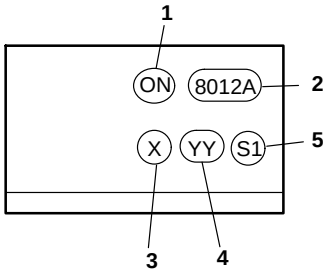
Applications

- Industrial Fieldbus Communications
  - DeviceNet, CAN, RS485
- Microprocessor System Interface
  - SPI, I^2C
- Programmable Logic Control
- Isolated Data Acquisition System
- Voltage Level Translator

Related Resources

- FOD8001/D, High Noise Immunity, 3.3 V/5 V Logic Gate Optocoupler Datasheet

MARKING DIAGRAM



1. ON = **onsemi** Logo
2. 8012A = Device Number
3. X = One−Digit Year Code, e.g. '8'
4. YY = Two Digit Work Week Ranging from '01' to '53'
5. S1 = Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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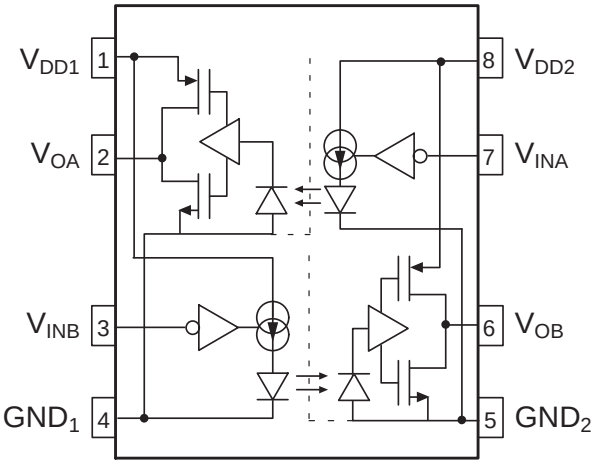
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TRUTH TABLE

V_{IN}	LED	V_O
High	OFF	High
Low	ON	Low

NOTE: When not communicating, V_{IN} must be in static high logic condition.

Functional Schematic



0.1μF bypass capacitor required from V_{DD} to GND

Figure 1. Functional Schematic

PIN DEFINITIONS

Pin Number	Pin Name	Description
1	V_{DD1}	**Supply Voltage** to Channel−A detector IC and Channel−B buffer IC
2	V_{OA}	**Output Voltage** from Channel−A detector IC
3	V_{INB}	**Input Voltage** to Channel−B buffer IC
4	GND_1	**Ground** for Channel−A detector IC and Channel−B buffer IC
5	GND_2	**Ground** for Channel−A buffer IC and Channel−B detector IC
6	V_{OB}	**Output Voltage** from Channel−B detector IC
7	V_{INA}	**Input Voltage** to Channel−A buffer IC
8	V_{DD2}	**Supply Voltage** to Channel−A buffer IC and Channel−B detector IC

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +110	°C
T_J	Junction Temperature	−40 to +130	°C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 s	°C
V_{DD1}, V_{DD2}	Supply Voltage	0 to 6.0	V
V_{IA}, V_{IB}	Input Voltage	−0.5 to V_{DD} + 0.5	V
I_{IA}, I_{IB}	Input DC Current	−10 to +10	μA
V_{OA}, V_{OB}	Output Voltage	−0.5 to V_{DD} + 0.5	V
I_{OA}, I_{OB}	Average Output Current	10	mA
PD_I	Input Power Dissipation (Note 1)	60	mW
PD_O	Output Power Dissipation (Note 1)	60	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. No derating required.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	−40	+110	°C
V_{DD1}, V_{DD2}	Supply Voltages (3.3 V Operation) (Note 2)	3.0	3.6	V
	Supply Voltages (5.0 V Operation) (Note 2)	4.5	5.5	
V_{IH}	Logic High Input Voltage	2.0	V_{DD}	V
V_{IL}	Logic Low Input Voltage	0	0.8	V
t_r, t_f	Input Signal Rise and Fall Time		1.0	ms

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. 0.1 μF bypass capacitor must be connected between Pin 1 and 4, and 5 and 8. The capacitors should be kept close to the supply pins.

ISOLATION CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at T_A = 25°C)

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Input−Output Isolation Voltage	f = 60 Hz, t = 1.0 min., $I_{I-O} \le$ 10 μA (Notes 3, 4)	3750			Vac_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 3)	10^{11}			Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, f = 1.0 MHz (Note 3)		0.2		pF

3. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
4. 3,750 VAC_{RMS} for 1 minute duration is equivalent to 4,500 VAC_{RMS} for 1 second duration.

ELECTRICAL CHARACTERISTICS (T_A = −40°C to +110°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, unless otherwise specified. Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD1L}, I_{DD2L}	Logic Low Supply Current	V_{IA}, V_{IB} = 0 V		5.8	8.0	mA
I_{DD1H}, I_{DD2H}	Logic High Supply Current	V_{IA}, V_{IB} = V_{DD}		2.5	4.0	mA
I_{IA}, I_{IB}	Input Current		−10		+10	μA
V_{OH}	Logic High Output Voltage	I_O = −20 μA, V_I = V_{IH}, V_{DD} = 3.3 V	3.2	3.3		V
		I_O = −4 mA, V_I = V_{IH}, V_{DD} = 3.3 V	3.0	3.1		
		I_O = −20 μA, V_I = V_{IH}, V_{DD} = 5 V	4.9	5.0		
		I_O = −4 mA, V_I = V_{IH}, V_{DD} = 5 V	4.7	4.8		
V_{OL}	Logic Low Output Voltage	I_O = 20 μA, V_I = V_{IL}, V_{DD} = 3.3 V or 5 V		0	0.1	V
		I_O = 4 mA, V_I = V_{IL}, V_{DD} = 3.3 V or 5 V		0.26	0.6	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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SWITCHING CHARACTERISTICS (T_A = −40°C to +110°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, unless otherwise specified.
Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Data Rate				15	Mbit/s
t_{PHL}	Propagation Delay Time to Logic Low Output	PW = 66.7 ns, C_L = 15 pF		37	60	ns
t_{PLH}	Propagation Delay Time to Logic High Output	PW = 66.7 ns, C_L = 15 pF		40	60	ns
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	PW = 66.7 ns, C_L = 15 pF (Note 5)		3	15	ns
$t_{PSK(CC)}$	Channel−Channel Skew	PW = 66.7 ns, C_L = 15 pF (Note 6)		12	25	ns
$t_{PSK(PP)}$	Part−Part Skew	PW = 66.7 ns, C_L = 15 pF (Note 7)			30	ns
t_R	Output Rise Time (10% to 90%)	PW = 66.7 ns, C_L = 15 pF		6.5		ns
t_F	Output Fall Time (90% to 10%)	PW = 66.7 ns, C_L = 15 pF		6.5		ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	V_I = V_{DD1}, V_O > 0.8 V_{DD1}, V_{CM} = 1000 V (Note 8)	20	40		kV/μs
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	V_I = 0 V, V_O < 0.8 V, V_{CM} = 1000 V (Note 8)	20	40		kV/μs

5. PWD is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen for one channel switching, while holding the other channel output at a low or high state, or while both channels are in synchronous data transmission mode.
6. $t_{PSK(CC)}$ is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between the two channels within a single device.
7. $t_{PSK(PP)}$ is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between any two units from the same manufacturing date code that are operated at same case temperature, at same operating conditions, with equal loads.
8. Common mode transient immunity at output high is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dVcm/dt on the trailing edge of the common pulse signal, Vcm, to assure that the output will remain low.

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TYPICAL PERFORMANCE CURVES

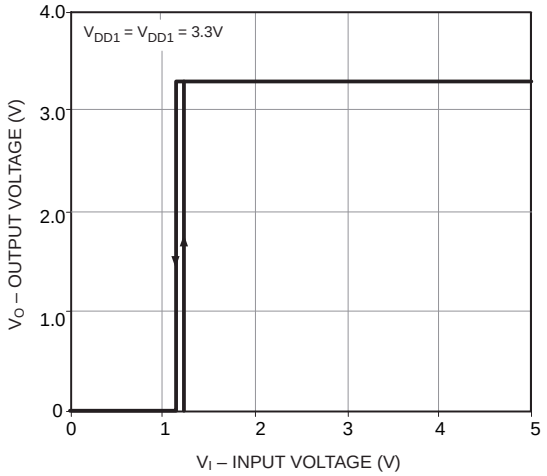


Figure 2. Typical Output Voltage vs. Input Voltage (Channel A & B)

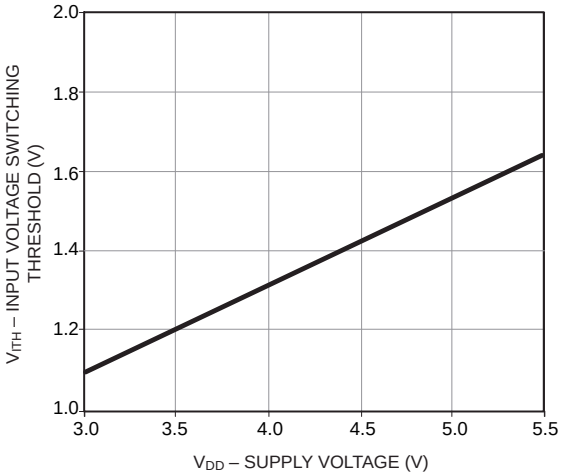


Figure 3. Typical Input Voltage Switching Threshold vs. Input Supply Voltage (Channel A & B)

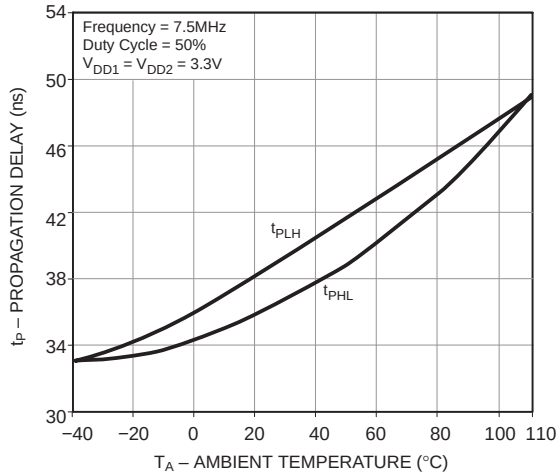


Figure 4. Typical Propagation Delay vs. Ambient Temperature (Channel A & B)

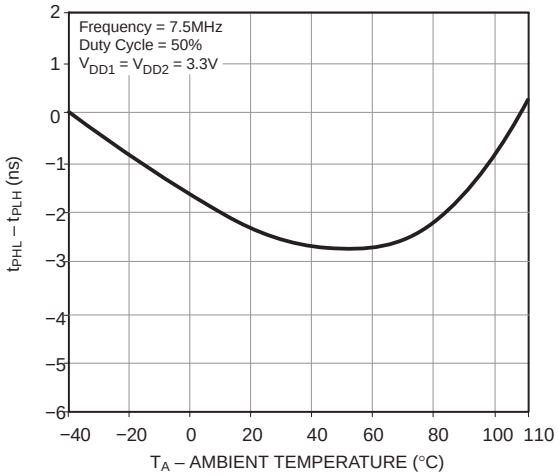


Figure 5. Typical $t_{PHL} – t_{PLH}$ vs. Ambient Temperature (Channel A & B)

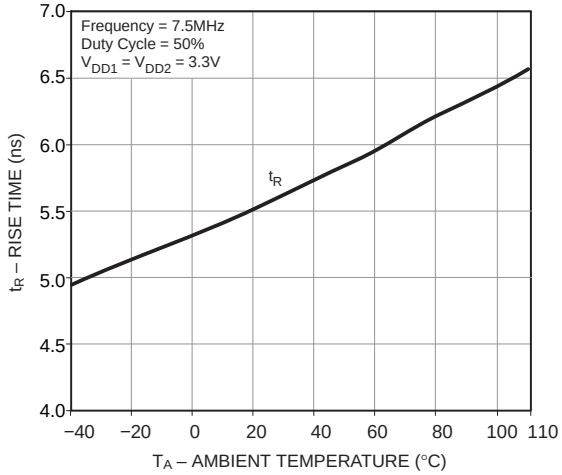


Figure 6. Typical Rise Time vs. Ambient Temperature (Channel A & B)

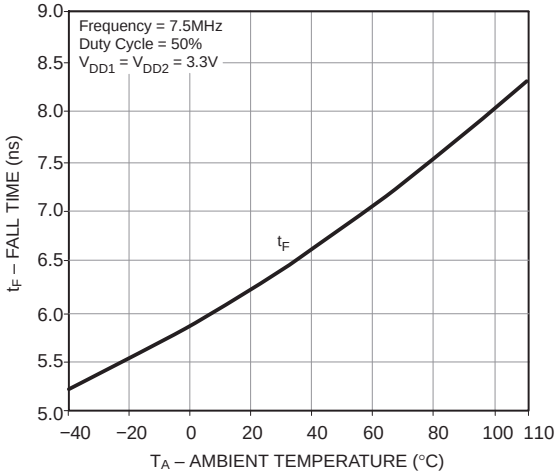


Figure 7. Typical Fall Time vs. Ambient Temperature (Channel A & B)

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TYPICAL PERFORMANCE CURVES (Continued)

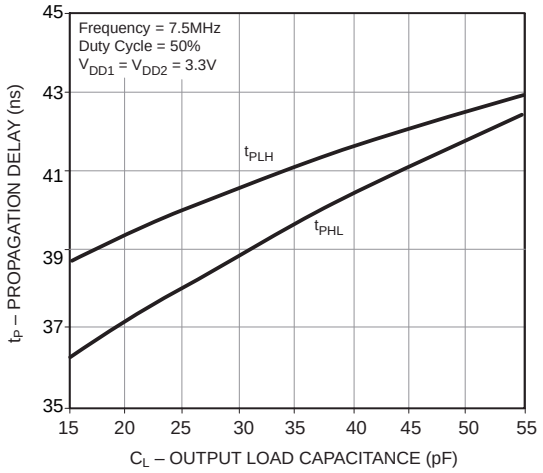


Figure 8. Typical Propagation Delay vs. Output Load Capacitance (Channel A & B)

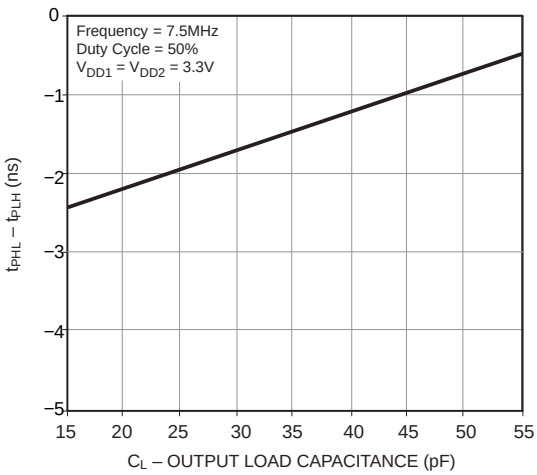


Figure 9. Typical $t_{PHL} - t_{PLH}$ vs. Output Load Capacitance (Channel A & B)

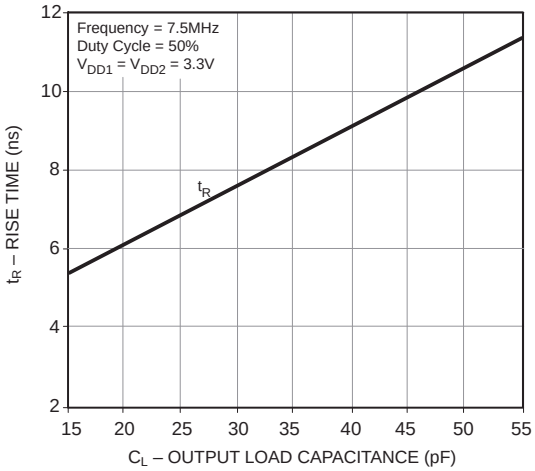


Figure 10. Typical Rise Time vs. Output Load Capacitance (Channel A & B)

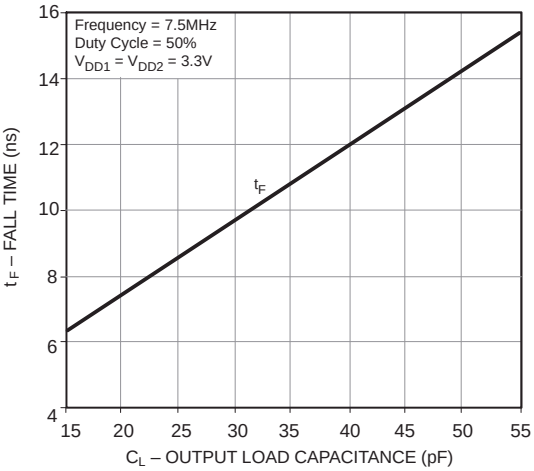


Figure 11. Typical Fall Time vs. Output Load Capacitance (Channel A & B)

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TYPICAL PERFORMANCE CURVES (Continued)

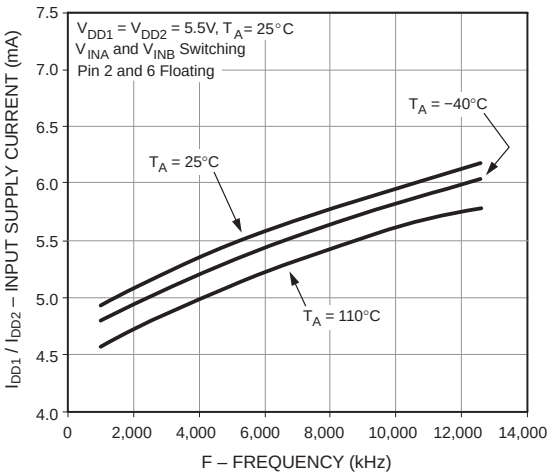


Figure 12. Typical I_{DD1}/I_{DD2} Supply Current vs. Frequency

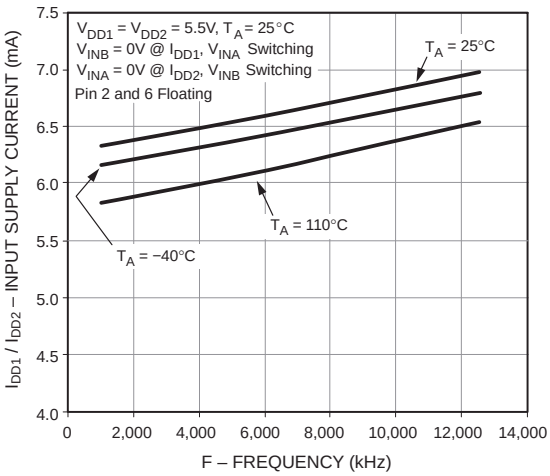


Figure 13. Typical I_{DD1}/I_{DD2} Supply Current vs. Frequency

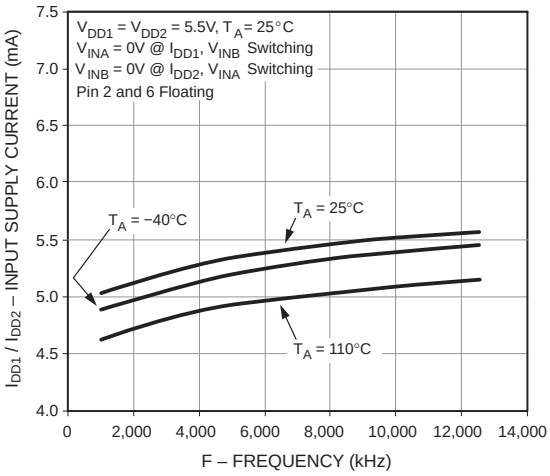


Figure 14. Typical I_{DD1}/I_{DD2} Supply Current vs. Frequency

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TEST CIRCUITS

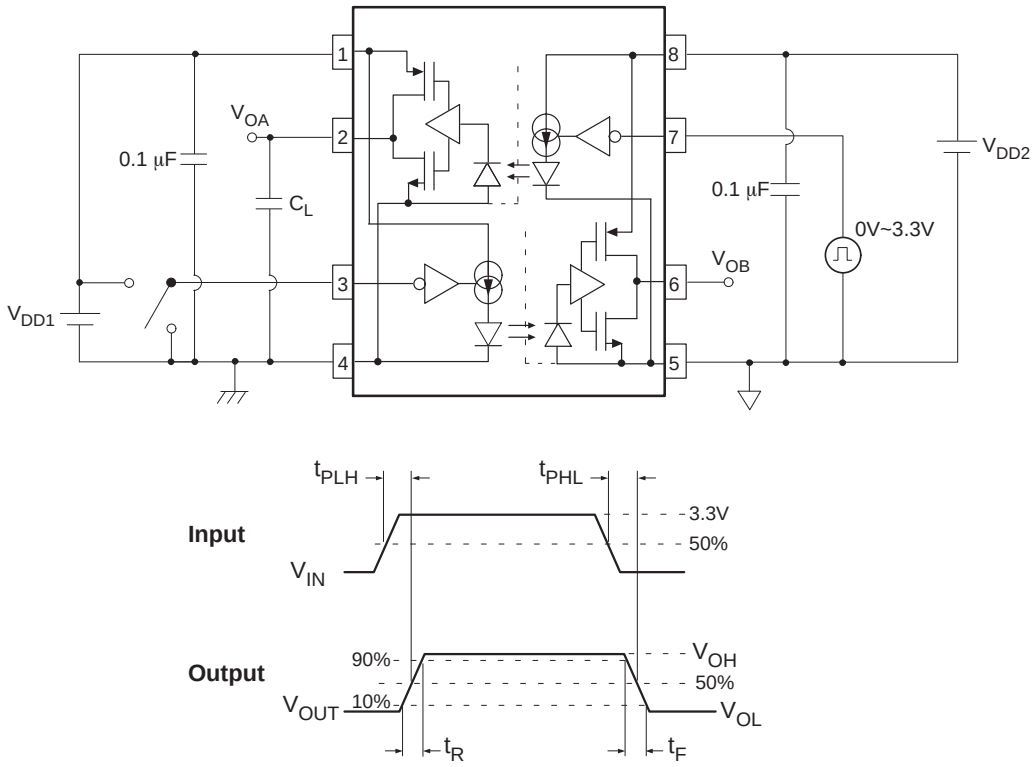


Figure 15. Test Circuit for Propagation Delay Time and Rise Time, Fall Time

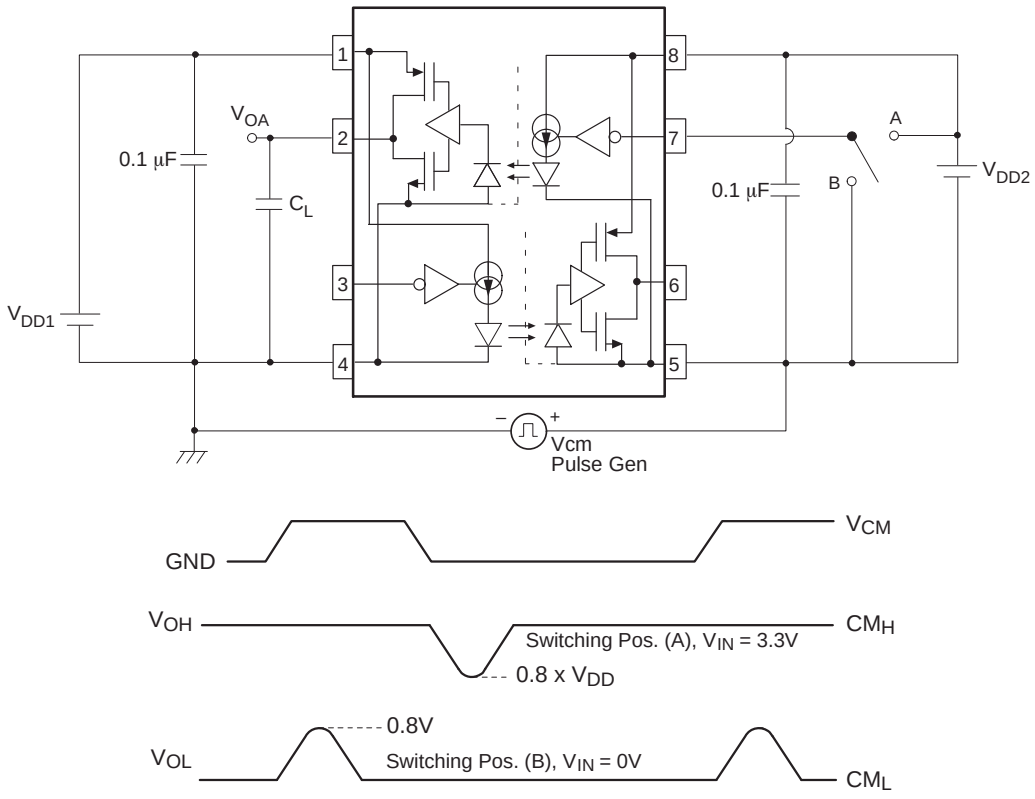


Figure 16. Test Circuit for Instantaneous Common Mode Rejection Voltage

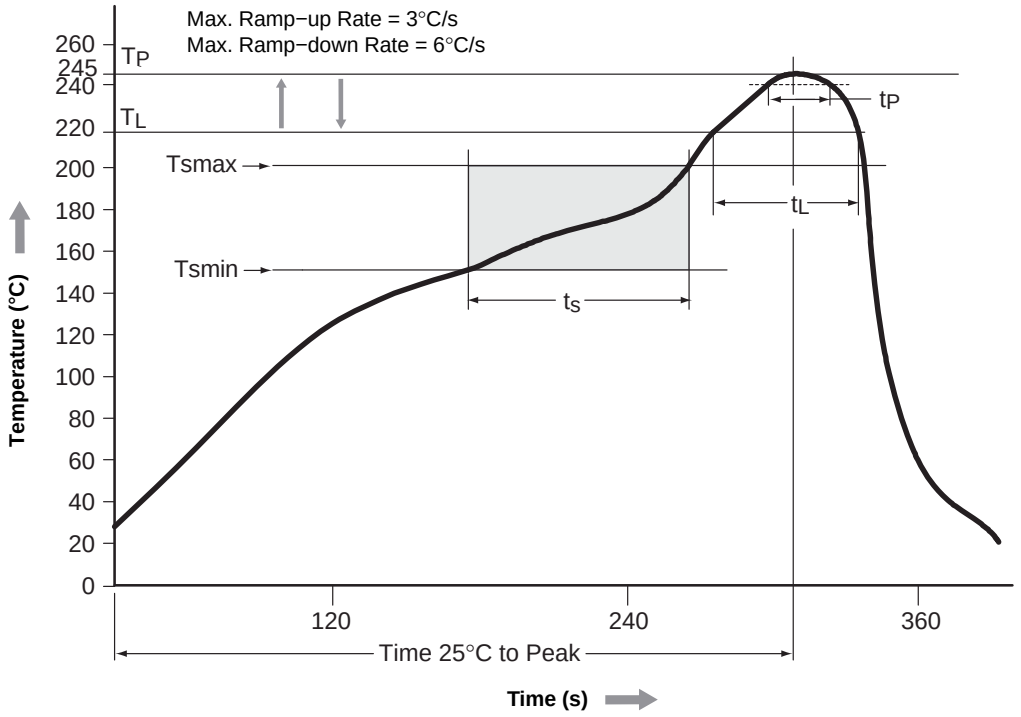
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ORDERING INFORMATION

Option	Order Entry Identifier	Package	Packing Method†
No Suffix	FOD8012A	SOIC8 (Pb−Free)*	Tube (50 Units per Tube)
R2	FOD8012AR2	SOIC8 (Pb−Free)*	Tape and Reel (2,500 Units per Reel)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*All packages are lead free per JEDEC: J−STD−020B standard.

REFLOW PROFILE



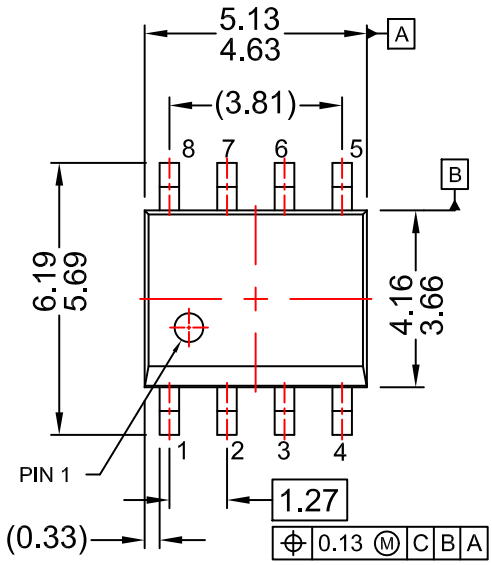
Profile Freature	Pb−Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60 − 120 s
Ramp−up Rate (t_L to t_P)	3°C/s max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 − 150 s
Peak Body Package Temperature	245°C + 0°C / −5°C
Time (t_P) within 5°C of 245°C	30 s
Ramp−down Rate (T_P to T_L)	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

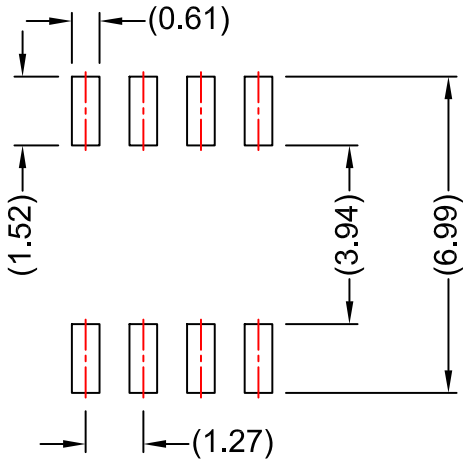
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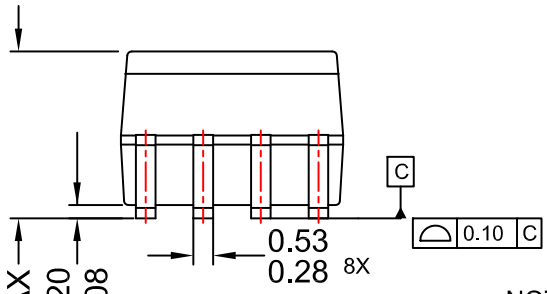
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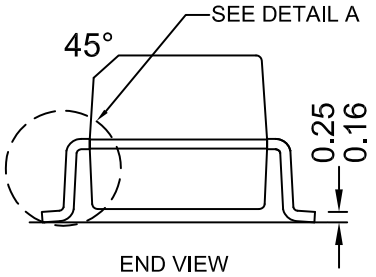
DATE 30 SEP 2016



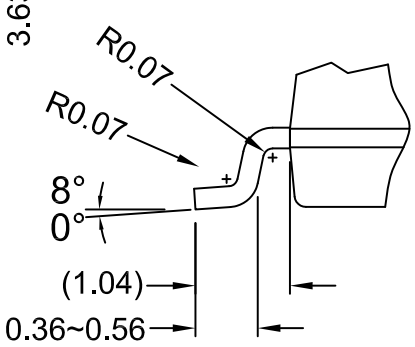


LAND PATTERN RECOMMENDATION





END VIEW



DETAIL A
SCALE: 2:1

NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.

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DESCRIPTION:	**SOIC8**		**PAGE 1 OF 1**

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