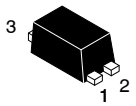
PNP General Purpose Transistor

NST857BF3T5G

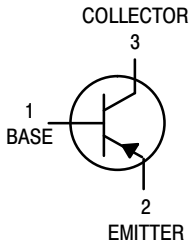


SOT−1123
CASE 524AA
STYLE 1

The NST857BF3T5G device is a spin−off of our popular SOT−23/SOT−323/SOT−563/SOT−963 three−leaded device. It is designed for general purpose amplifier applications and is housed in the SOT−1123 surface mount package. This device is ideal for low−power surface mount applications where board space is at a premium.

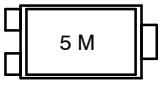
Features

- h_{FE}, 220−475
- Low $V_{CE(sat)}$, ≤ −0.3 V
- Reduces Board Space
- This is a Pb−Free Device



NST857BF3T5G

MARKING DIAGRAM



5 = Device Code
M = Date Code

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CEO}	Collector − Emitter Voltage	−45	Vdc
V_{CBO}	Collector − Base Voltage	−50	Vdc
V_{EBO}	Emitter − Base Voltage	−5.0	Vdc
I_C	Collector Current − Continuous	−100	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
P_D (Note 1)	Total Device Dissipation, T_A = 25°C Derate above 25°C	290 2.3	mW mW/°C
$R_{\theta JA}$ (Note 1)	Thermal Resistance, Junction−to−Ambient	432	°C/W
P_D (Note 2)	Total Device Dissipation, T_A = 25°C Derate above 25°C	347 2.8	mW mW/°C
$R_{\theta JA}$ (Note 2)	Thermal Resistance, Junction−to−Ambient	360	°C/W
$R_{\Psi JL}$ (Note 2)	Thermal Resistance, Junction−to−Lead 3	143	°C/W
T_J, T_{stg}	Junction and Storage Temperature Range	−55 to +150	°C

1. 100 mm^2 1 oz, copper traces.
2. 500 mm^2 1 oz, copper traces.

ORDERING INFORMATION

Device	Package	Shipping†
NST857BF3T5G	SOT−1123 (Pb−Free)	8,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector – Emitter Breakdown Voltage (I_C = –10 mA)	–45	–	–	V
$V_{(BR)CES}$	Collector – Emitter Breakdown Voltage (I_C = –10 μA, V_{EB} = 0)	–50	–	–	V
$V_{(BR)CBO}$	Collector – Base Breakdown Voltage (I_C = –10 μA)	–50	–	–	V
$V_{(BR)EBO}$	Emitter – Base Breakdown Voltage (I_E = –1.0 μA)	–5.0	–	–	V
I_{CBO}	Collector Cutoff Current (V_{CB} = –30 V) (V_{CB} = –30 V, T_A = 150°C)	– –	– –	–15 –4.0	nA μA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (I_C = –10 μA, V_{CE} = –5.0 V) (I_C = –2.0 mA, V_{CE} = –5.0 V)	– 220	150 290	– 475	–
$V_{CE(sat)}$	Collector – Emitter Saturation Voltage (I_C = –10 mA, I_B = –0.5 mA) (I_C = –100 mA, I_B = –5.0 mA)	– –	– –	–0.3 –0.7	V
$V_{BE(sat)}$	Base – Emitter Saturation Voltage (I_C = –10 mA, I_B = –0.5 mA) (I_C = –100 mA, I_B = –5.0 mA)	– –	–0.7 –0.9	– –	V
$V_{BE(on)}$	Base – Emitter On Voltage (I_C = –2.0 mA, V_{CE} = –5.0 V) (I_C = –10 mA, V_{CE} = –5.0 V)	–0.6 –	– –	–0.75 –0.82	V
SMALL– SIGNAL CHARACTERISTICS					
f_T	Current – Gain – Bandwidth Product (I_C = –10 mA, V_{CE} = –5.0 Vdc, f = 100 MHz)	100	–	–	MHz
C_{obo}	Output Capacitance (V_{CB} = –10 V, f = 1.0 MHz)	–	–	4.5	pF
C_{ibo}	Input Capacitance (V_{EB} = –0.5 V, I_C = 0 mA, f = 1.0 MHz)	–	–	10	pF
NF	Noise Figure (I_C = –0.2 mA, V_{CE} = –5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	–	–	10	dB

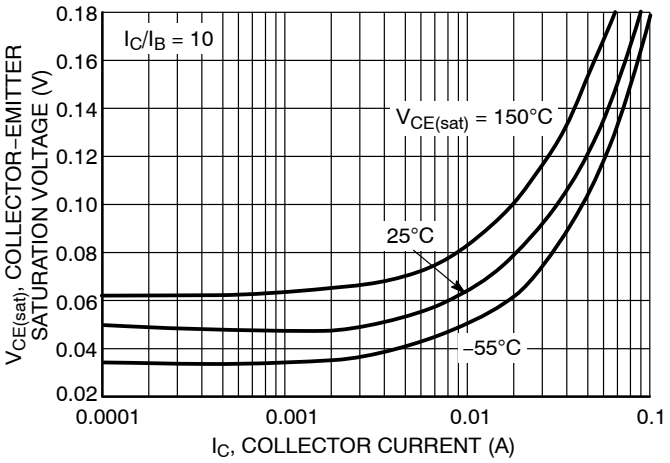


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

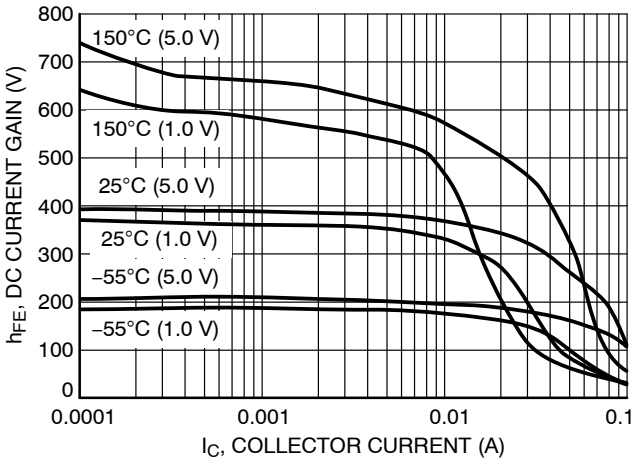


Figure 2. DC Current Gain vs. Collector Current

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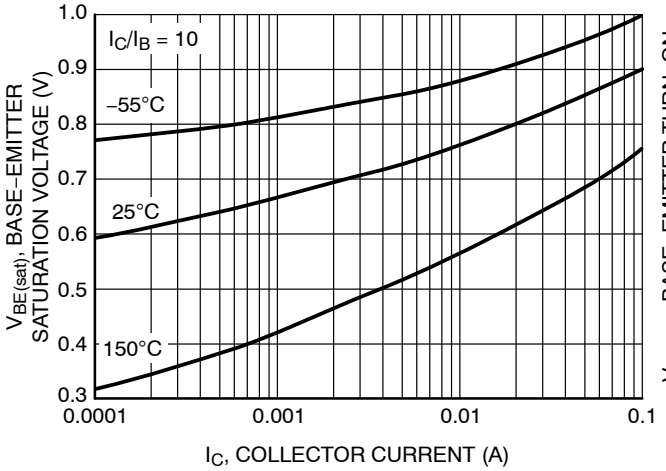


Figure 3. Base Emitter Saturation Voltage vs. Collector Current

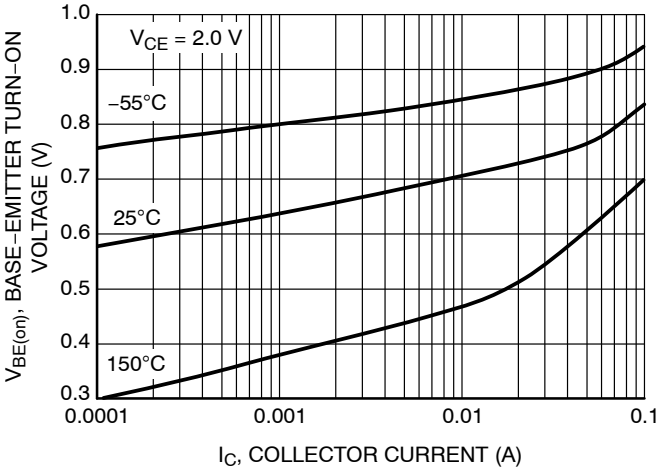


Figure 4. Base Emitter Turn−On Voltage vs. Collector Current

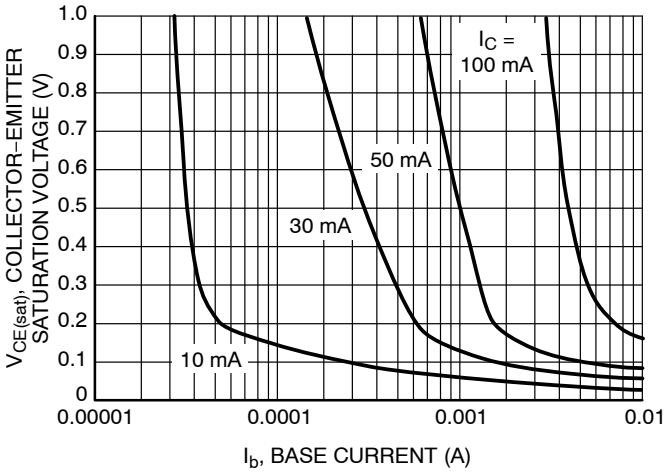


Figure 5. Saturation Region

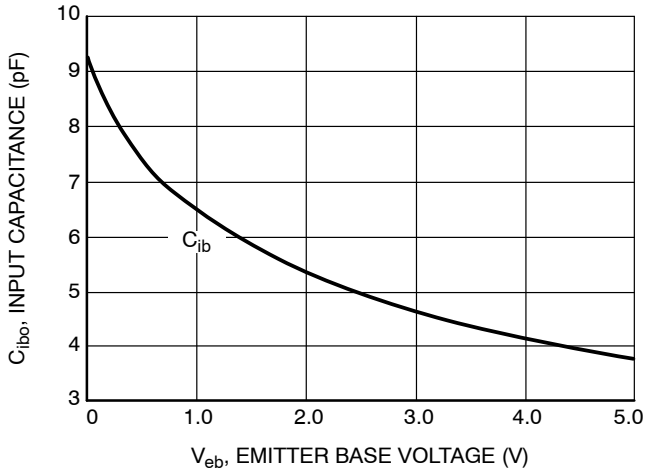


Figure 6. Input Capacitance

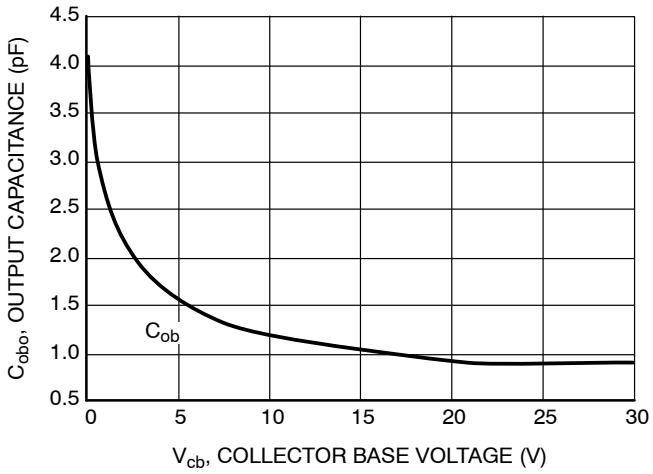
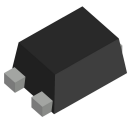


Figure 7. Output Capacitance

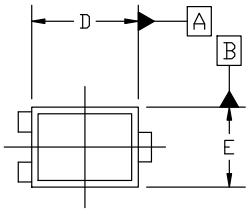
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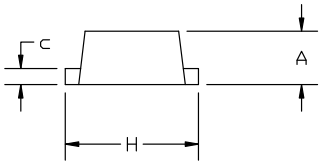


SOT−1123 0.80x0.60x0.37, 0.35P
CASE 524AA
ISSUE D

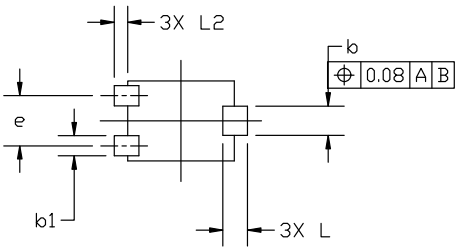
DATE 18 JAN 2024



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

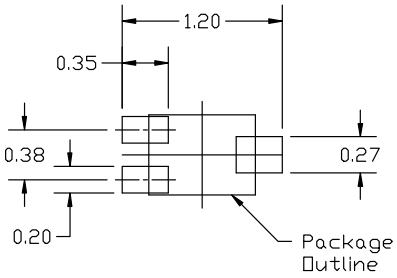
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.15	0.22	0.28
b1	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
e	0.35	0.38	0.40
H	0.950	1.000	1.050
L	0.185 REF		
L2	0.05	0.10	0.15

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

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