

ESD PROTECTION DEVICE
STAND-OFF VOLTAGE - 5.0 Volts
POWER DISSIPATION - 50 Watts
GENERAL DESCRIPTION

The L05ESDL5V0NA-4 is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over voltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

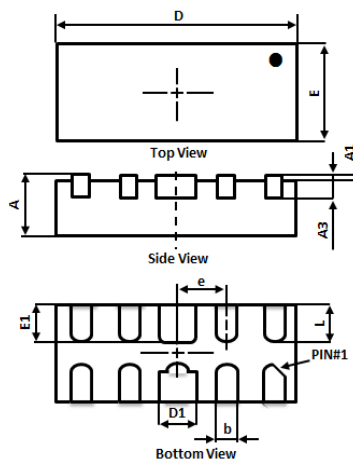
- Flow-through design
- Protects four I/O lines (Data line)
- Max. peak pulse power: P_{pp}=50w at t_p = 8/20 us.
- Low capacitance: 0.3pF typical (I/O to I/O)
- IEC 61000-4-2, level 4 (ESD), >±15KV(air)
; >±8KV(contact)

MECHANICAL DATA

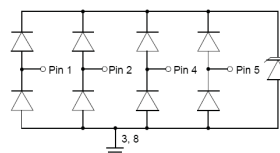
- Case material: "Green" molding compound UL flammability classification 94V-0 (No Br, Sb, Cl), "Halogen-free"
- Terminals: lead free plating (matte tin finish)
- Component in accordance to RoHs 2011/65/EU

APPLICATION

- High definition multi-media interface (HDMI)
- Digital visual interface (DVI)
- Display protTM interface
- MDDI ports
- LVDS
- SATA
- USB 3.0/3.1

SLP2510P8


SLP2510P8		
DIM.	MIN.	MAX.
A	0.45	0.55
A1	0.00	0.05
A3	0.152 REF.	
D	2.45	2.55
E	0.95	1.05
D1	0.35	0.45
E1	0.35	0.45
b	0.15	0.25
e	0.50 BSC	
L	0.35	0.45
All dimension in millimeter		



PIN ASSIGNMENT	
1,2,4,5	Input lines
6,7,9,10	NC
3,8	Ground

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

ABSOLUTE RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power (t _p = 8/20us)	P _{pk}	50	W
Peak pulse current (t _p = 8/20us)	I _{pp}	4.5	A
Operating junction temperature range	T _J	-55 to +125	°C
Storage temperature range	T _{STG}	55 to +150	°C
Soldering temperature, t max = 10s	T _L	260	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Reverse standoff voltage	Any I/O pin to ground	V _{RWM}	--	--	5.0	V
Reverse leakage current	V _{DRM} = 5V	I _{RM}	--	--	1.0	uA
Breakdown voltage	I _R = 1 mA	V _{BR}	6.0	--	--	V
Forward voltage	I _F = 15 mA, pin 3,8 to pin 1,2,4,5 @ T _J = 25°C	V _F	--	0.85	1.1	V
Clamping Voltage	I _{pp} = 4.5A, t _p = 8/20 us	V _C	--	--	10	V
Junction capacitance	VR = 0V, f = 1MHz, between I/O pins	C _J	--	0.3	0.4	pF
	VR = 0V, f = 1MHz, any I/O pin to ground		--	--	0.8	

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RATING AND CHARACTERISTIC CURVES L05ESDL5V0NA-4



FIG.1- 8/20us pulse waveform according to IEC 61000-4-5

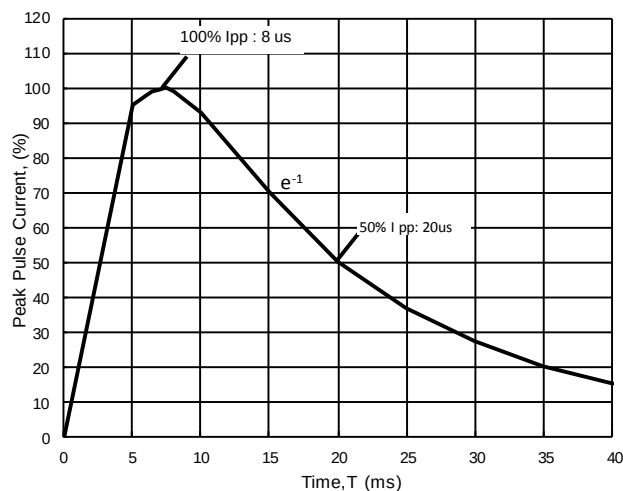


FIG.2- ESD pulse waveform according to IEC 61000-4-2

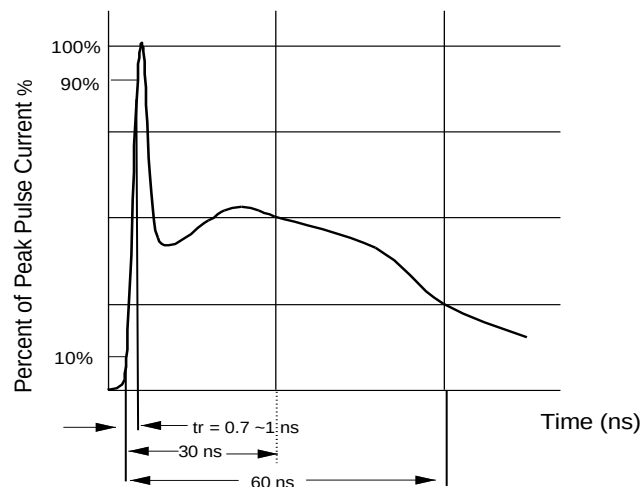


FIG3- Power dissipation versus pulse time

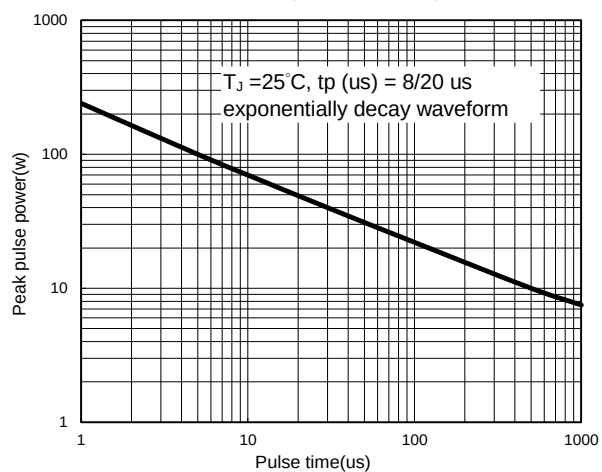


FIG4- Peak pulse power versus Tj

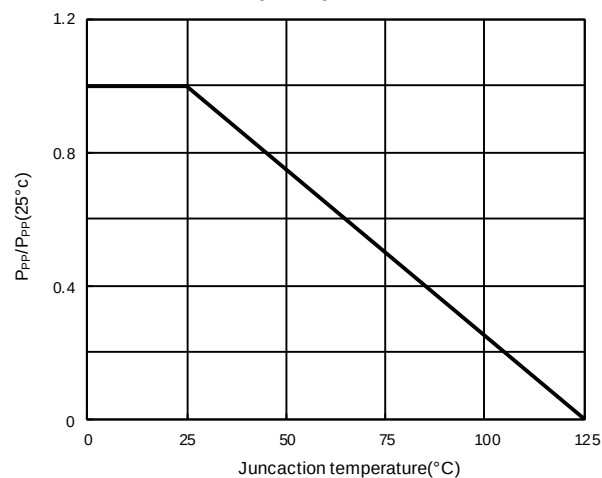


FIG.5- Typical junction capacitance

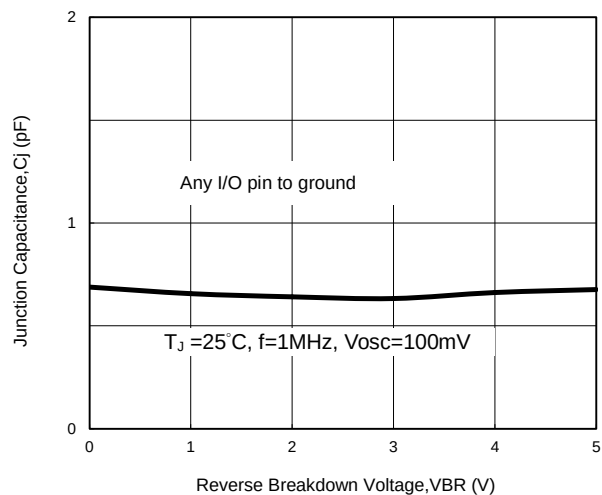
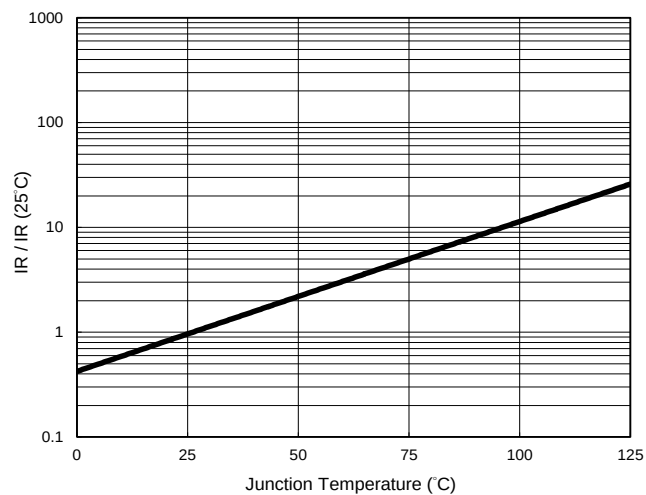


FIG.6- reverse leakage current versus Tj



RATING AND CHARACTERISTIC CURVES
L05ESDL5V0NA-4

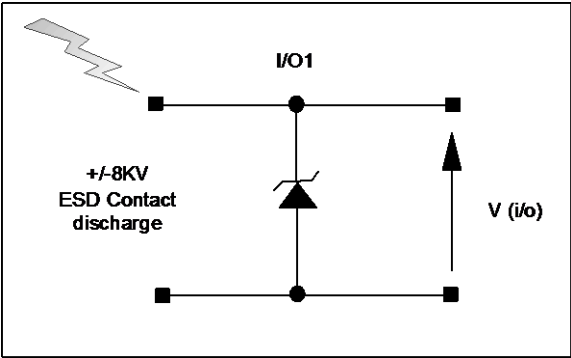


Figure 7. ESD Test Configuration

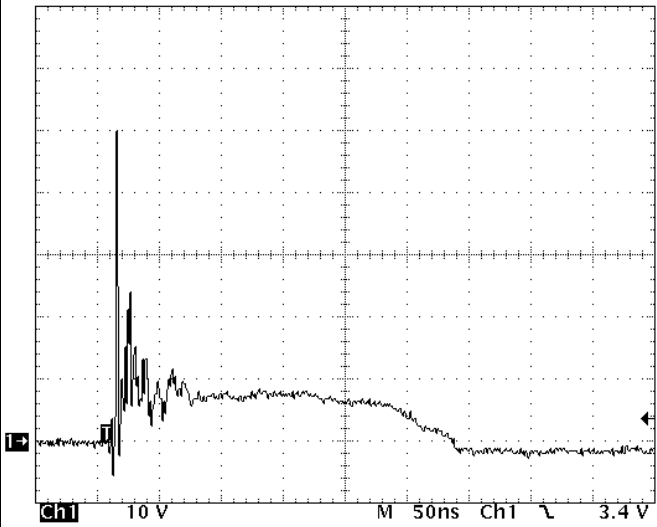


Figure 8. Clamped +8 kV ESD voltage waveform

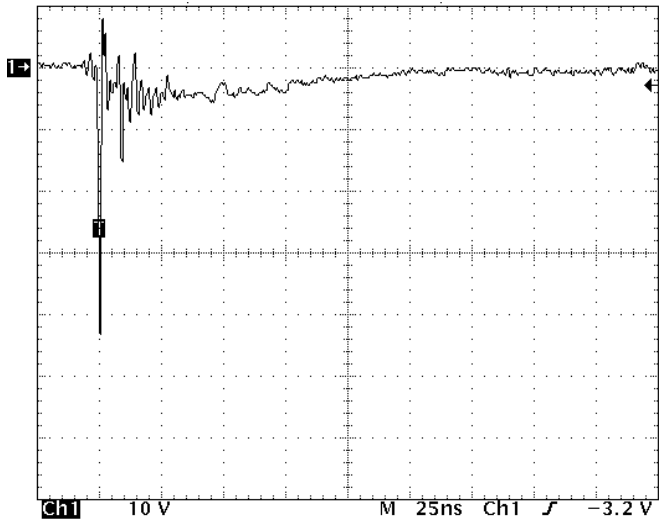


Figure 9. Clamped -8 kV ESD voltage waveform

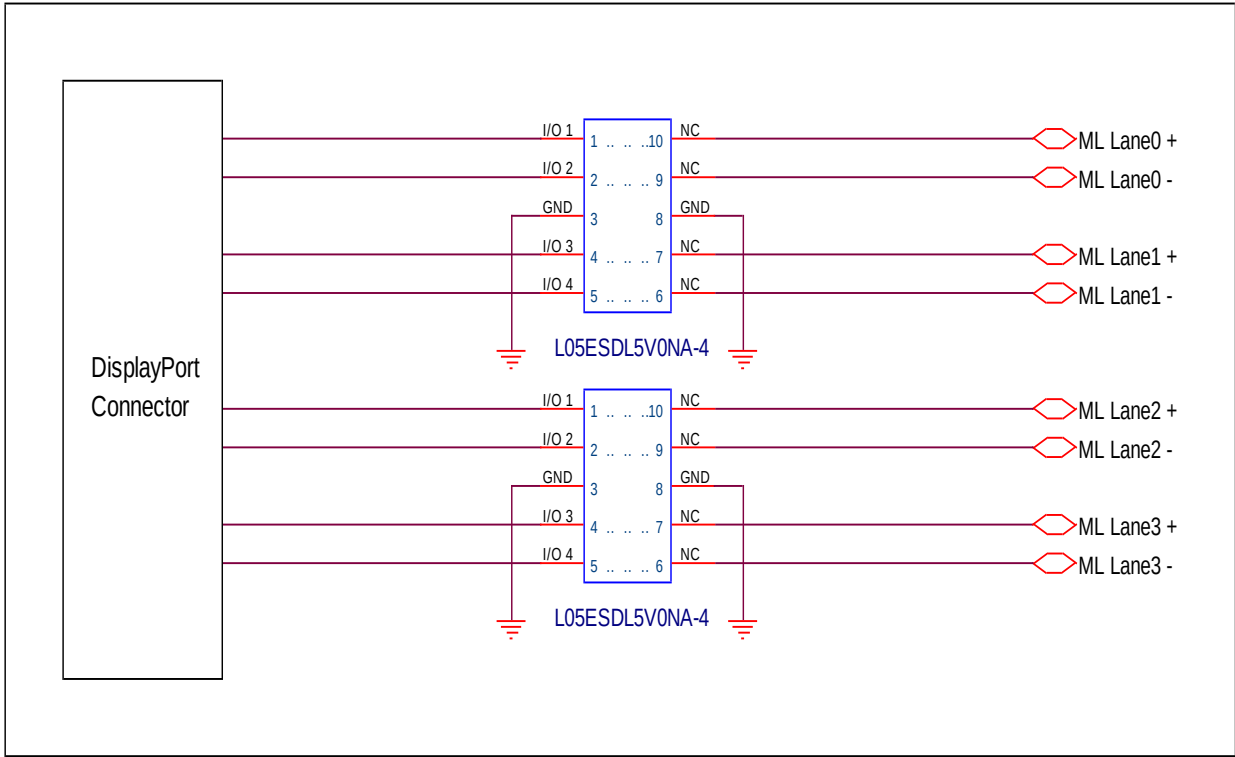


Figure 12. Display Port ESD Protection

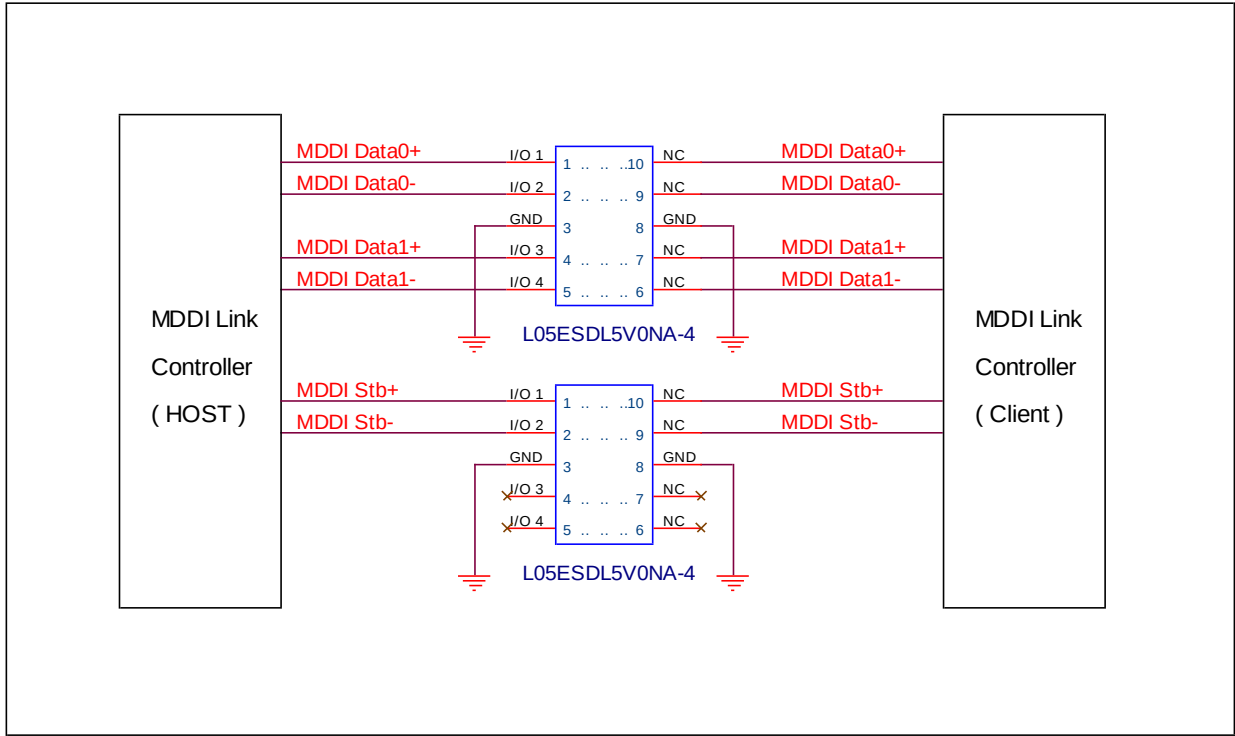


Figure 13. MDDI Interface ESD Protection

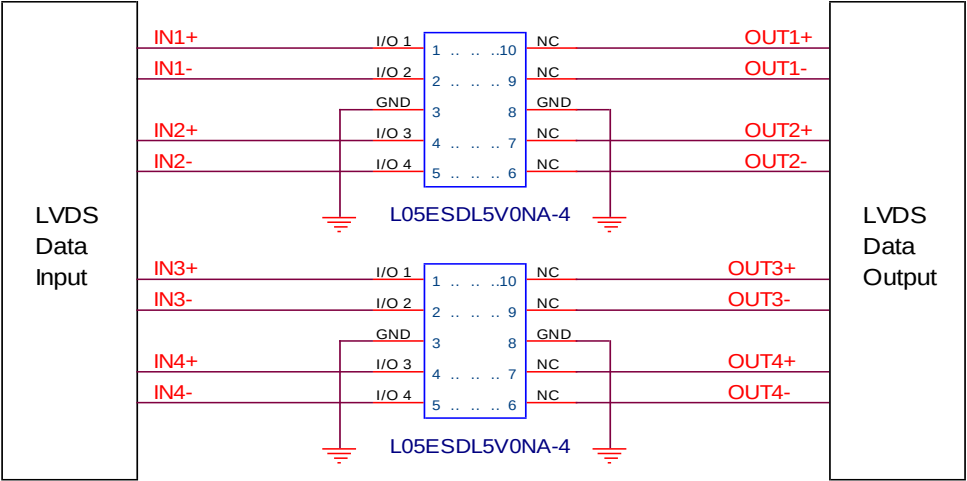


Figure 14. LVDS Interface ESD Protection

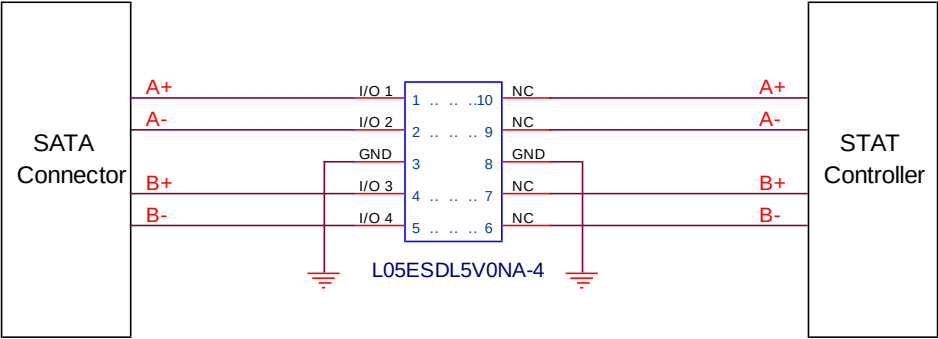
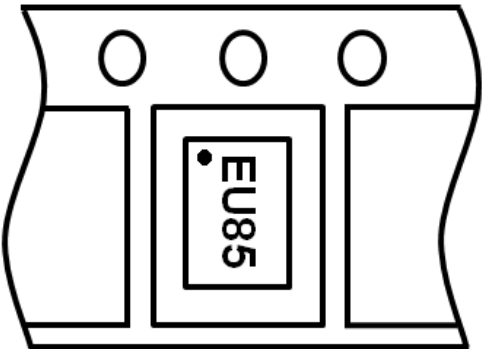


Figure 15. Serial ATA ESD Protection

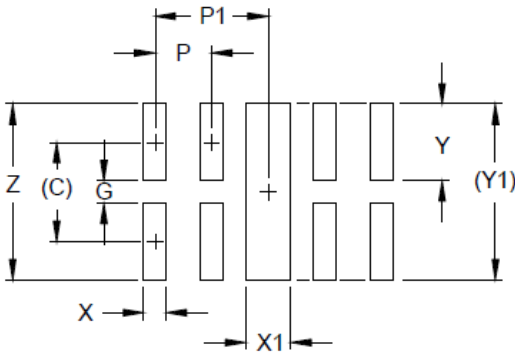
Marking and Orientation :



Packaging Information :

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L05ESDL5V0NA-4	3000	7	45000	90K/180K

SLP2510P8 Soldering Pad Layout :



DIM.	MILLIMETERS	INCHES
C	(0.875)	(0.034)
G	0.20	0.008
P	0.50	0.020
P1	1.00	0.039
X	0.20	0.008
X1	0.40	0.016
Y	0.68	0.027
Y1	(1.550)	(0.061)
Z	1.550	0.061

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