NEC

MOS Integrated Circuit

V850ES/HF2

32-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The V850ES/HF2 is a 32-bit single chip microcontroller of the V850ES series. 32-bit CPU, ROM, RAM, timer/counters, serial interface, A/D converter and so on are integrated on a single chip.

FEATURES

- V850ES core, 32-bit RISC architecture
- Instruction execution time: 50ns(min.) @20MHz , Integrated PLL(x4) circuit
- On-chip high-capacity ROM , RAM

Type / Part Number	Program Memory (Flash Memory Size)	Data Memory (RAM Size)
μPD70F3702	**64KB**	**12KB**
μPD70F3703	**128KB**	**12KB**
μPD70F3704	**256KB**	**12KB**

- Timer:
  - 16-bit timer(Type TMP) : 4 channels
  - 16-bit timer(Type TMQ) : 1 channel
  - 16-bit timer(Type TMM) : 1 channel
  - Watch timer : 1 channel
  - Watchdog timer : 1 channel
- Serial interface :
  - UART : 2 channels
  - CSI : 2 channels
- A/D converter : 10-bit resolution : 12 channels
- On-chip debug function : JTAG interface (N-wire type)
- Operation Voltage :
  - 3.5V to 5.5V : 20MHz max. (OSC=5MHz x4)
- Package : 80-pin plastic TQFP (12 x 12mm, 0.5mm pitch)

Please note: The information in this document is subject to change without notice

Function Table

Device name		V850ES /HE2	V850ES/HF2			V850ES /HG2	V850ES /HJ2
			μPD 70F3702	μPD 70F3703	μPD 70F3704		
CPU core		V850ES					
CPU performance		29MIPS(@20MHz)					
Internal flash memory		64KB/128KB	64KB	128KB	256KB	128KB/256KB	128KB/256KB/ 376KB/512KB
Internal RAM		6KB	12KB			12KB	12KB/ 20KB
External bus interface	Bus type	-	-			-	Multiplexed
	Address bus	-	-			-	16 bits
	Data bus	-	-			-	8/16 bits
	Chip select signal	-	-			-	4
Interrupt sources	Internal	32	32			43	50/52
	External	9	9			12	16
Timer/counter		TMM x 1ch TMP x 4ch TMQ x 1ch Watch x 1ch WDT x 1ch	16-bit interval timer (TMM) x 1ch 16-bit timer (TMP) x 4ch 16-bit timer (TMQ) x 1ch Watch timer x 1 ch Watchdog timer x 1 ch			TMM x 1ch TMP x 4ch TMQ x 2ch Watch x 1ch WDT x 1ch	TMM x 1 ch TMP x 4 ch TMQ x 3 ch Watch x 1 ch WDT x 1 ch
Serial interface		CSI x 2 ch UART x 2 ch	CSI x 2 ch UART(LIN compatible) x 2 ch			CSI x 2 ch UART x 3 ch	CSI x 3 ch UART x 3 ch or 4 ch
A/D converter		10-bit x 10ch	10-bit x 12ch			10-bit x 16ch	10-bit x 24 ch
DMA controller		–	–			4 ch	4 ch
Ports	I/O	51	67			84	128
Debug control unit		Provided (RUN/break)					
Other peripheral functions		LVI/Clock monitor Key return input					
Operating frequency		When using main clock : 16 to 20MHz When using subclock : 32.768kHz Internal oscillation clock : Typ.200kHz					
Power supply voltage		3.5 to 5.5V (@20MHz)					
Package		64-pin LQFP (10x10 mm)	80-pin TQFP (12x12 mm)			100-pin LQFP (14x14 mm)	144-pin LQFP (20 x 20 mm)
Operating ambient temperature		-40°C to +85°C					

Serial interface functions overview

Function	Overview
CSI	➢ Master mode and slave mode selectable ➢ 3-wire serial interface for 8-bit to 16-bit transfer ➢ Interrupt request signals (INTCBnT and INTCBnR) ➢ Serial clock and data phase selectable ➢ Transfer data length selectable from 8 to 16 bits in 1-bit units ➢ Data transfer with MSB- or LSB-first selectable ➢ 3-wire SOBn : Serial data output SIBn : Serial data input SCKBn : Serial clock I/O ➢ Transmission mode, reception mode, and transmission/reception mode selectable **Remark** n = 0, 1
UART	➢ Transfer rate : 300 bps to 312.5 kbps (using internal system clock of 20MHz and dedicated baud rate generator) ➢ Full-duplex communication: UARTA receive data register n (UAnRX) UARTA transmit data register n (UAnTX) ➢ 2-pin configuration: TXDAn: Output pin of transmit data RXDAn: Input pin of receive data ➢ Reception error detection function ✓ Parity error ✓ Framing error ✓ Overrun error ➢ Interrupt sources: 2 types ✓ Reception complete interrupt (INTUAnR): An interrupt is generated in the reception enabled status by ORing three types of reception errors. It is also generated when receive data is transferred from the shift register to receive buffer register n after completion of serial transfer. ✓ Transmission enable interrupt (INTUAnT): Generated when transmit data is transferred from the transmit buffer register to the shift register in the transmission enabled status. ➢ Character length of transmit/receive data is specified by the UAnCTL0 register. ➢ Character length: 7 or 8 bits ➢ Parity function: Odd, even, 0, none ➢ Transmission stop bit: 1 or 2 bits ➢ Dedicated baud rate generator ➢ MSB/LSB first transfer selectable ➢ Transmit/receive data reversible ➢ 13 to 20 bits selectable for SBF (Sync Break Field) transmission in LIN (Local interconnect Network) communication format ➢ 11 or more bits recognizable for SBF reception in LIN communication format ➢ SBF reception flag **Remark** n = 0, 1

Timer functions overview

Function	Overview
16-bit interval timer (TMM)	➢ Interval function ➢ Clock selection x 8 ➢ Simple counter x 1 (The simple counter is a counter that does not use a counter read buffer. This counter cannot be read during timer count operation.) ➢ Simple compare x 1 (The simple compare register is a register that does not use a compare write buffer. No data can be written to this compare register during timer count operation.) ➢ Compare match interrupt x 1
16-bit timer/event counter (TMP)	➢ PWM output ➢ Interval timer ➢ External event counter (operation disabled when clock is stopped) ➢ One-shot pulse output ➢ Pulse width measurement function ➢ Timer synchronized operation function ➢ Free-running function ➢ External trigger pulse output function ➢ Capture trigger input signal x 2 ➢ External trigger input signal x 1 ➢ Clock selection x 8 ➢ External event count input x 1 ➢ Readable counter x 1 ➢ Capture/compare reload register x 2 ➢ Capture/compare match interrupt x 2 ➢ Timer output (TOPn0, TOPn1) x 2 **Remark** n = 0 to 3
16-bit timer/event counter (TMQ)	➢ PWM output ➢ Interval timer ➢ External event counter (operation disabled when clock is stopped) ➢ One-shot pulse output ➢ Pulse width measurement function ➢ Triangular wave PWM output ➢ Timer synchronized operation function ➢ Capture trigger input signal x 4 ➢ External trigger input signal x 1 ➢ Clock selection x 8 ➢ External event count input x 1 ➢ Readable counter x 1 ➢ Capture/compare reload register x 4 ➢ Capture/compare match interrupt x 4 ➢ Timer output (TOQ00 to TOQ03) x 4
Watch timer	➢ Watch timer The watch timer generates an interrupt request (INTWT) at time intervals of 0.5 or 0.25 seconds by using the subclock (f_{XT} = 32.768 kHz) ➢ Interval timer The watch timer generates an interrupt request (INTWTI) at time intervals specified in advance. ➢ The watch timer and interval timer functions can be used at the same time.
Watchdog timer 2	➢ Default-start watchdog timer ✓ Reset mode: Reset operation upon overflow of watchdog timer 2 (generation of WDT2RES signal) ✓ Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer 2 (generation of INTWDT2 signal) ➢ Input selectable from main clock and internal oscillation clock as the source clock.

Other functions overview(1/2)

Function	Overview
A/D converter	➢ 10-bit resolution ➢ 12 channels ➢ Successive approximation method ➢ Operating voltage: AV_{REF0} = 4.0 to 5.5 V ➢ Analog input voltage: 0 V to AV_{REF0} ➢ The following functions are provided as operation modes. ✓ Continuous select mode ✓ Continuous scan mode ✓ One-shot scan mode ➢ The following functions are provided as trigger modes. ✓ Software trigger mode ✓ External trigger mode (external, 1) ✓ Timer trigger mode ➢ Power-fail monitor function (conversion result compare function)
Interrupt/exception Processing	➢ Interrupts ✓ Non-maskable interrupts: 2 sources ✓ Maskable interrupts: External: 8, Internal: 31 sources ✓ 8 levels of programmable priorities (maskable interrupts) ✓ Multiple interrupt control according to priority ✓ Masks can be specified for each maskable interrupt request ✓ Noise elimination, edge detection, and valid edge specification for external interrupt request signals ➢ Exceptions ✓ Software exceptions: 32 sources ✓ Exception trap: 2 sources (illegal op code exception, debug trap)
Key interrupt	➢ A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7) by setting the key return mode register (KRM).
Standby	➢ The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. ✓ HALT mode: Mode in which only the operating clock of the CPU is stopped ✓ IDLE1 mode: Mode in which all the internal operations of the chip except the oscillator, PLL, and flash memory are stopped ✓ IDLE2 mode: Mode in which all the internal operations of the chip except the oscillator are stopped ✓ STOP mode: Mode in which all the internal operations of the chip except the subclock oscillator are stopped ✓ Subclock operation mode: Mode in which the subclock is used as the internal system clock ✓ Sub-IDLE mode: Mode in which all the internal operations of the chip except the oscillator, PLL and flash memory are stopped, in the subclock operation mode

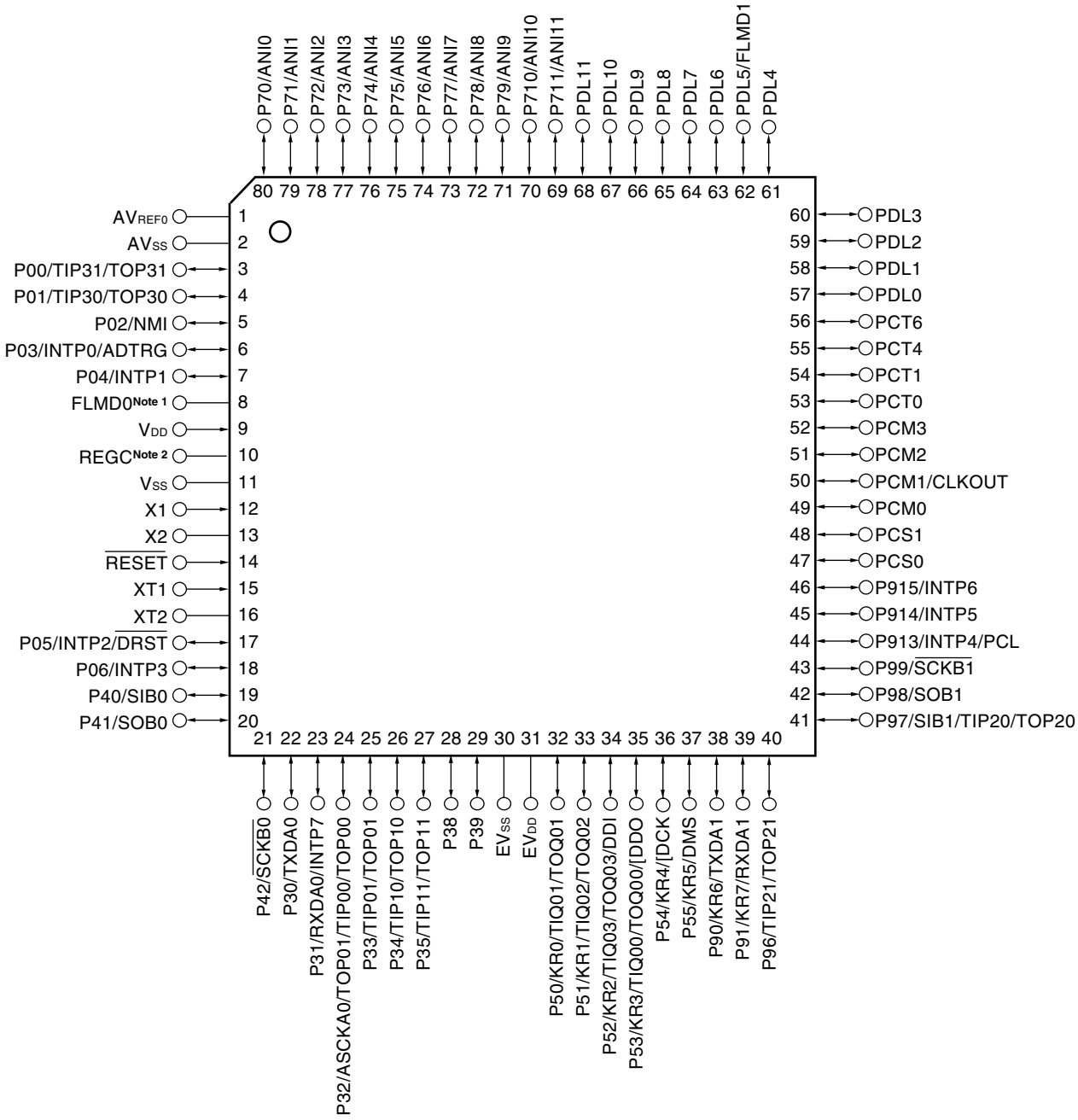
Other functions overview(2/2)

Function	Overview
Clock monitor	➢ The clock monitor samples the main clock by using the internal oscillation clock and generates a reset request signal when oscillation of the main clock is stopped. ➢ Once the operation of the clock monitor has been enabled by an operation enable flag, it cannot be cleared to 0 by any means other than reset. ➢ The clock monitor automatically stops under the following conditions. ✓ While oscillation stabilization time is being counted after software STOP mode is released ✓ When the main clock is stopped (MCK bit of the PCC register = 1 during subclock operation, or CLS bit of the PCC register = 0 during main clock operation) ✓ When the sampling clock is stopped (Internal oscillation clock) ✓ When the CPU operates with the internal oscillation clock
Low-voltage Detector (LVI)	➢ Compares the supply voltage (V_{DD}) and detected voltage (V_{LVI}) and generates an internal interrupt signal or internal reset signal when $V_{DD} < V_{LVI}$. ➢ The level of the supply voltage to be detected can be changed by software (in two steps). ➢ Interrupt or reset signal can be selected by software. ➢ Can operate in STOP mode too. ➢ Operation can be stopped by software.

Pin configuration (Top View)

80-pin plastic TQFP (fine pitch) (12 x 12)

μPD70F3702GK-9EU-A
μPD70F3703GK-9EU-A
μPD70F3704GK-9EU-A



Notes **1.** FLMD0 pin: Connect to V_{SS} in normal operation mode.

2. To stabilize the output voltage of the regulator, connect a capacitor (4.7 μF) to the REGC pin.

Caution Make EV_{DD} the same potential as V_{DD}.

Pin Functions

(1) Port pins

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Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 7-bit I/O port Input/output can be specified in 1-bit units.	TIP31/TOP31
P01			TIP30/TOP30
P02			NMI
P03			INTP0/ADTRG
P04			INTP1
P05			INTP2/$\overline{\text{DRST}}$
P06			INTP3
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TXDA0
P31			RXDA0/INTP7
P32			ASCKA0/TIP00/TOP00/TOP01
P33			TIP01/TOP01
P34			TIP10/TOP10
P35			TIP11/TOP11
P38			–
P39			–
P40	I/O	Port 4 3-bit I/O port Input/output can be specified in 1-bit units.	SIB0
P41			SOB0
P42			$\overline{\text{SCKB0}}$
P50	I/O	Port 5 6-bit I/O port Input/output can be specified in 1-bit units.	KR0/TIQ01/TOQ01
P51			KR1/TIQ02/TOQ02
P52			KR2/TIQ03/TOQ03/DDI
P53			KR3/TIQ00/TOQ00/DDO
P54			KR4/DCK
P55			KR5/DMS

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Pin Name	I/O	Function	Alternate Function
P70 to P711	I/O	Port 7 12-bit I/O port Input/output can be specified in 1-bit units.	ANI0 to ANI11
P90	I/O	Port 9 9-bit I/O port Input/output can be specified in 1-bit units.	KR6/TXDA1
P91			KR7/RXDA1
P96			TIP21/TOP21
P97			SIB1/TIP20/TOP20
P98			SOB1
P99			$\overline{\text{SCKB1}}$
P913			INTP4/PCL
P914			INTP5
P915			INTP6
PCM0	I/O	Port CM 4-bit I/O port Input/output can be specified in 1-bit units.	–
PCM1			CLKOUT
PCM2, PCM3			–
PCS0, PCS1	I/O	Port CS 2-bit I/O port Input/output can be specified in 1-bit units.	–
PCT0, PCT1, PCT4, PCT6	I/O	Port CT 4-bit I/O port Input/output can be specified in 1-bit units.	–
PDL0 to PDL4	I/O	Port DL 8-bit I/O port Input/output can be specified in 1-bit units.	–
PDL5			FLMD1
PDL6 to PDL11			–

(2) Non-port pins

(1/3)

Pin Name	I/O	Function	Alternate Function
NMI	Input	External interrupt input (non-maskable, with analog noise eliminated)	P02
INTP0	Input	External interrupt request input (maskable, with analog noise eliminated)	P03/ADTRG
INTP1			P04
INTP2			P05/$\overline{\text{DRST}}$
INTP3			P06
INTP4			P913/PCL
INTP5			P914
INTP6			P915
INTP7			P31/RXDA0
TIP00	Input	External event/clock input (TMP00)	P32/ASCKA0/TOP00/TOP01
TIP01		External event input (TMP01)	P33/TOP01
TIP10		External event/clock input (TMP10)	P34/TOP10
TIP11		External event input (TMP11)	P35/TOP11
TIP20		External event/clock input (TMP20)	P97/SIB1/TOP20
TIP21		External event input (TMP21)	P96/TOP21
TIP30		External event/clock input (TMP30)	P01/TOP30
TIP31		External event input (TMP31)	P00/TOP31
TOP00	Output	Timer output (TMP00)	P32/ASCKA0/TIP00/TOP01
TOP01		Timer output (TMP01)	P32/ASCKA0/TIP00/TOP00
			P33/TIP01
TOP10		Timer output (TMP10)	P34/TIP10
TOP11		Timer output (TMP11)	P35/TIP11
TOP20		Timer output (TMP20)	P97/SIB1/TIP20
TOP21		Timer output (TMP21)	P96/TIP21
TOP30		Timer output (TMP30)	P01/TIP30
TOP31		Timer output (TMP31)	P00/TIP31

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Pin Name	I/O	Function	Alternate Function
TIQ00	Input	External event/clock input (TMQ00)	P53/KR3/TOQ00/DDO
TIQ01		External event input (TMQ01)	P50/KR0/TOQ01
TIQ02		External event input (TMQ02)	P51/KR1/TOQ02
TIQ03		External event input (TMQ03)	P52/KR2/TOQ03/DDI
TOQ00	Output	Timer output (TMQ00)	P53/KR3/TIQ00/DDO
TOQ01		Timer output (TMQ01)	P50/KR0/TIQ01
TOQ02		Timer output (TMQ02)	P51/KR1/TIQ02
TOQ03		Timer output (TMQ03)	P52/KR2/TIQ03/DDI
SIB0	Input	Serial receive data input (CSIB0)	P40
SIB1		Serial receive data input (CSIB1)	P97/TIP20/TOP20
SOB0	Output	Serial transmit data output (CSIB0)	P41
SOB1		Serial transmit data output (CSIB1)	P98
$\overline{\text{SCKB0}}$	I/O	Serial clock I/O (CSIB0)	P42
$\overline{\text{SCKB1}}$		Serial clock I/O (CSIB1)	P99
RXDA0	Input	Serial receive data input (UARTA0)	P31/INTP7
RXDA1		Serial receive data input (UARTA1)	P91/KR7
TXDA0	Output	Serial transmit data output (UARTA0)	P30
TXDA1		Serial transmit data output (UARTA1)	P90/KR6
ASCKA0	Input	Baud rate clock input to UARTA0	P32/TIP00/TOP00/TOP01
ANI0 to ANI11	Input	Analog voltage input to A/D converter	P70 to P711
AV_{REF0}	Input	Reference voltage input to A/D converter (same potential as V_{DD})	–
AV_{SS}	–	Ground potential for A/D and D/A converters (same potential as V_{SS})	–
ADTRG	Input	A/D converter external trigger input	P03/INTP0
KR0	Input	Key interrupt input	P50/TIQ01/TOQ01
KR1			P51/TIQ02/TOQ02
KR2			P52/TIQ03/TOQ03/DDI
KR3			P53/TIQ00/TOQ00/DDO
KR4			P54/DCK
KR5			P55/DMS
KR6			P90/TXDA1
KR7			P91/RXDA1

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Pin Name	I/O	Function	Alternate Function
DMS	Input	Debug mode select	P55/KR5
DDI	Input	Debug data input	P52/KR2/TIQ03/TOQ03
DDO	Output	Debug data output	P53/KR3/TIQ00/TOQ00
DCK	Input	Debug clock input	P54/KR4
$\overline{\text{DRST}}$	Input	Debug reset input	P05/INTP2
FLMD0	Input	Flash programming mode setting pins	–
FLMD1			PDL5
CLKOUT	Output	Internal system clock output	PCM1
PCL	Output	Clock output (timing output of X1 input clock and subclock)	P913/INTP4
REGC	–	Regulator output stabilizing capacitor connection	–
$\overline{\text{RESET}}$	Input	System reset input	–
X1	Input	Main clock resonator connection	–
X2	–		–
XT1	Input	Subclock resonator connection	–
XT2	–		–
V_{DD}	–	Positive power supply pin for internal circuitry	–
V_{SS}	–	Ground potential for internal circuitry	–
EV_{DD}	–	Positive power supply pin for external circuitry (same potential as V_{DD})	–
EV_{SS}	–	Ground potential for external circuitry (same potential as V_{SS})	–