

## TLC6C5912-Q1 Power Logic 12-Channel Shift Register LED Driver

### 1 Features

- Qualified for Automotive Applications
- Wide  $V_{CC}$  Range from 3 V to 5.5 V
- Output Maximum Rating of 40 V
- Twelve Power DMOS Transistor Outputs of 50-mA Continuous Current With  $V_{CC} = 5$  V
- Thermal Shutdown Protection
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption
- Slow Switching Time ( $t_r$  and  $t_f$ ), Which Helps Significantly With Reducing EMI
- 20-Pin TSSOP-PW Package
- 20-Pin DW Package

### 2 Applications

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls

### 3 Description

The TLC6C5912-Q1 is a monolithic, medium-voltage, low-current power 12-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear (CLR) is high. A low on CLR clears all registers in the device. Holding the output enable ( $\overline{G}$ ) high holds all data in the output buffers low, and all drain outputs are off. Holding  $\overline{G}$  low makes data from the storage register transparent to the output buffers.

When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. The device contains a built-in thermal shutdown protection.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50-mA continuous sink-current capabilities when  $V_{CC} = 5$  V. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2000 V of ESD protection when tested using the human-body model and 200 V when tested using the machine model.

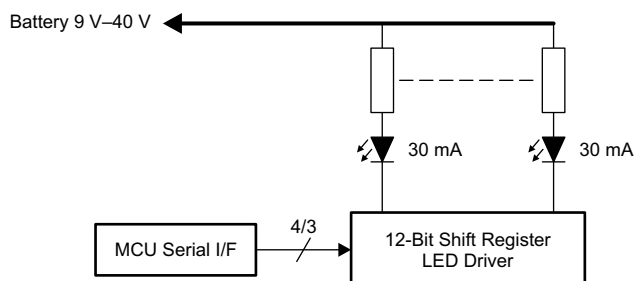
The TLC6C5912-Q1 characterization is for operation over the operating ambient temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC6C5912-Q1	SOIC (20)	12.80 mm x 7.50 mm
	TSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Schematic



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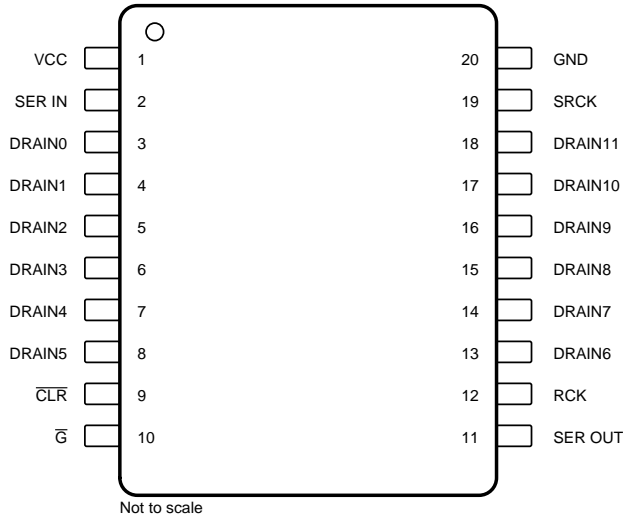
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

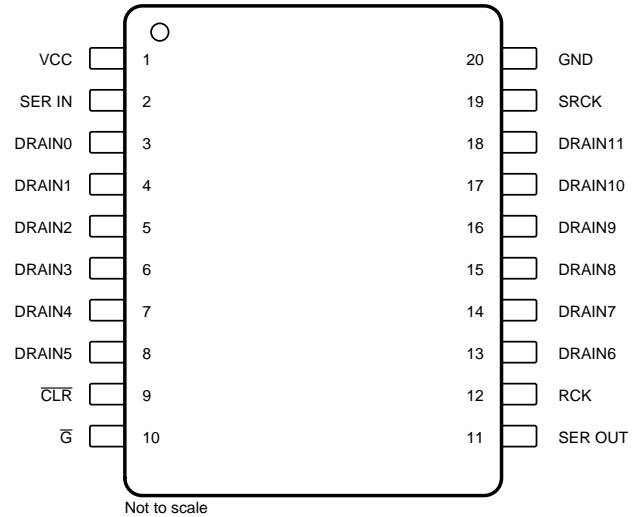
<b>Changes from Revision B (December 2015) to Revision C</b> .....	<b>Page</b>
• Changed $r_{DS(on)}$ test condition from 50 mA to 20 mA .....	5
• Added the <i>Receiving Notification of Documentation Updates</i> section .....	16
<b>Changes from Revision A (January 2013) to Revision B</b> .....	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
<b>Changes from Original (December 2012) to Revision A</b> .....	<b>Page</b>
• Changed the device status from PRODUCT PREVIEW to PRODUCTION DATA .....	1

## 5 Pin Configuration and Functions

**PW Package  
20-Pin TSSOP  
Top View**



**DW Package  
20-Pin SOIC  
Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CLR}}$	9	I	<b>Shift register clear, active-low:</b> $\overline{\text{CLR}}$ is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear $\overline{\text{CLR}}$ is high. Driving $\overline{\text{CLR}}$ is low clears all the registers in the device.
DRAIN0	3	O	<b>Open-drain output:</b> DRAIN0 to DRAIN11 are the LED current-sink channels. These pins connect to the LED cathodes, and they can survive up to 40-V LED supply voltage. This is quite helpful during automotive load-dump conditions.
DRAIN1	4	O	
DRAIN2	5	O	
DRAIN3	6	O	
DRAIN4	7	O	
DRAIN5	8	O	
DRAIN6	13	O	
DRAIN7	14	O	
DRAIN8	15	O	
DRAIN9	16	O	
DRAIN10	17	O	
DRAIN11	18	O	
$\overline{\text{G}}$	10	I	<b>Output enable, active-low:</b> $\overline{\text{G}}$ is the LED channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.
GND	20	—	<b>Power ground:</b> GND is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
RCK	12	I	<b>Register clock:</b> RCK is the storage register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable $\overline{\text{G}}$ input signal is high.
SER IN	2	I	<b>Serial-data input:</b> SER IN is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

### Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SER OUT	11	O	<b>Serial-data output:</b> SER OUT is the serial data output of the 12-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.
SRCK	19	I	<b>Shift-register clock:</b> SRCK is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V <sub>CC</sub>	1	I	<b>Power supply:</b> V <sub>CC</sub> is the power supply pin voltage for the device. TI recommends adding a 0.1 $\mu$ F ceramic capacitor close to the pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
V <sub>CC</sub> Logic supply voltage		8	V
V <sub>I</sub> Logic input-voltage	–0.3	8	V
V <sub>DS</sub> Power DMOS drain-to-source voltage		42	V
Continuous total dissipation	See <a href="#">Thermal Information</a>		
Operating ambient temperature (Top)		125	°C
T <sub>J</sub> Operating junction temperature	–40	150	°C
T <sub>stg</sub> Storage temperature	–55	165	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

	VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
	Charged device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V <sub>CC</sub> Supply voltage	3	5.5	V
V <sub>IH</sub> High-level input voltage	2.4		V
V <sub>IL</sub> Low-level input voltage		0.7	V
t <sub>su</sub> Setup time, SER IN high before SRCK↑	15		ns
t <sub>h</sub> Hold time, SER IN high after SRCK↑	15		ns
t <sub>w</sub> Pulse duration	40		ns
T <sub>C</sub> Operating case temperature	–40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLC6C5912-Q1		UNIT
		20 PINS		
		PW (TSSOP)	DW (SOIC)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	114.8	81.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	44.1	45.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	61.3	49.1	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.7	17.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	60.8	48.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

V<sub>CC</sub> = 5 V, T<sub>C</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRAIN0 to DRAIN11, drain-to-source voltage					40	V
V <sub>OH</sub>	High-level output voltage, SER OUT	I <sub>OH</sub> = -20 μA	4.9	4.99		V
		I <sub>OH</sub> = -4 mA	4.5	4.69		
V <sub>OL</sub>	Low-level output voltage, SER OUT	I <sub>OH</sub> = 20 μA		0.001	0.01	V
		I <sub>OH</sub> = 4 mA		0.25	0.4	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = 5 V, V <sub>I</sub> = V <sub>CC</sub>		0.2		μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = 5 V, V <sub>I</sub> = 0		-0.2		μA
I <sub>CC</sub>	Logic supply current	V <sub>CC</sub> = 5 V, No clock signal		0.1	1	μA
		All outputs off All outputs on		130	170	
I <sub>CC(FRQ)</sub>	Logic supply current at frequency	f <sub>SRCK</sub> = 5 MHz, C <sub>L</sub> = 30 pF, all outputs on		300		μA
I <sub>DSX</sub>	Off-state drain current	V <sub>DS</sub> = 30 V, V <sub>CC</sub> = 5 V			0.1	μA
		V <sub>DS</sub> = 30 V, T <sub>C</sub> = 125°C, V <sub>CC</sub> = 5 V		0.15	0.3	
r <sub>DS(on)</sub>	Static drain-source on-state resistance	I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C, single channel ON	6	7.4	8.6	Ω
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C, all channels ON	6.7	8.9	9.6	
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C, single channel ON	7.9	9.3	11.2	
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C, all channels ON	8.7	10.6	12.3	
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 5 V, T <sub>A</sub> = 125°C, single channel ON	9.1	11.2	12.9	
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 5 V, T <sub>A</sub> = 125°C, all channels ON	10.3	13	14.5	
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 125°C, single channel ON	11.6	13.7	16.4	
		I <sub>D</sub> = 20 mA, V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 125°C, all channels ON	12.8	15.6	18.2	
T <sub>SHUTDOWN</sub>	Thermal shutdown trip point		150	175	200	°C
T <sub>HYS</sub>	Hysteresis			15		°C

## 6.6 Switching Characteristics

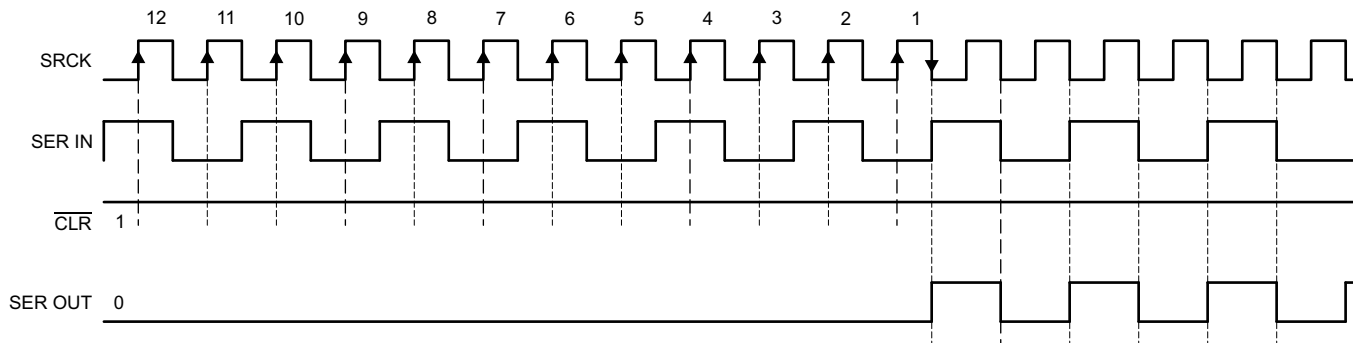
V<sub>CC</sub> = 5 V, T<sub>J</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output from $\overline{G}$		210		ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output from $\overline{G}$		75		ns
t <sub>r</sub>	Rise time, drain output		250		ns
t <sub>f</sub>	Fall time, drain output		200		ns
t <sub>pd</sub>	Propagation delay time, SRCK↓ to SEROUT	C <sub>L</sub> = 30 pF, I <sub>D</sub> = 48 mA	35		ns
T <sub>or</sub>	SEROUT rise time (10% to 90%)	C <sub>L</sub> = 30 pF	20		ns
T <sub>of</sub>	SEROUT fall time (90% to 10%)	C <sub>L</sub> = 30 pF	20		ns

## Switching Characteristics (continued)

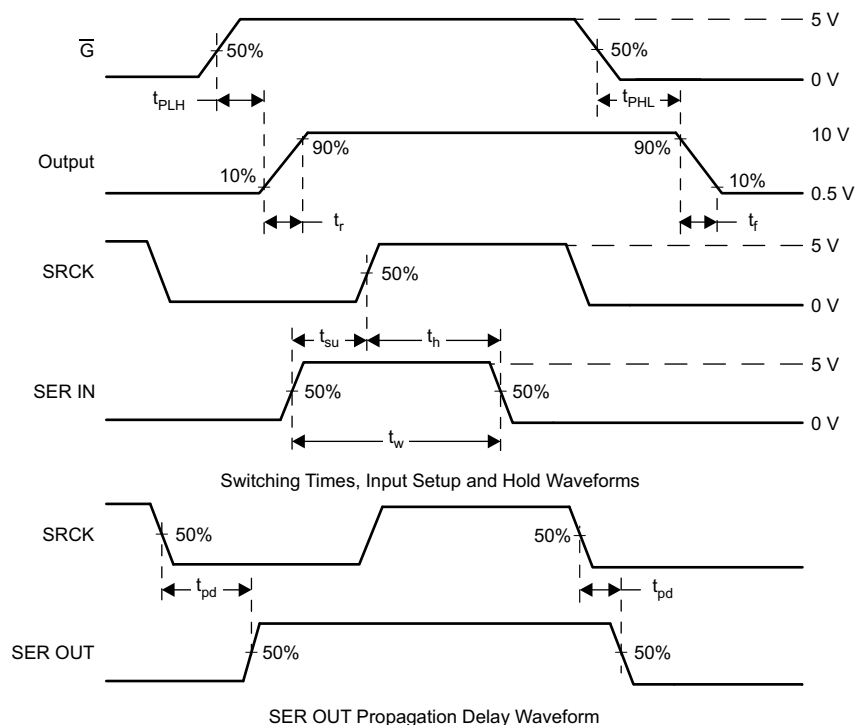
 $V_{CC} = 5\text{ V}$ ,  $T_J = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SRCK)}$	Serial clock frequency	$C_L = 30\text{ pF}$ , $I_D = 20\text{ mA}$			10	MHz
$T_{SRCK\_WH}$	SRCK pulse duration, high		30			ns
$T_{SRCK\_WL}$	SRCK pulse duration, low		30			ns



**Figure 1. SER IN to SER OUT Waveform**

Figure 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

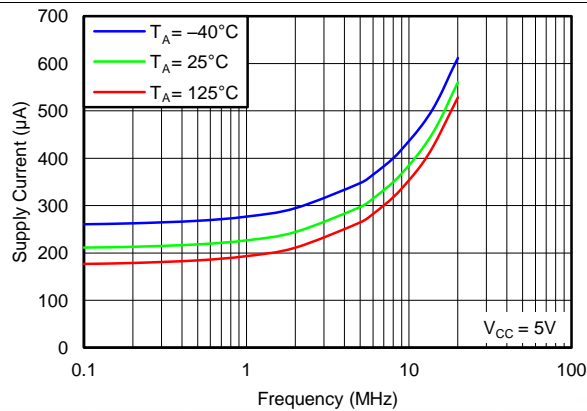


**Figure 2. Switching Times and Voltage Waveforms**

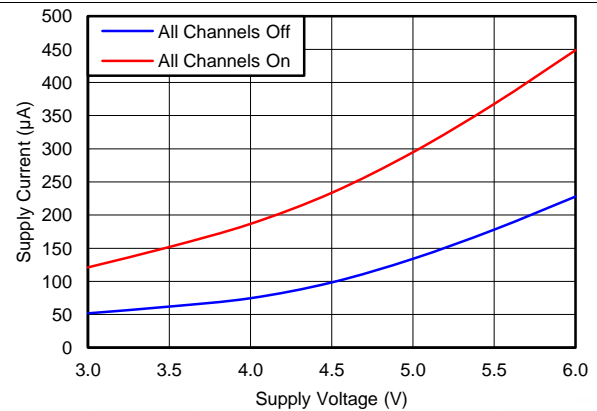
Figure 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 12.

## 6.7 Typical Characteristics

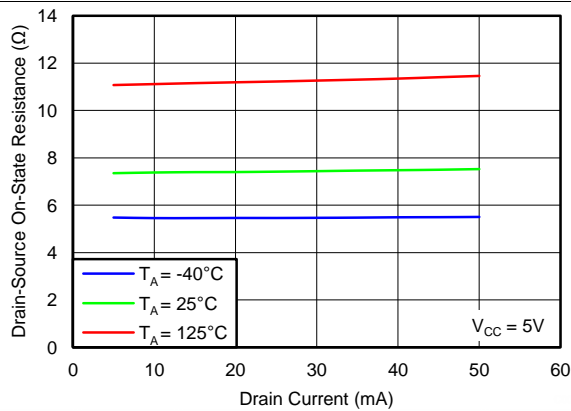
Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.



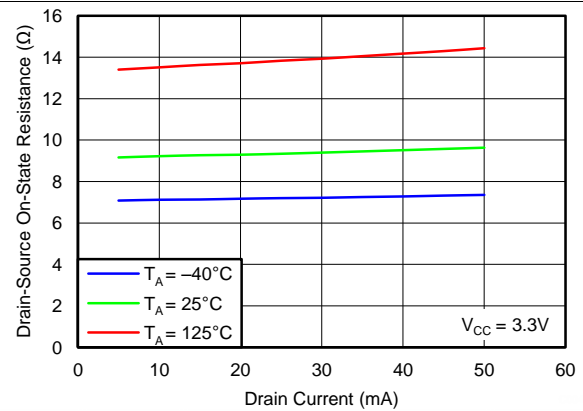
**Figure 3. Supply Current vs Frequency**



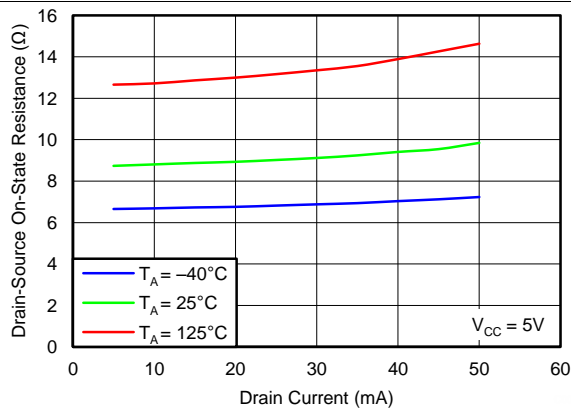
**Figure 4. Supply Current vs Supply Voltage**



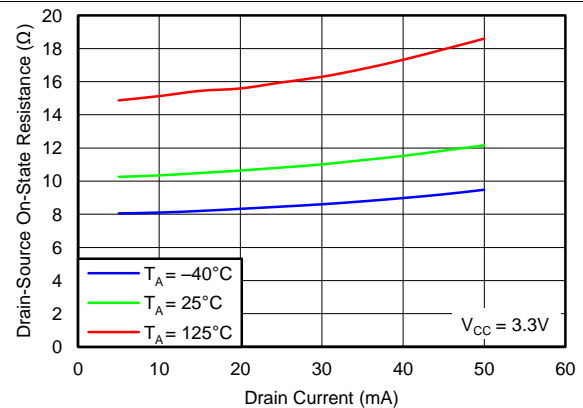
**Figure 5. Drain-to-Source On-State Resistance vs Drain Current**



**Figure 6. Drain-to-Source On-State Resistance vs Drain Current**



**Figure 7. Drain-to-Source On-State Resistance vs Drain Current**



**Figure 8. Drain-to-Source On-State Resistance vs Drain Current**

## Typical Characteristics (continued)

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.

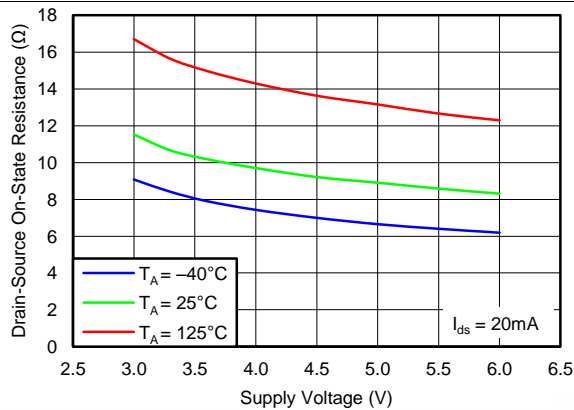


Figure 9. Drain-to-Source On-State Resistance vs Drain Current

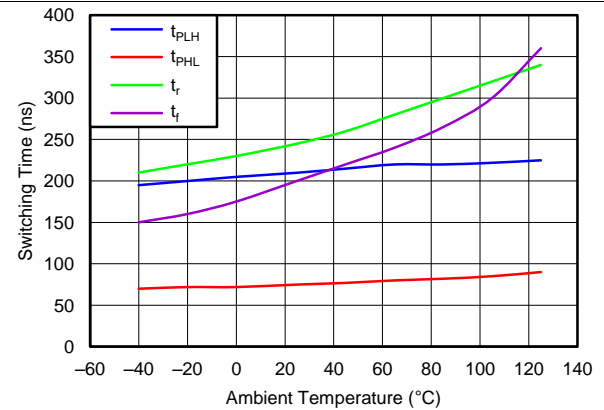
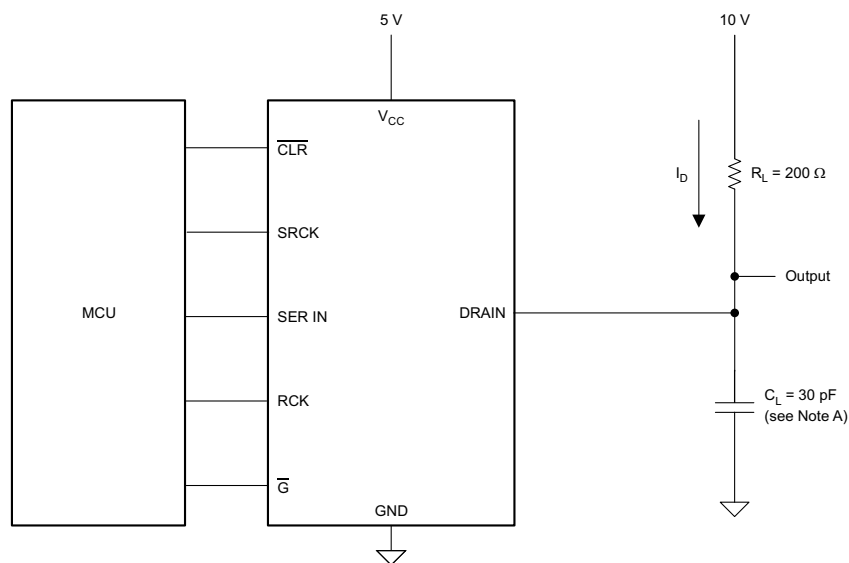


Figure 10. Switching Time vs Ambient Temperature



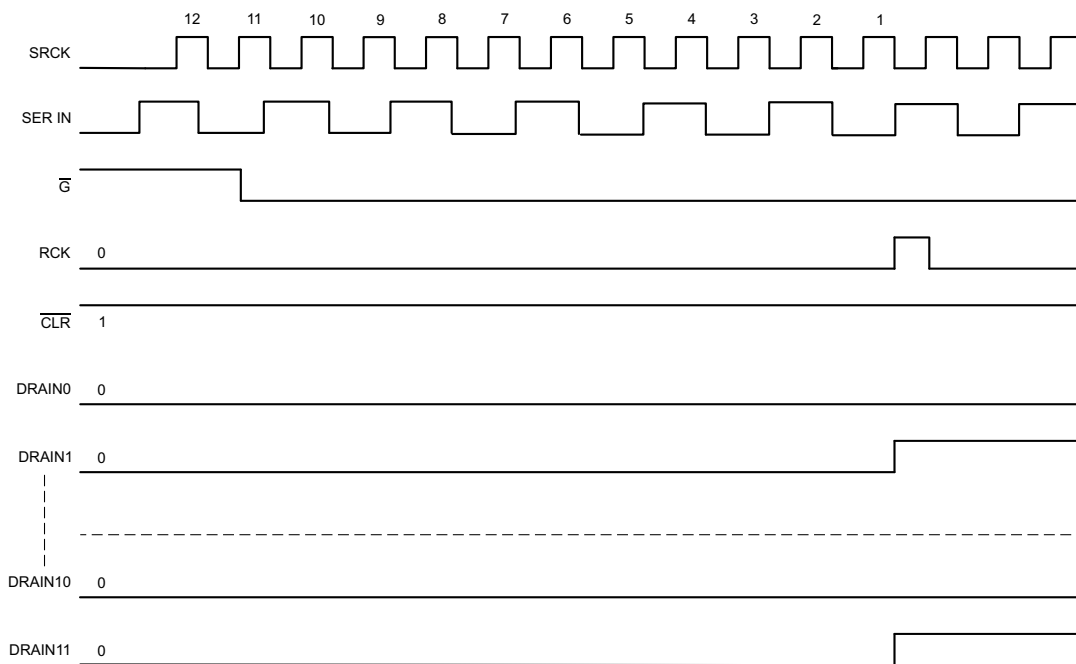
## 7 Parameter Measurement Information



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A. C<sub>L</sub> includes probe and jig capacitance.

**Figure 11. Resistive-Load Test Circuit**



**Figure 12. Voltage Waveforms**

Figure 11 and Figure 12 show the resistive-load test circuit and voltage waveforms. One can see from Figure 12 that with  $\overline{G}$  held low and CLR held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.



## Feature Description (continued)

### 8.3.2 Serial-In Interface

The TLC6C598 device contains an 8-bit serial-in, parallel out shift register that feeds an 8-bit D-type storage register. Data transfer through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage transfers data to the output buffer when shift register clear (CLR) is high.

### 8.3.3 Clear Register

A logic low on  $\overline{\text{CLR}}$  clears all registers in the device. TI suggests clearing the device during power up or initialization.

### 8.3.4 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid that the second device receives SRCK and data input at the same rising edge of SRCK.

### 8.3.5 Output Control

Holding the output enable (G) high holds all data in the output buffers low, and all drain outputs are off. Holding G low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sink-current. This pin also be used for global PWM dimming.

## 8.4 Device Functional Modes

### 8.4.1 Operation With $V_{CC} < 3\text{ V}$

This device works normally during  $3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ , when operation voltage is lower than 3 V. The behavior of device cannot be ensured, including communication interface and current capability.

### 8.4.2 Operation With $5.5\text{ V} \leq V_{CC} \leq 8\text{ V}$

The device works normally during this voltage range, but reliability issues may occurs while the device works for a long time in this voltage range.

## 9 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 9.1 Application Information

The TLC6C5912-Q1 device is a serial-in, parallel-out, power logic 8-bit shift register with low-side open-drain DMOS output rating of 40 V and 50-mA continuous sink-current capabilities when  $V_{CC} = 5$  V. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model.

### 9.2 Typical Application

[Figure 13](#) shows a typical cascade application circuit with two TLC6C5912-Q1 chips configured to cascade topology. The MCU generates all the input signals.

## Typical Application (continued)

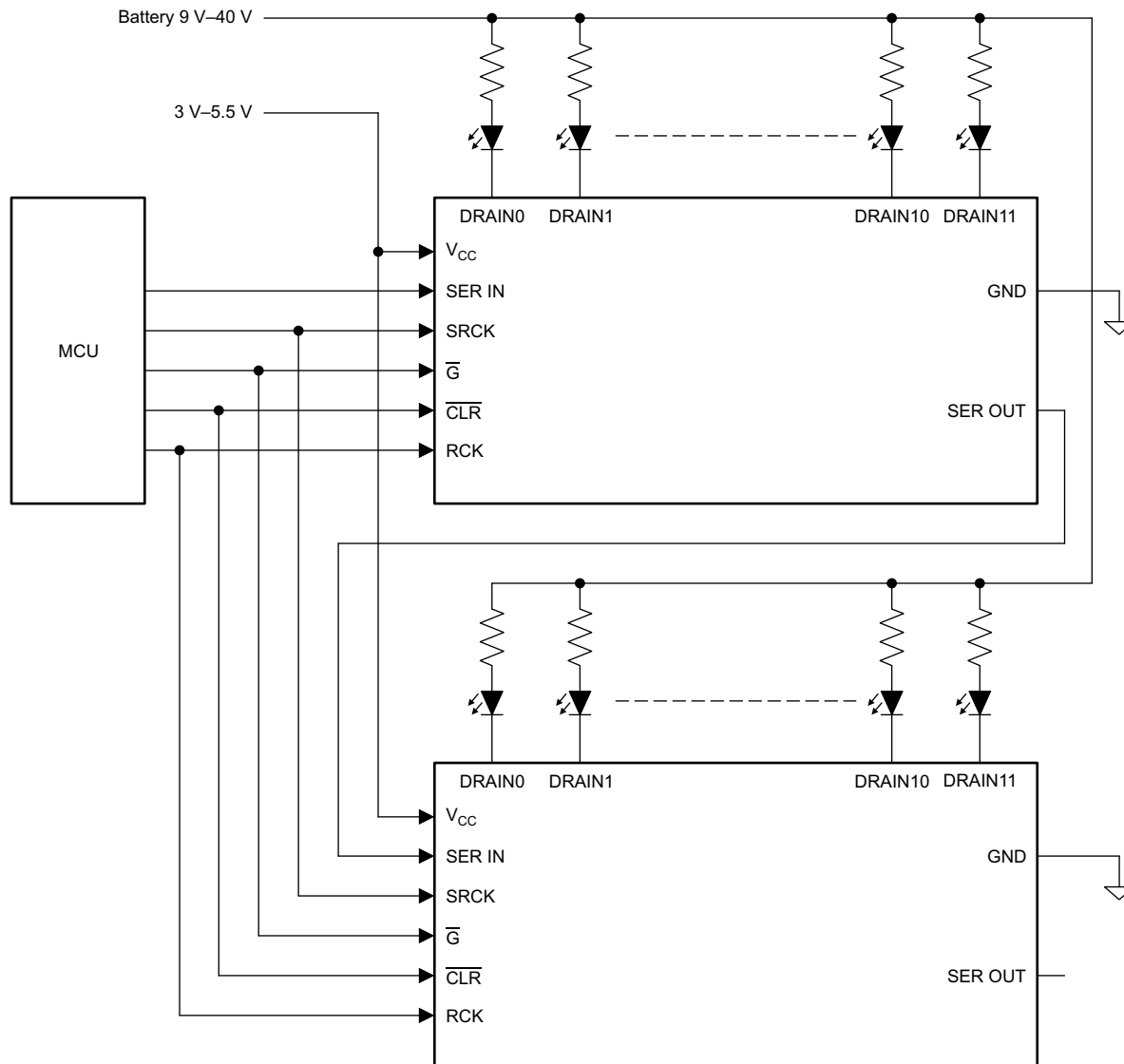


Figure 13. Typical Application Circuit

### 9.2.1 Design Requirements

Table 1 lists the parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Vbattery	9 to 40 V
V <sub>CC-1</sub>	3.3 V
I(D0), I(D1), I(D2), I(D3), I(D4), I(D5), I(D6), I(D7), I(D8), I(D9), I(D10), I(D11)	30 mA
V <sub>CC-2</sub>	5 V
I(D12), I(D13), I(D14), I(D15), I(D16), I(D17), I(D18), I(D19), I(D20), I(D21), I(D22), I(D23)	50 mA

### 9.2.2 Detailed Design Procedure

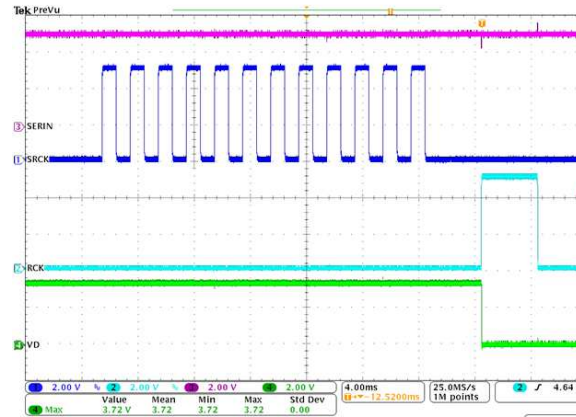
To begin the design process, the designer must decide on a few parameters:

- V<sub>supply</sub>: LED supply voltage
- V<sub>Dx</sub>: LED forward voltage
- I: LED current

After determining the parameters, calculate the resistor in series with LED using [Equation 1](#).

$$R_x = (V_{\text{supply}} - V_{Dx}) / I \quad (1)$$

### 9.2.3 Application Curve



**Figure 14. TLC6C5912-Q1 Application Waveform**

## 10 Power Supply Recommendations

The TLC6C5912-Q1 device is designed to operate from an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the  $V_{CC}$  pin.

## 11 Layout

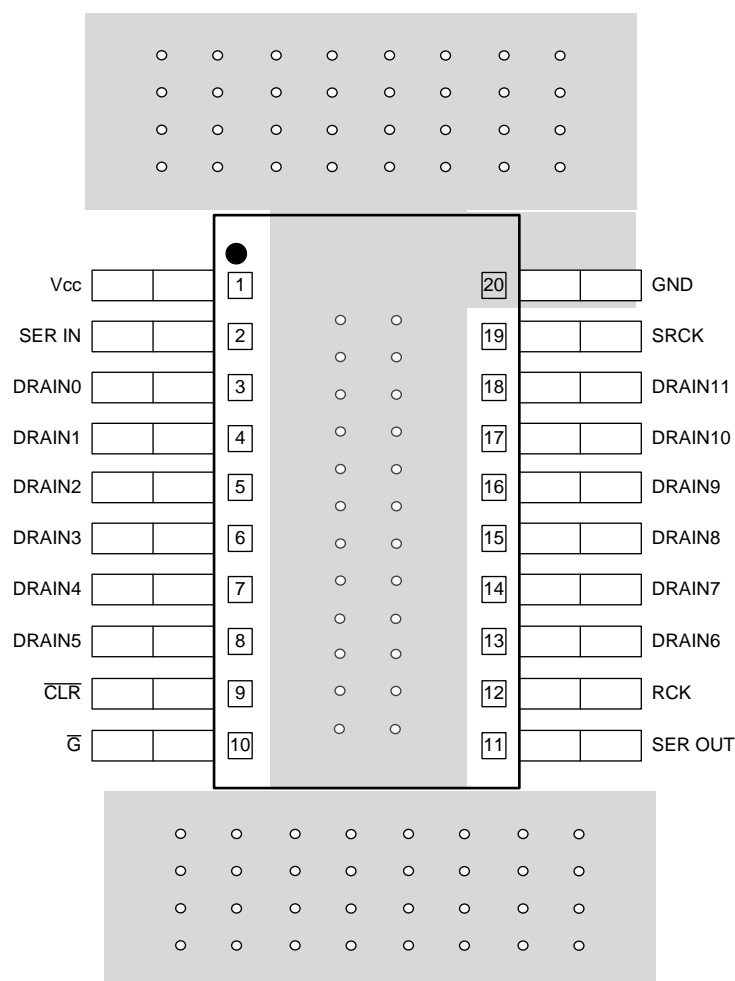
### 11.1 Layout Guidelines

There are no special layout requirement for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pin.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the cooper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

### 11.2 Layout Example



**Figure 15. Layout Recommendation**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C5912GQPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912G	<a href="#">Samples</a>
TLC6C5912QDWRQ1	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5912	<a href="#">Samples</a>
TLC6C5912QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLC6C5912-Q1 :**

- Catalog: [TLC6C5912](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5912GQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC6C5912QDWRQ1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC6C5912QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5912GQPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0
TLC6C5912QDWRQ1	SOIC	DW	20	2000	367.0	367.0	45.0
TLC6C5912QPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0

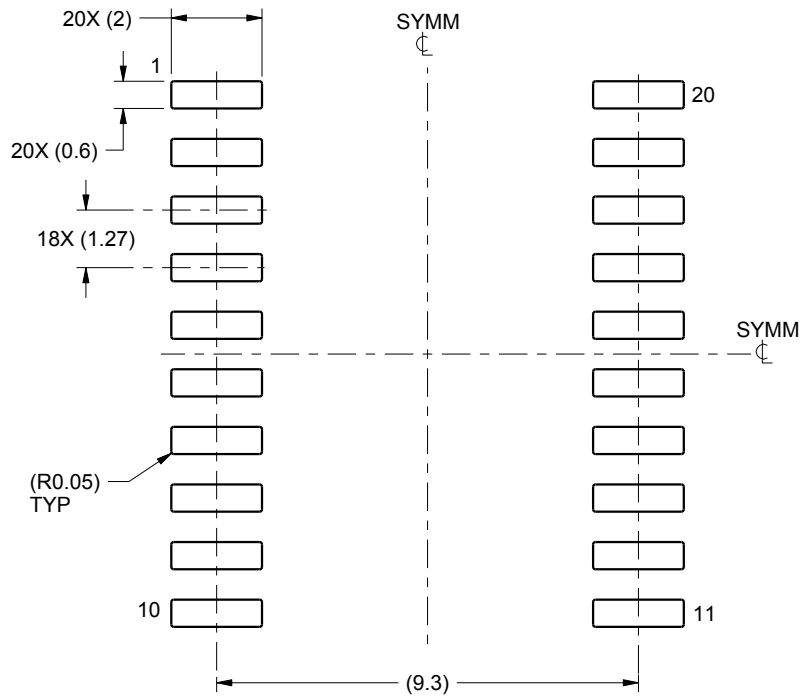


# EXAMPLE BOARD LAYOUT

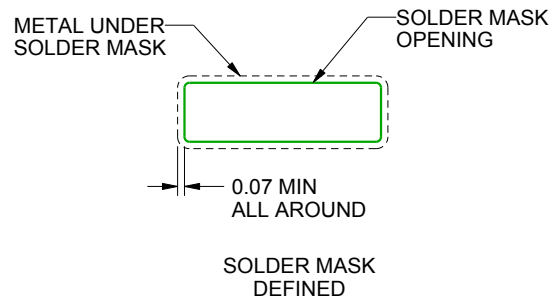
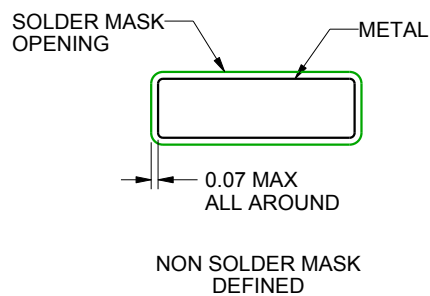
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

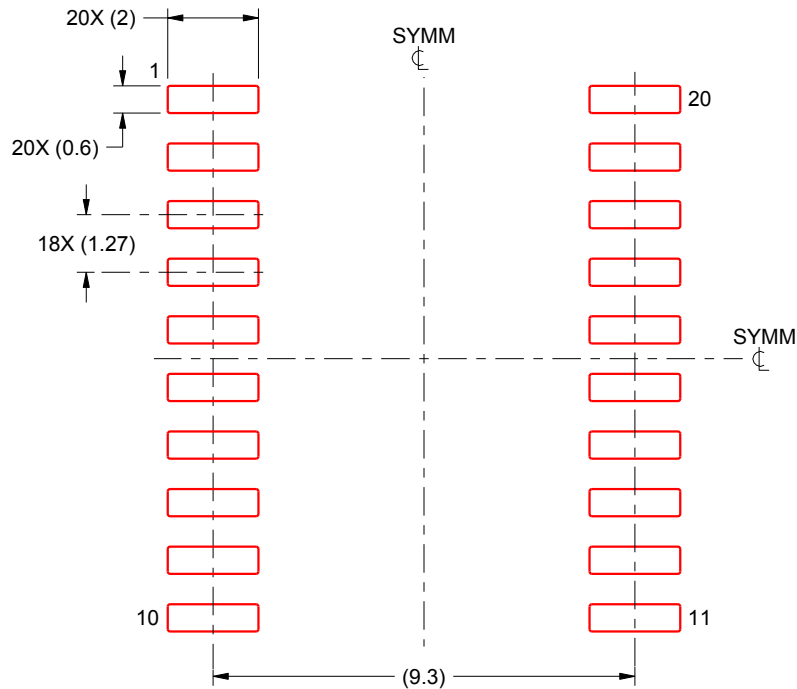
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



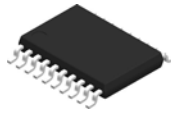
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

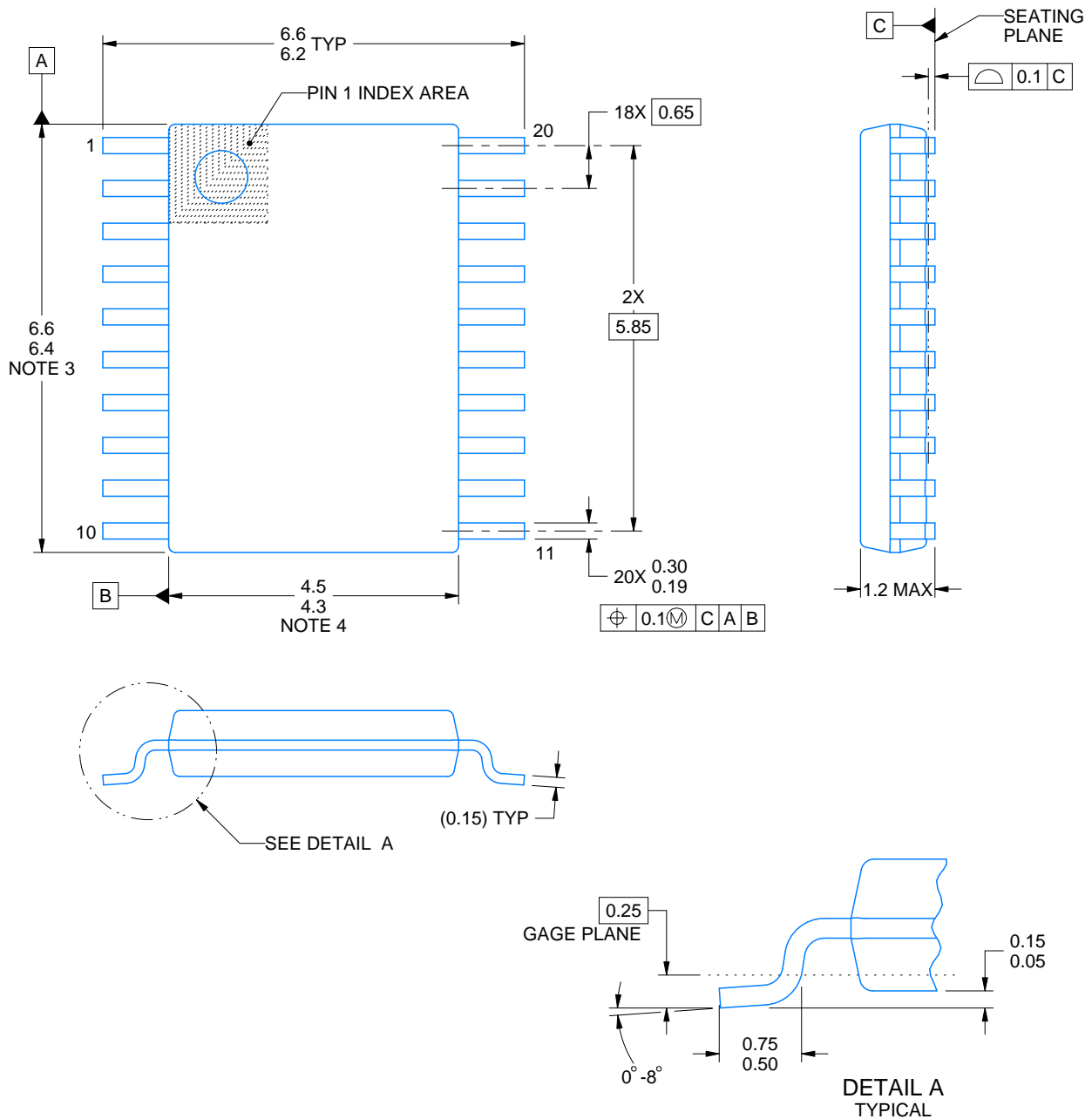
PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



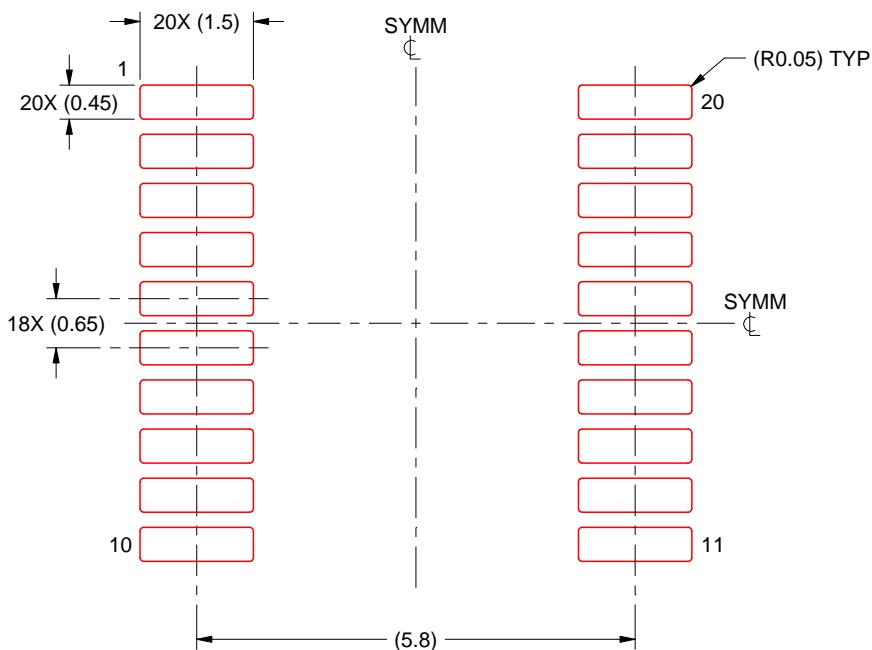


# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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