

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

SSM3K36MFV

○ High-Speed Switching Applications

1. Features

- 1.5-V drive
- Low ON-resistance: $R_{on} = 1.52 \Omega$ (max) (@ $V_{GS} = 1.5 V$)
 - : $R_{on} = 1.14 \Omega$ (max) (@ $V_{GS} = 1.8 V$)
 - : $R_{on} = 0.85 \Omega$ (max) (@ $V_{GS} = 2.5 V$)
 - : $R_{on} = 0.66 \Omega$ (max) (@ $V_{GS} = 4.5 V$)
 - : $R_{on} = 0.63 \Omega$ (max) (@ $V_{GS} = 5.0 V$)

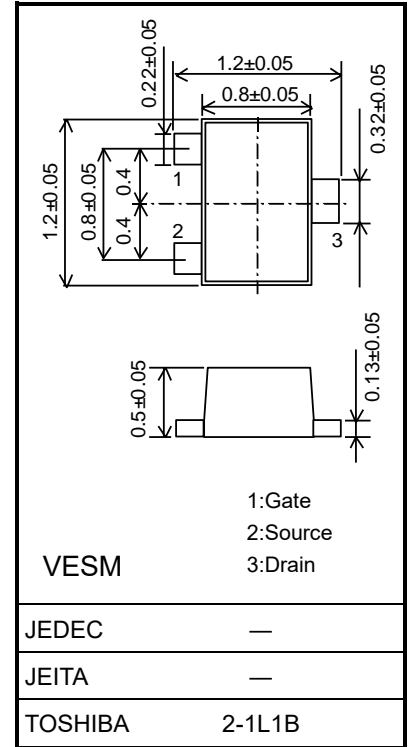
2. Absolute Maximum Ratings (Note) ($T_a = 25^\circ C$)

| Characteristics | Symbol | Rating | Unit |
|-------------------------|----------------|------------|------------|
| Drain-source voltage | V_{DSS} | 20 | V |
| Gate-source voltage | V_{GSS} | ± 10 | V |
| Drain current | DC | I_D | 500 |
| | Pulse | I_{DP} | 1000 |
| Drain power dissipation | P_D (Note 1) | 150 | mW |
| Channel temperature | T_{ch} | 150 | $^\circ C$ |
| Storage temperature | T_{stg} | -55 to 150 | $^\circ C$ |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

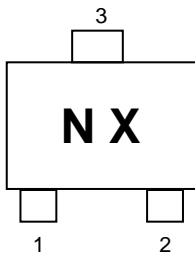
Note1: Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.585 mm²)

Unit: mm

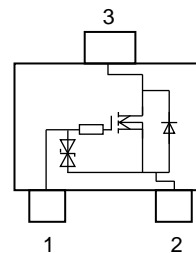


Weight: 1.5 mg (typ.)

3. Marking



4. Equivalent Circuit (Top view)



Start of commercial production
2008-02

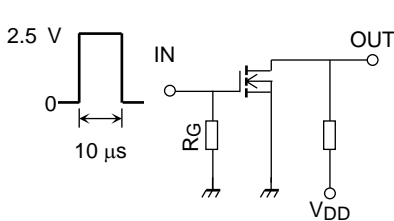
4. Electrical Characteristics (Ta = 25°C)

| Characteristics | Symbol | Test Conditions | Min | Typ. | Max | Unit | |
|--------------------------------|---------------|--|--|-------|---------|---------------|----|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$ | 20 | — | — | V | |
| | $V_{(BR)DSX}$ | $I_D = 1 \text{ mA}, V_{GS} = -10 \text{ V}$ | 12 | — | — | | |
| Drain cutoff current | I_{DSS} | $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ | — | — | 1 | μA | |
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$ | — | — | ± 1 | μA | |
| Gate threshold voltage | V_{th} | $V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$ | 0.35 | — | 1.0 | V | |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = 3 \text{ V}, I_D = 200 \text{ mA}$ (Note2) | 420 | 840 | — | mS | |
| Drain-source ON-resistance | $R_{DS(ON)}$ | $I_D = 200 \text{ mA}, V_{GS} = 5.0 \text{ V}$ (Note2) | — | 0.46 | 0.63 | Ω | |
| | | $I_D = 200 \text{ mA}, V_{GS} = 4.5 \text{ V}$ (Note2) | — | 0.51 | 0.66 | | |
| | | $I_D = 200 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note2) | — | 0.66 | 0.85 | | |
| | | $I_D = 100 \text{ mA}, V_{GS} = 1.8 \text{ V}$ (Note2) | — | 0.81 | 1.14 | | |
| | | $I_D = 50 \text{ mA}, V_{GS} = 1.5 \text{ V}$ (Note2) | — | 0.95 | 1.52 | | |
| Input capacitance | C_{iss} | $V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | — | 46 | — | pF | |
| Output capacitance | C_{oss} | | — | 10.8 | — | | |
| Reverse transfer capacitance | C_{rss} | | — | 7.3 | — | | |
| Total Gate Charge | Q_g | $V_{DS} = 10 \text{ V}, I_D = 0.5 \text{ A}, V_{GS} = 4.0 \text{ V}$ | — | 1.23 | — | nC | |
| Gate–Source Charge | Q_{gs} | | — | 0.60 | — | | |
| Gate–Drain Charge | Q_{gd} | | — | 0.63 | — | | |
| Switching time | Turn-on time | t_{on} | $V_{DD} = 10 \text{ V}, I_D = 200 \text{ mA}$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}, R_G = 50 \Omega$ | — | 30 | — | ns |
| | Turn-off time | t_{off} | | — | 75 | — | |
| Drain-source forward voltage | V_{DSF} | $I_D = -0.5 \text{ A}, V_{GS} = 0 \text{ V}$ (Note2) | — | -0.88 | -1.2 | V | |

Note2: Pulse test

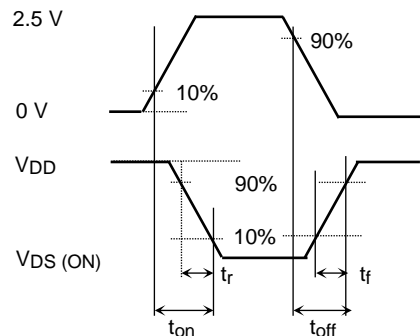
5. Switching Time Test Circuit

(a) Test Circuit



$V_{DD} = 10 \text{ V}$
 $R_G = 50 \Omega$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) VIN



(c) VOUT

Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the SSM3K36MFV). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

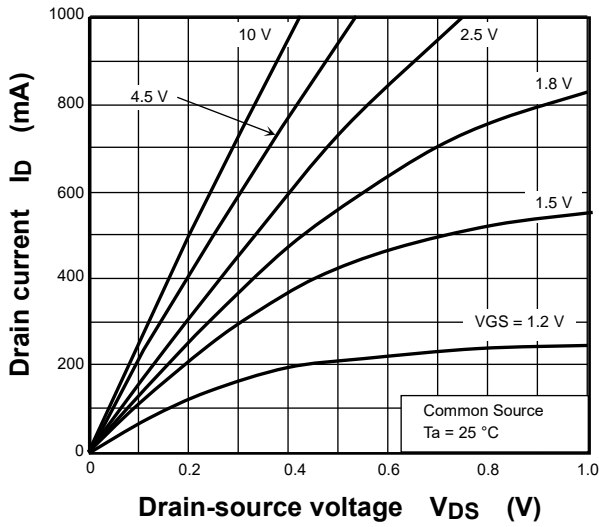
Take this into consideration when using the device.

Handling Precaution

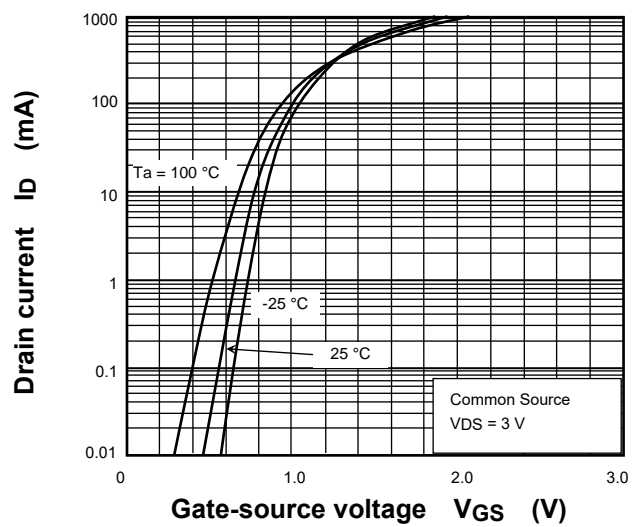
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

6. Characteristics Curves (Note)

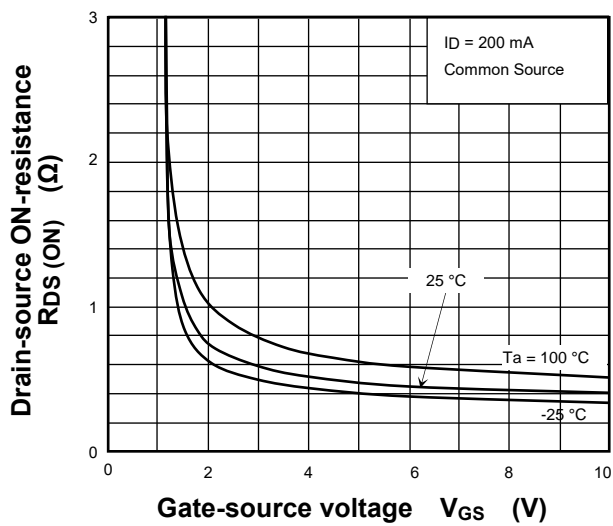
$I_D - V_{DS}$



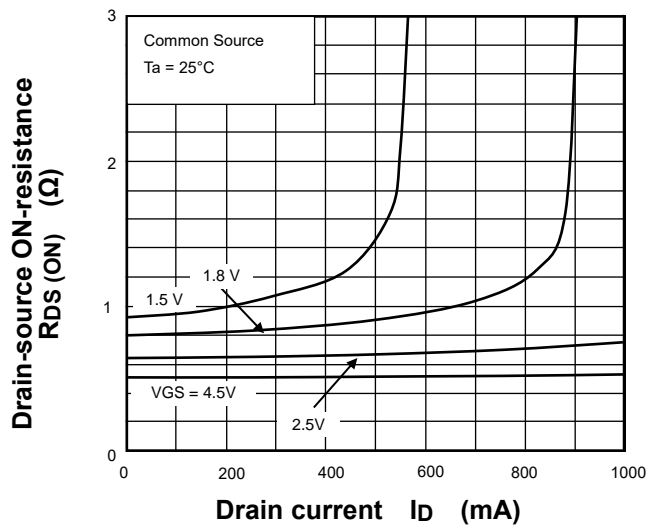
$I_D - V_{GS}$



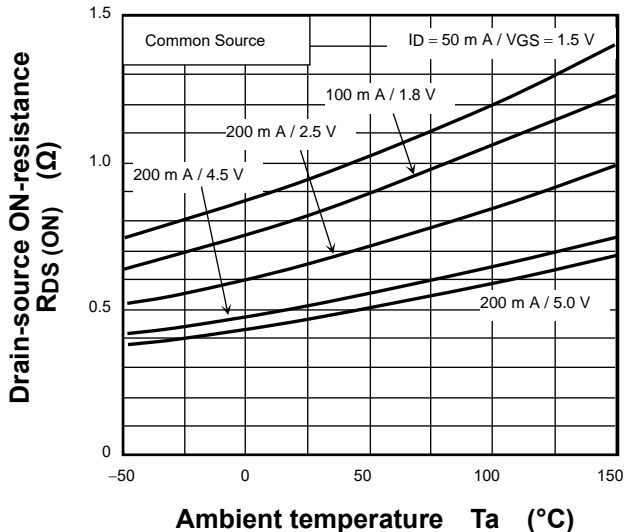
$R_{DS(ON)} - V_{GS}$



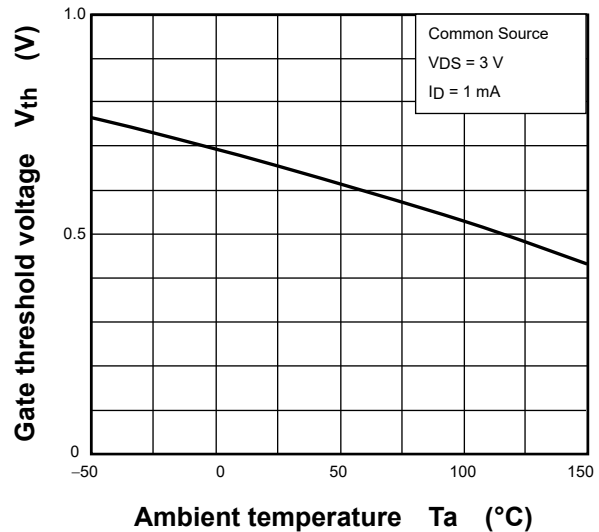
$R_{DS(ON)} - I_D$

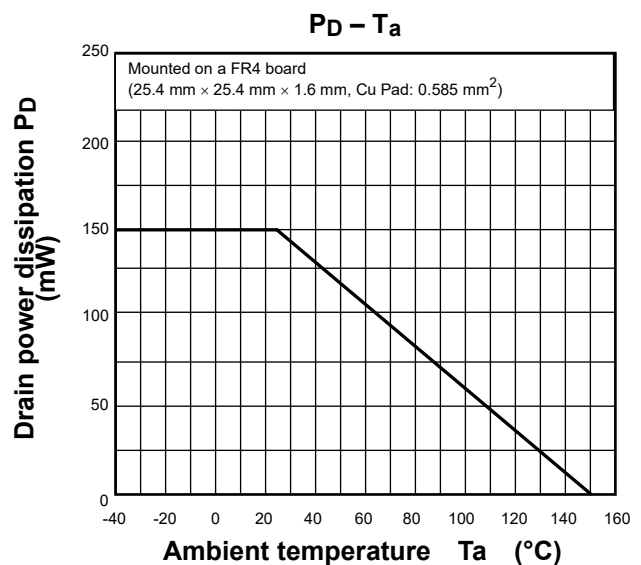
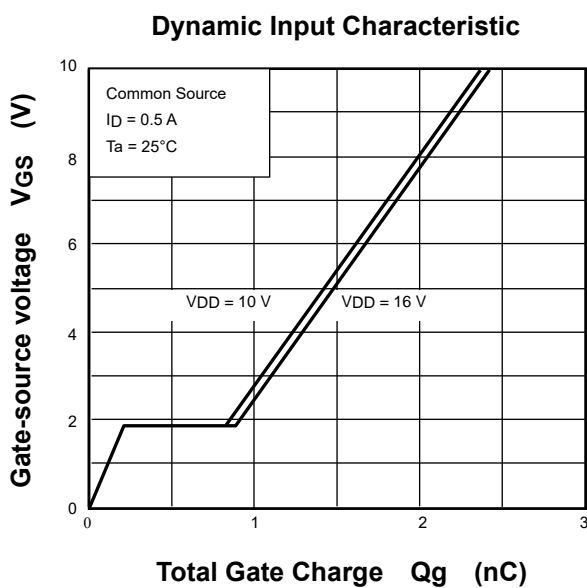
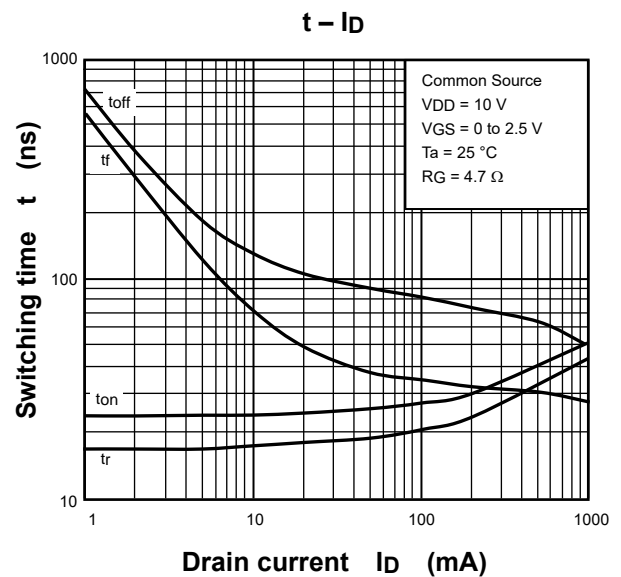
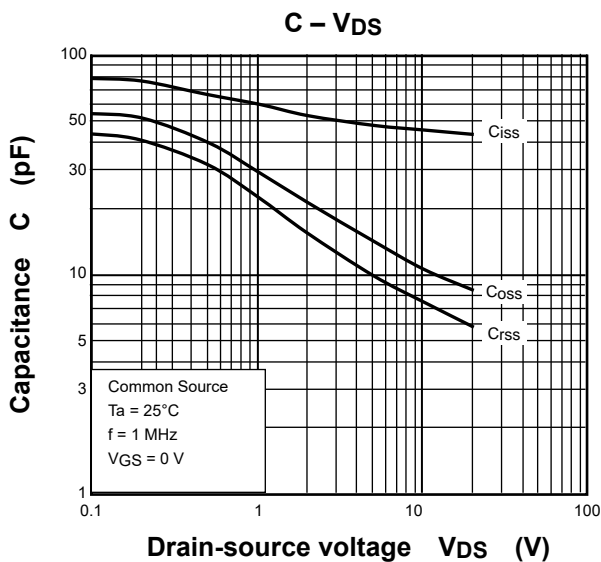
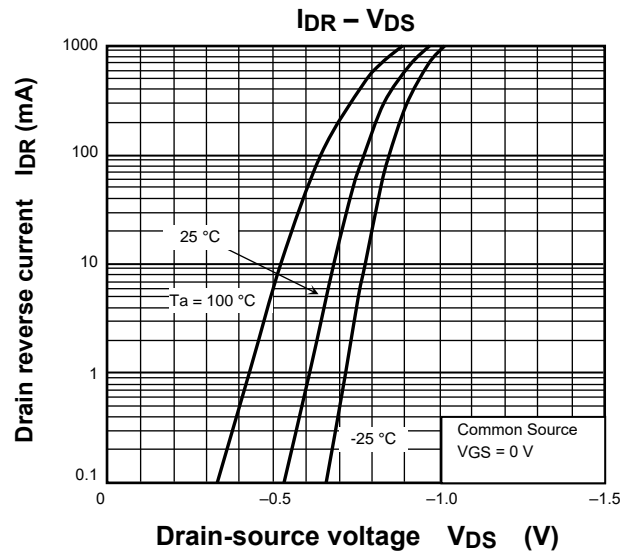
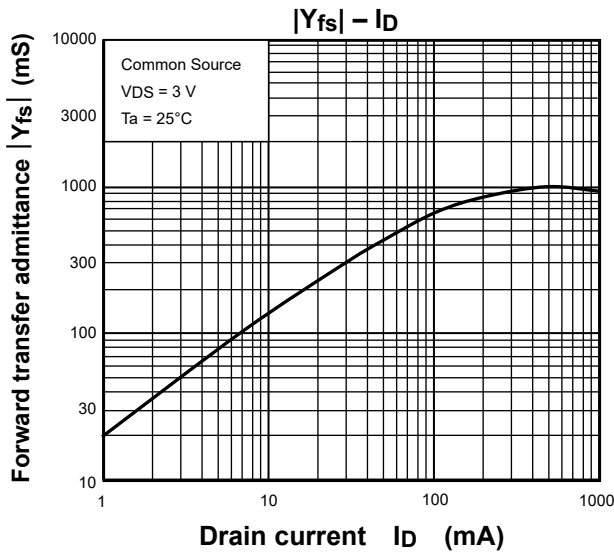


$R_{DS(ON)} - T_a$



$V_{th} - T_a$





Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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