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MOSFET - Power, Single N-Channel

80 V, 9 mΩ, 58 A

NTTYS009N08HL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	80	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	I_D	$T_C = 25^\circ\text{C}$	58
		$T_C = 100^\circ\text{C}$	41
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)	P_D	$T_C = 25^\circ\text{C}$	73
		$T_C = 100^\circ\text{C}$	36
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	I_D	$T_A = 25^\circ\text{C}$	12
		$T_A = 100^\circ\text{C}$	8
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	P_D	$T_A = 25^\circ\text{C}$	3.2
		$T_A = 100^\circ\text{C}$	1.6
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	590
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	60	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 26.4 \text{ A}, L = 0.1 \text{ mH}$)	E_{AS}	35	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 3)	$R_{\theta JC}$	2.0	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	46	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JE51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

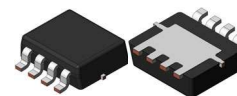
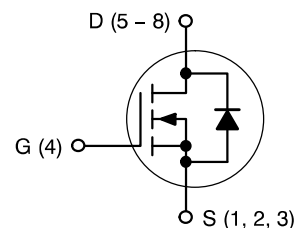


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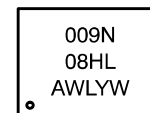
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	9 mΩ @ 10 V	58 A
	10.9 mΩ @ 4.5 V	

N-Channel



LPAK8
3.3x3.3
CASE 760AD

MARKING DIAGRAM



009N08HL = Specific Device Code

A = Assembly Location

WL = Wafer Lot

Y = Year

W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			53.4		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 5)

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		7.1	8.6	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		8.9	11	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 70\text{ }\mu\text{A}$	1.2	1.6	2.0	V
Gate Threshold Voltage Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.2		mV/ $^\circ\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		64.1		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ $V_{DS} = 40\text{ V}$		1402		pF
Reverse Transfer Capacitance	C_{rss}			187		pF
Output Capacitance	C_{oss}			10.5		pF
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 10\text{ A}$		2		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 10\text{ A}$		24		
Gate-to-Source Charge	Q_{GS}			3.5		
Gate-to-Drain Charge	Q_{GD}			4.3		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 6\text{ V}, V_{DS} = 64\text{ V},$ $I_D = 10\text{ A}, R_G = 6\text{ m}\Omega$		11		ns
Turn-Off Delay Time	$t_{d(off)}$			29		
Rise Time	t_r			10		
Fall Time	t_f			9		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^{\circ}\text{C}$		0.8	1.2	V
			$T_J = 125^{\circ}\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dl/dt = 100\text{ A}/\mu\text{s},$ $I_S = 10\text{ A}$			39		ns
Charge Time	t_a				20		
Discharge Time	t_b				20		
Reverse Recovery Charge	Q_{RR}				27		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

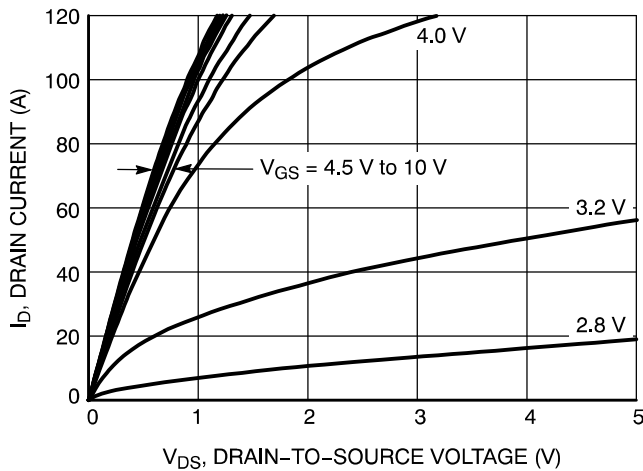


Figure 1. On-Region Characteristics

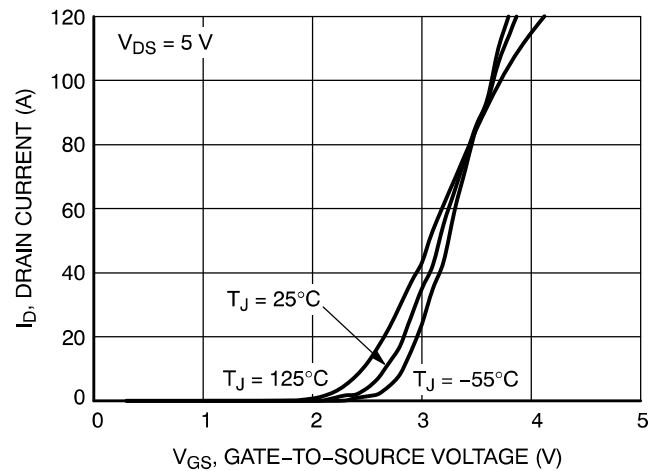


Figure 2. Transfer Characteristics

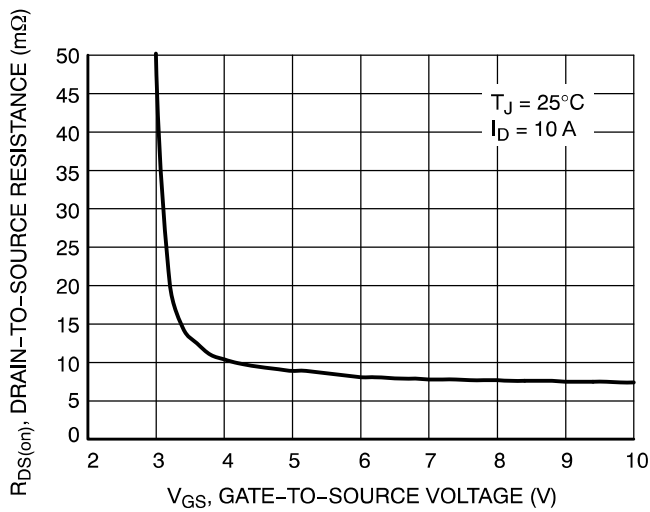


Figure 3. On-Resistance vs. Gate-to-Source Voltage

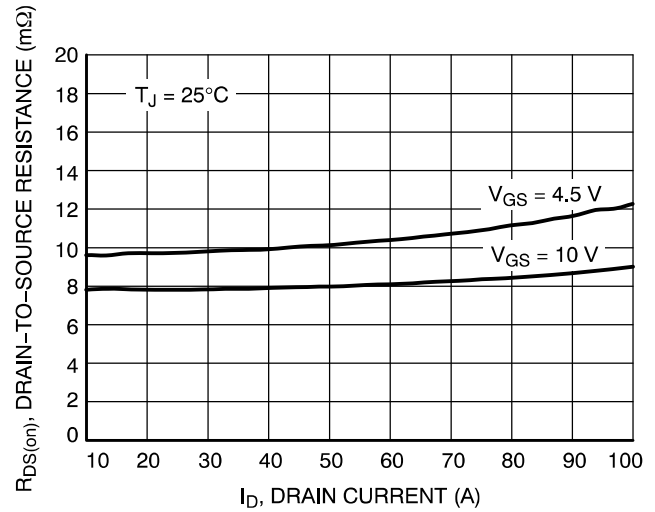


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

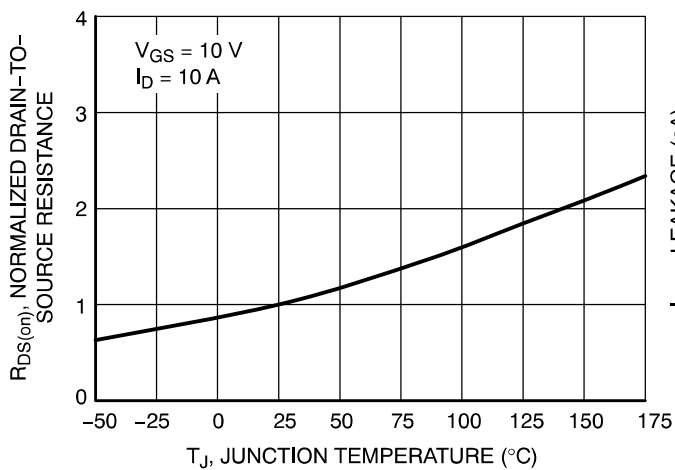


Figure 5. On-Resistance Variation with Temperature

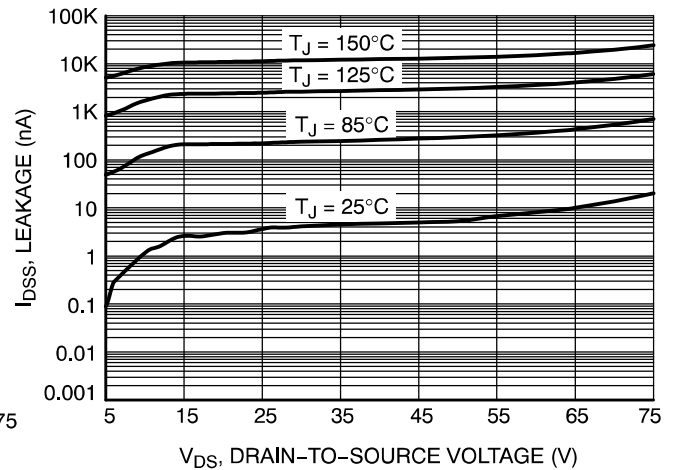


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

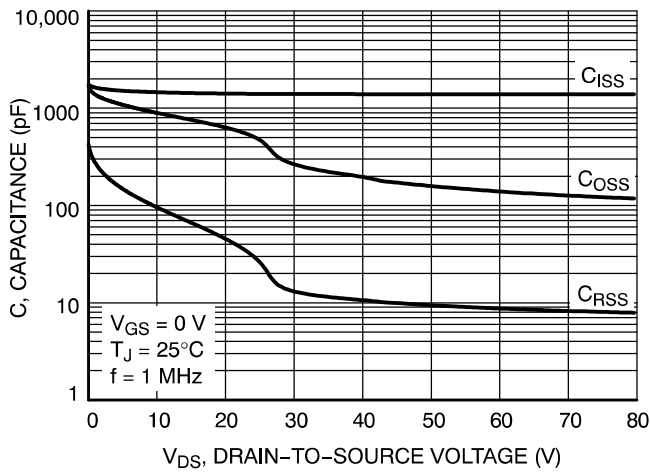


Figure 7. Capacitance Variation

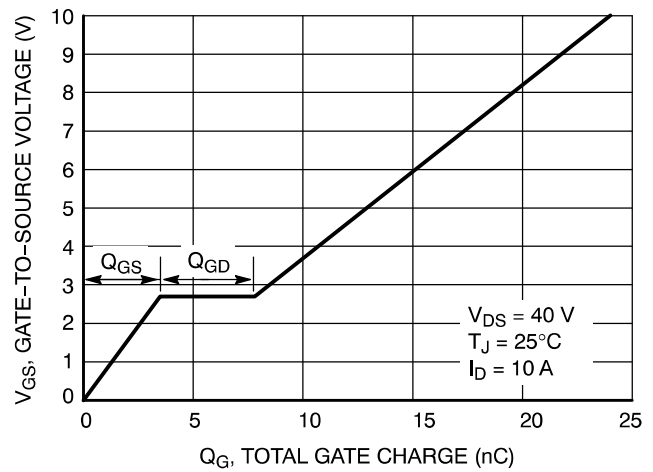


Figure 8. Gate-to-Source vs. Total Charge

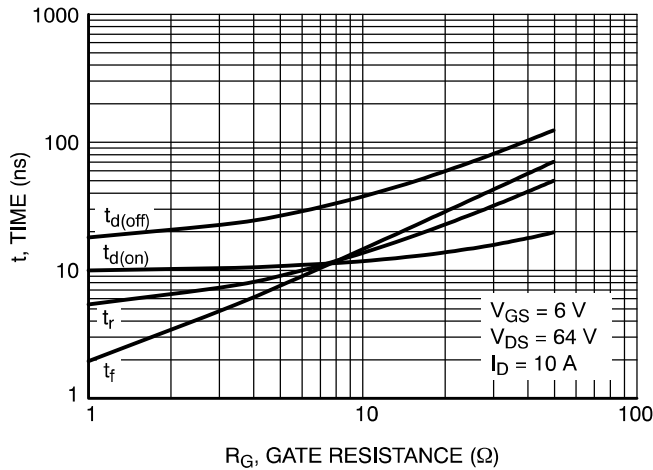


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

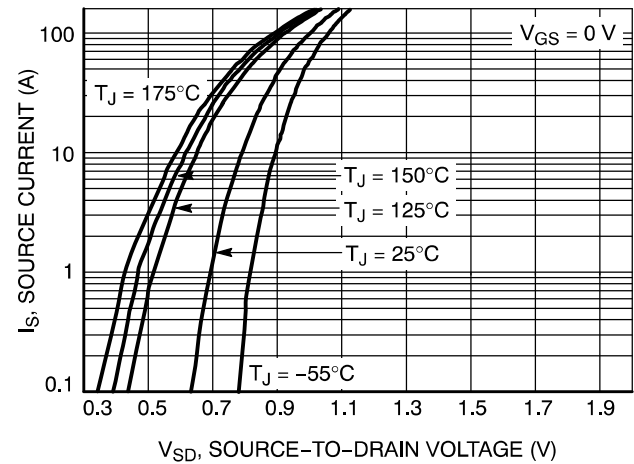


Figure 10. Diode Forward Voltage vs. Current

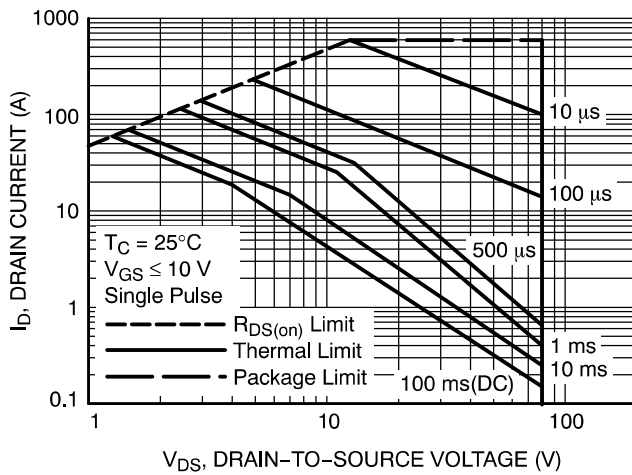


Figure 11. Maximum Rated Forward Biased Safe Operating Area

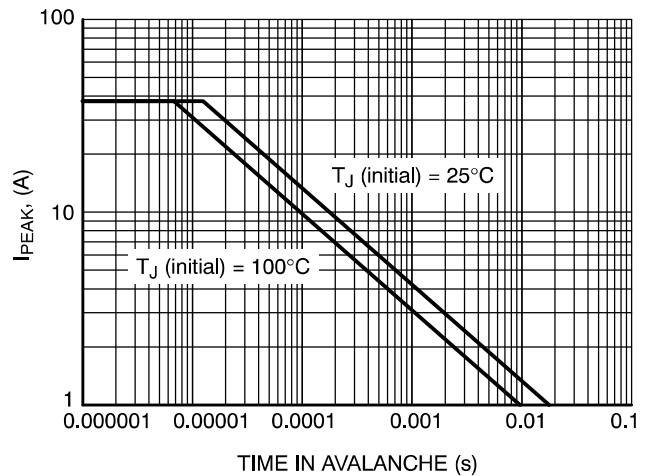


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTTYS009N08HL

TYPICAL CHARACTERISTICS

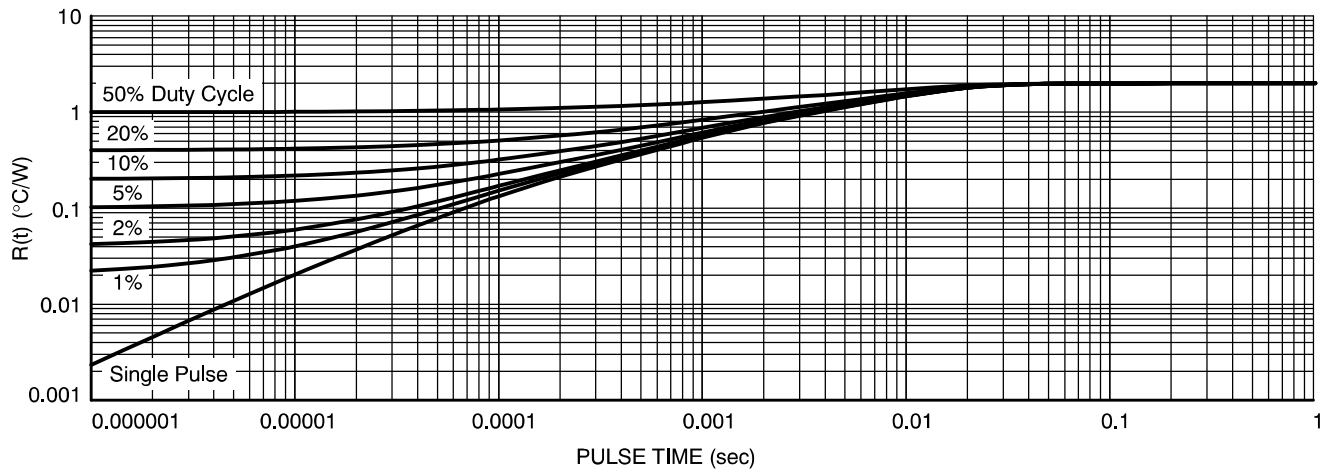


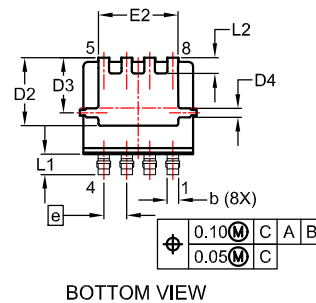
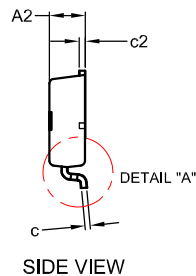
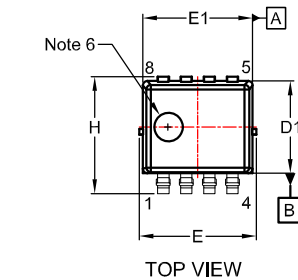
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

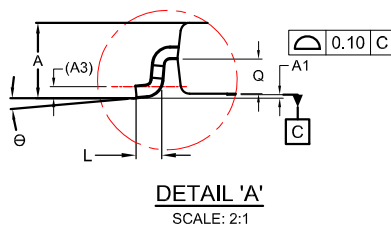
Device	Marking	Package	Shipping [†]
NTTYS009N08HLTWG	009N 08HL	LFPAK8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

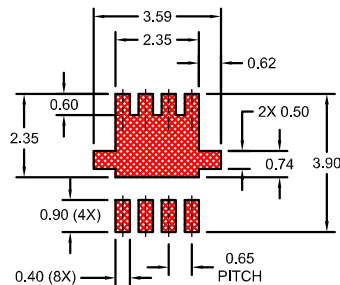
LFPAK8 3.3x3.3, 0.65P
CASE 760AD
ISSUE E

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
Θ	0°	4°	8°



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/RM.

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