

NSB4904DW1T1G, NSB4904DW1T2G

Dual Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB4904DW1T1G and NSB4904DW1T2G, two complementary BRT devices are housed in the SC-88/SOT-363 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , - minus sign for Q_1 (PNP) omitted)

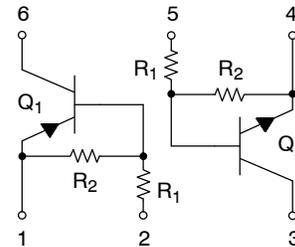
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB0}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



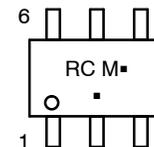
ON Semiconductor®

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**SC-88/SOT-363
CASE 419B
STYLE 1**

MARKING DIAGRAM



RC = Device Marking
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See specific ordering information in the ordering information table on page 3 of this data sheet.

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THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1) 490 (Note 2)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1) 325 (Note 2)	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	188 (Note 1) 208 (Note 2)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 inch Pad.

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ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , - minus sign for Q_1 (PNP) omitted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	-	-	100	nA
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	-	-	500	nA
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	-	-	0.1	mA
Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	-	-	V
Collector-Emitter Breakdown Voltage (Note 4) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	-	-	V

ON CHARACTERISTICS (Note 4)

DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	h_{FE}	80	140	-	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$)	$V_{CE(sat)}$	-	-	0.25	V
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 3.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	-	-	0.2	V
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	-	-	V
Input Resistor	R1	32.9	47	61.1	k Ω
Resistor Ratio	R1/R2	0.8	1.0	1.2	

3. New resistor combinations. Updated curves to follow in subsequent data sheets.

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

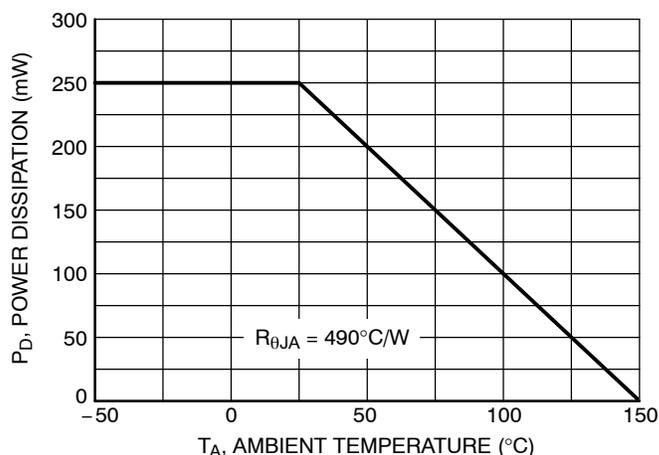


Figure 1. Derating Curve

ORDERING INFORMATION AND RESISTOR VALUES

Device	R1 (K)	R2 (K)	Package	Shipping [†]
NSB4904DW1T1G	47	47	SOT-363 (Pb-Free)	3000/Tape & Reel
NSB4904DW1T2G	47	47	SOT-363 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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TYPICAL ELECTRICAL CHARACTERISTICS – NSB4904DW1T1G, NSB4904DW1T2G NPN TRANSISTOR

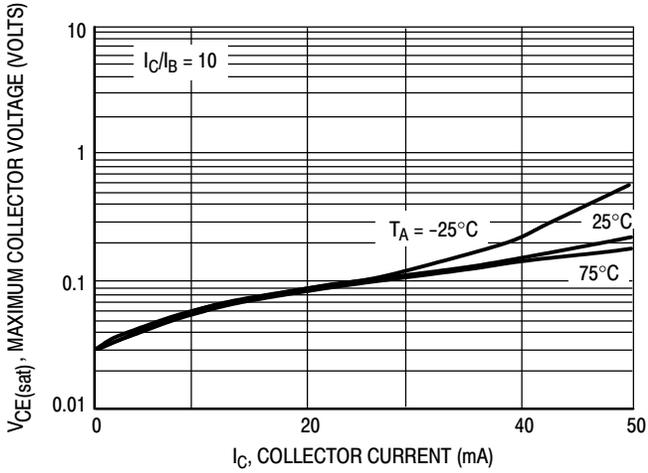


Figure 2. $V_{CE(sat)}$ versus I_C

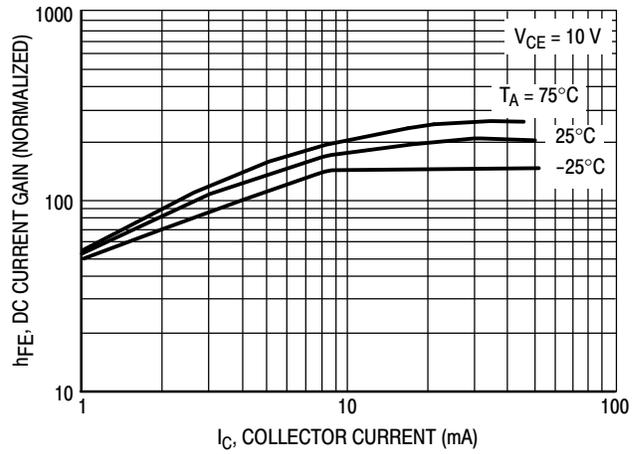


Figure 3. DC Current Gain

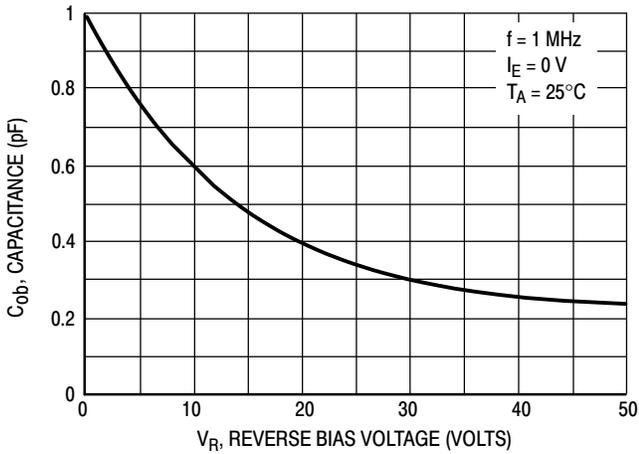


Figure 4. Output Capacitance

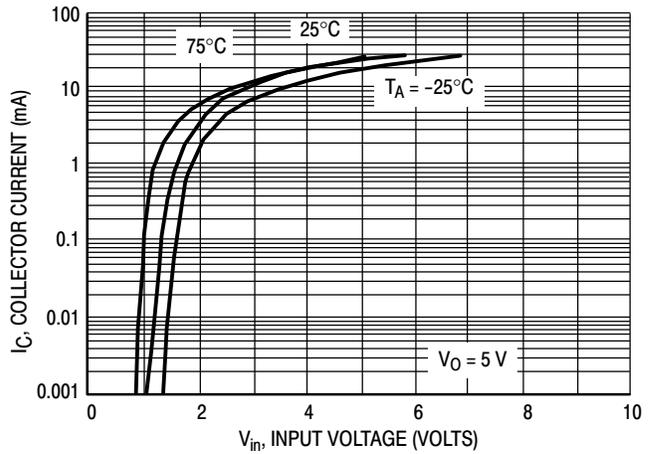


Figure 5. Output Current versus Input Voltage

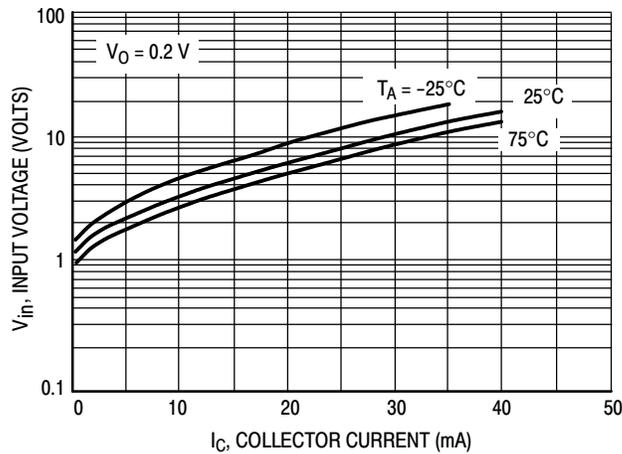


Figure 6. Input Voltage versus Output Current

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TYPICAL ELECTRICAL CHARACTERISTICS – NSB4904DW1T1G, NSB4904DW1T2G PNP TRANSISTOR

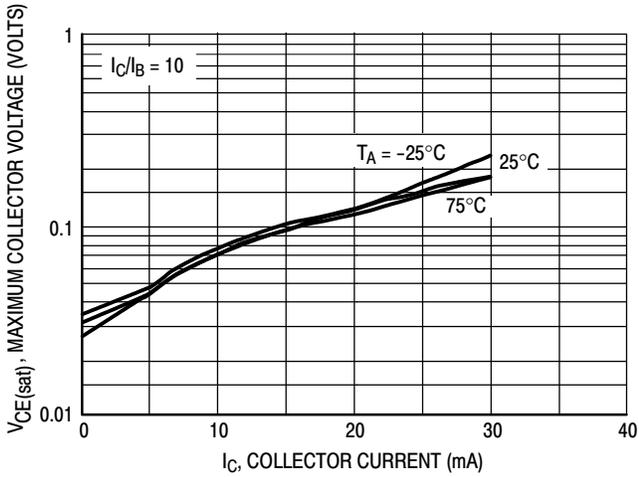


Figure 7. $V_{CE(sat)}$ versus I_C

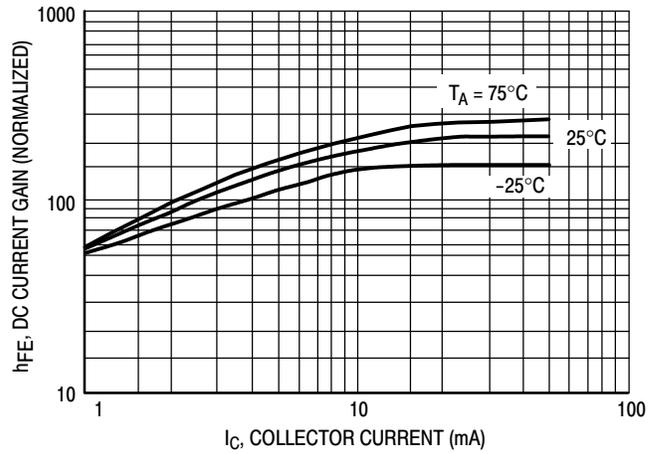


Figure 8. DC Current Gain

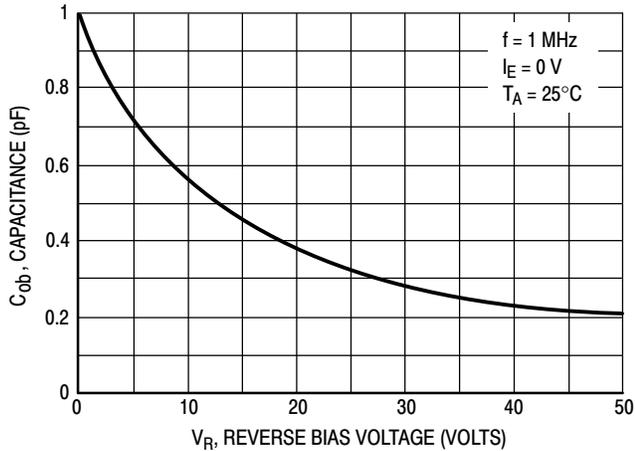


Figure 9. Output Capacitance

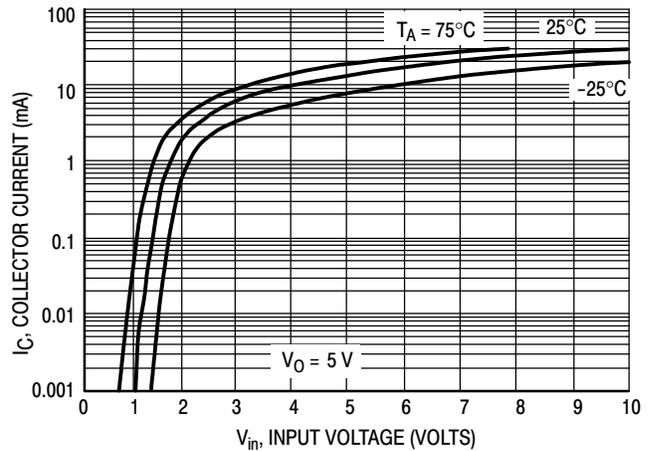


Figure 10. Output Current versus Input Voltage

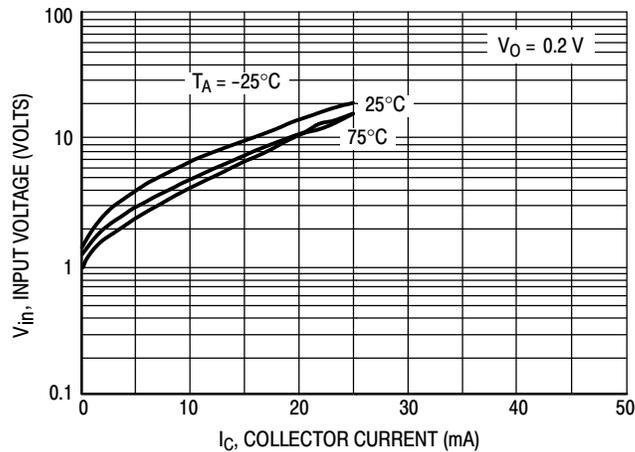


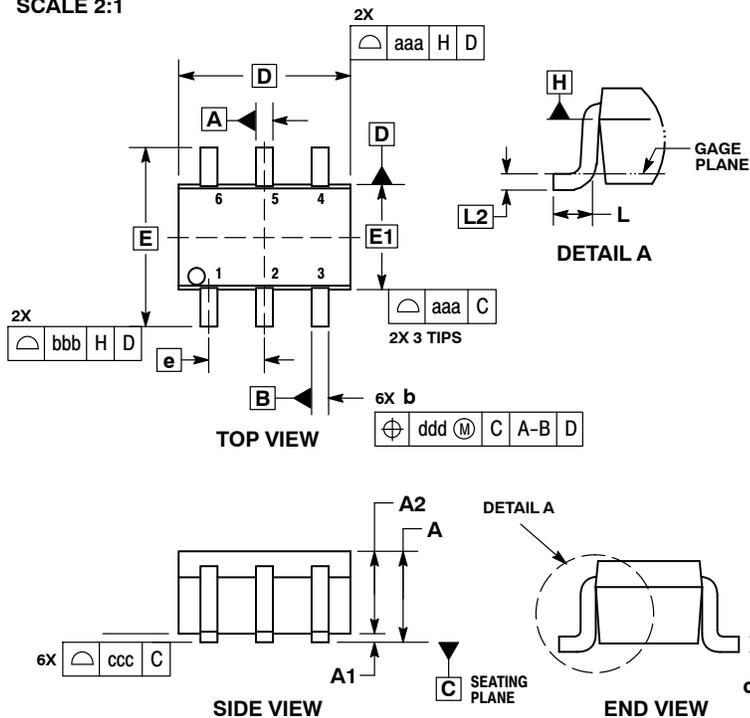
Figure 11. Input Voltage versus Output Current



1
SCALE 2:1

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CASE 419B-02
ISSUE Y

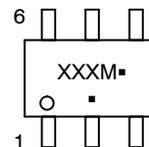
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



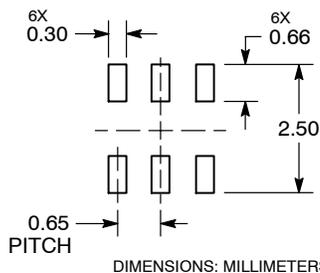
- XXX = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (j) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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