

**PI6C49CB02Q**

**Automotive AEC-Q100 Qualified Low Skew, 1-To-2 LVCMOS / LVTTTL Fanout Buffer**

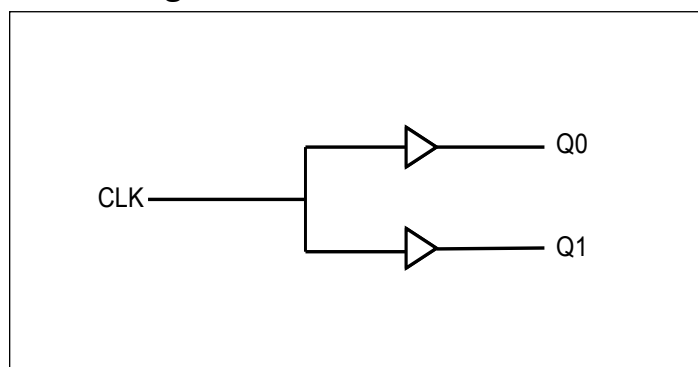
**Features**

- 2 LVCMOS / LVTTTL outputs
- LVCMOS / LVTTTL clock input accepts LVCMOS or LVTTTL input levels
- Maximum output frequency: 250MHz
- Output skew: 25ps (typical)
- Part-to-part skew: 250ps (typical)
- Small 8 lead SOIC package saves board space
- Full 3.3V, 2.5V operation modes
- AEC-Q100 Qualified
- Automotive Grade 2 temperature range (-40 to 105 °C)
- Automotive Grade 3 temperature range (-40 to 85 °C)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free “Green” Device (Note 3)
- The PI6C49CB02Q is suitable for automotive applications requiring specific change control and is AEC-Q100 qualified, has a grade 2, -40 to 105 °C temperature rating and grade 3, -40 to 85 °C temperature rating, is PPAP capable, and is manufactured in IATF16949:2016 certified facilities.
- Package: 8-Pin, SOIC (W)

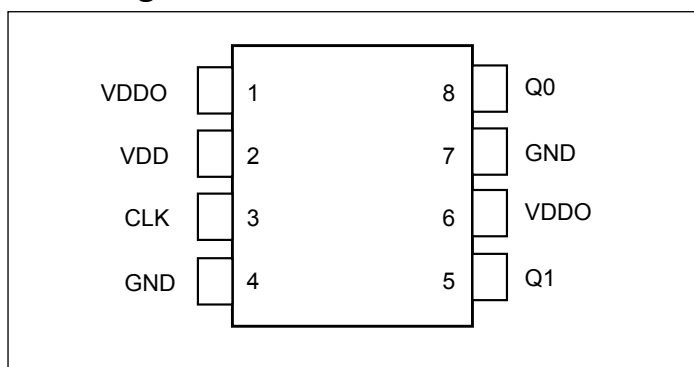
**Description**

The PI6C49CB02Q is an automotive qualified low skew, 1-to-2 LVCMOS/LVTTTL High Performance Fanout Buffer. The PI6C49CB02Q has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTTL input levels. The PI6C49CB02Q features a pair of LVCMOS/LVTTTL outputs. Guaranteed output and part-to-part skew characteristics make the PI6C49CB02Q ideal for clock distribution applications demanding well defined performance and repeatability.

**Block Diagram**



**Pin Assignment**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Descriptions

Pin#	Pin Name	Pin Type		Pin Description
1, 6	VDDO	Power		Output supply pins.
2	VDD	Power		Core supply pin.
3	CLK	Input	Pull-down	LVC MOS / LVTTTL clock input.
4, 7	GND	Power		Power supply ground.
5	Q1	Output		Single clock output. LVC MOS / LVTTTL interface levels.
8	Q0	Output		Single clock output. LVC MOS / LVTTTL interface levels.

Note: Pull-down refer to internal input resistors, typical values in Pin Characteristics table.

## Pin Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$C_N$	Capacitance			4		pF
$R_{PULLDOWN}$	Input Pull-down Resistor			51		k $\Omega$
$R_{OUT}$	Output Impedance		5	7	12	$\Omega$

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, VDD, VDDO .....	4.6V
Inputs, $V_I$ .....	-0.5V to VDD+0.5V
Output, $V_O$ .....	-0.5V to VDDO+0.5V
Storage Temperature .....	-65°C to 150°C
ESD Protection (HBM) .....	2000V
Junction Temperature .....	125°C (Max)

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics

is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Automotive Grade 2)	-40		+105	°C
Ambient Operating Temperature (Automotive Grade 3)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+2.375		+3.465	V

## Power Supply DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Core Supply Voltage	3.3V Operation	3.135	3.3	3.465	V
		2.5V Operation	2.375	2.5	2.625	
VDDO	Output Power Supply Voltage	3.3V Supply	3.135	3.3	3.465	V
		2.5V Supply	2.375	2.5	2.625	
IDD	Power Supply Current	$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$			5	mA
IDDO	Output Supply Current	Unloaded, 25 MHz, $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$			6.5	mA
IDD	Power Supply Current	$T_A = -40^{\circ}\text{C}$ to $105^{\circ}\text{C}$			5	mA
IDDO	Output Supply Current	Unloaded, 25 MHz, $T_A = -40^{\circ}\text{C}$ to $105^{\circ}\text{C}$			6.5	mA

Note: Parameters measured up to  $f_{\text{max}}$  unless otherwise noted.

**PI6C49CB02Q**
**LVCMOS / LVTTTL DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage	VDD = 3.3V	2		VDD+0.3	V
		VDD = 2.5V	1.7		VDD+0.3	
$V_{IL}$	Input Low Voltage	VDD = 3.3V	-0.3		0.8	V
		VDD = 2.5V	-0.3		0.8	
$I_{IH}$	Input High Current	VDD = $V_{IN} = 3.465\text{V}$			100	$\mu\text{A}$
		VDD = $V_{IN} = 2.625\text{V}$			80	
$I_{IL}$	Input Low Current	VDD = 3.465V, $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		VDD = 2.625V, $V_{IN} = 0\text{V}$	-5			
$V_{OH}$	Output High Voltage	VDDO = 3.3V $I_{OH} = -100\mu\text{A}$	2.9			V
		VDDO = 2.5V $I_{OH} = -100\mu\text{A}$	2.2			V
$V_{OL}$	Output Low Voltage	VDDO = 3.3V $I_{OL} = 100\mu\text{A}$			0.2	V
		VDDO = 2.5V $I_{OL} = 100\mu\text{A}$			0.2	V

**LVCMOS / LVTTTL DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$** 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage	VDD = 3.3V	2		VDD+0.3	V
		VDD = 2.5V	1.7		VDD+0.3	
$V_{IL}$	Input Low Voltage	VDD = 3.3V	-0.3		0.8	V
		VDD = 2.5V	-0.3		0.8	
$I_{IH}$	Input High Current	VDD = $V_{IN} = 3.465\text{V}$			100	$\mu\text{A}$
		VDD = $V_{IN} = 2.625\text{V}$			80	
$I_{IL}$	Input Low Current	VDD = 3.465V, $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		VDD = 2.625V, $V_{IN} = 0\text{V}$	-5			
$V_{OH}$	Output High Voltage	VDDO = 3.3V $I_{OH} = -100\mu\text{A}$	2.9			V
		VDDO = 2.5V $I_{OH} = -100\mu\text{A}$	2.2			V
$V_{OL}$	Output Low Voltage	VDDO = 3.3V $I_{OL} = 100\mu\text{A}$			0.2	V
		VDDO = 2.5V $I_{OL} = 100\mu\text{A}$			0.2	V

**PI6C49CB02Q**
**AC Characteristics, VDD = 3.3V  $\pm$  5%, T<sub>A</sub> = -40°C to 85°C**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f <sub>MAX</sub>	Output Frequency	VDDO = 3.3V	4		250	MHz
		VDDO = 2.5V	4		250	
tp <sub>LH</sub>	Propagation Delay, Low-to-High <sup>(1)</sup>	VDDO = 3.3V, f ≤ 250MHz	1.4		2.2	ns
		VDDO = 2.5V, f ≤ 250MHz	1.5		3.0	
tsk(o)	Output Skew <sup>(2)</sup>			25	80	ps
tsk(pp)	Part-to-Part Skew <sup>(3)</sup>			250	800	ps
t <sub>R</sub>	Output Rise Time <sup>(4)</sup>	VDDO = 3.3V	100	300	400	ps
		VDDO = 2.5V	100	350	500	
t <sub>F</sub>	Output Fall Time <sup>(4)</sup>	VDDO = 3.3V	100	300	400	ps
		VDDO = 2.5V	100	350	500	
odc	Output Duty Cycle <sup>(5)</sup>	f ≤ 133MHz	48		52	%
		133MHz < f ≤ 200MHz	47		53	%
		200MHz < f ≤ 250MHz	47		53	%
t <sub>jit</sub>	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.1		ps
		125MHz (@12kHz to 20MHz)		0.07		ps

**Note:**

Parameters measured at f<sub>MAX</sub> unless otherwise noted.

1. Measured from VDD /2 of the input to VDDO /2 of the output.

2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO /2.

3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO /2.

4. Defined from 20% to 80%

5. Measured at VDDO /2

**AC Characteristics**,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $105^{\circ}C$ 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{MAX}$	Output Frequency	$V_{DDO} = 3.3V$	4		250	MHz
		$V_{DDO} = 2.5V$	4		250	
$t_{pLH}$	Propagation Delay, Low-to-High <sup>(1)</sup>	$V_{DDO} = 3.3V, f \leq 250MHz$	1.4		2.2	ns
		$V_{DDO} = 2.5V, f \leq 250MHz$	1.5		3.0	
$tsk(o)$	Output Skew <sup>(2)</sup>			25	80	ps
$tsk(pp)$	Part-to-Part Skew <sup>(3)</sup>			250	800	ps
$t_R$	Output Rise Time <sup>(4)</sup>	$V_{DDO} = 3.3V$	100	300	400	ps
		$V_{DDO} = 2.5V$	100	350	500	
$t_F$	Output Fall Time <sup>(4)</sup>	$V_{DDO} = 3.3V$	100	300	400	ps
		$V_{DDO} = 2.5V$	100	350	500	
odc	Output Duty Cycle <sup>(5)</sup>	$f \leq 133MHz$	48		52	%
		$133MHz < f \leq 200MHz$	47		53	%
		$200MHz < f \leq 250MHz$	47		53	%
$t_{jit}$	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.1		ps
		125MHz (@12kHz to 20MHz)		0.07		ps

**Note:**

Parameters measured at  $f_{MAX}$  unless otherwise noted.

1. Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .
4. Defined from 20% to 80%
5. Measured at  $V_{DDO}/2$

**AC Characteristics**,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

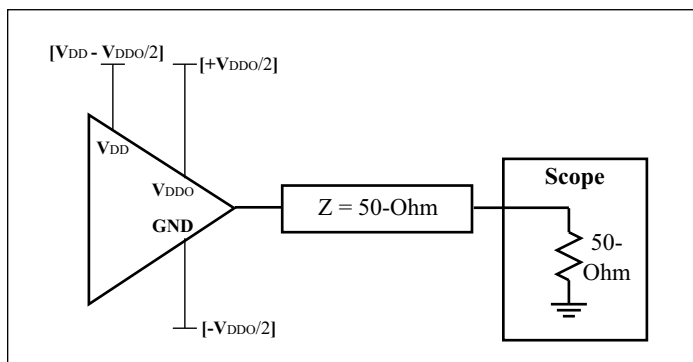
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{MAX}$	Output Frequency	$V_{DDO} = 2.5V$	4		250	MHz
$t_{pLH}$	Propagation Delay, Low-to-High <sup>(1)</sup>	$V_{DDO} = 2.5V, f \leq 250MHz$	1.5		2.8	ns
$tsk(o)$	Output Skew <sup>(2)</sup>			25	75	ps
$tsk(pp)$	Part-to-Part Skew <sup>(3)</sup>			250	800	ps
$t_R$	Output Rise Time <sup>(4)</sup>	$V_{DDO} = 2.5V$	100	350	500	ps
$t_F$	Output Fall Time <sup>(4)</sup>	$V_{DDO} = 2.5V$	100	350	500	ps
odc	Output Duty Cycle <sup>(5)</sup>	$f \leq 133MHz$	48		52	%
		$133MHz < f \leq 200MHz$	47		53	%
		$200MHz < f \leq 250MHz$	42		58	%
$t_{jit}$	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.1		ps
		125MHz (@12kHz to 20MHz)		0.07		ps

**Note:**

Parameters measured at  $f_{MAX}$  unless otherwise noted.

1. Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .
4. Defined from 20% to 80%
5. Measured at  $V_{DDO}/2$

**AC Test Circuit Load**



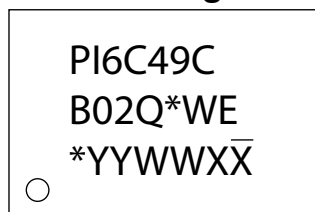
**PI6C49CB02Q**
**AC Characteristics**,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{MAX}$	Output Frequency	$V_{DDO} = 2.5V$	4		250	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High <sup>(1)</sup>	$V_{DDO} = 2.5V$ , $f \leq 250\text{MHz}$	1.5		2.8	ns
$tsk(o)$	Output Skew <sup>(2)</sup>			25	75	ps
$tsk(pp)$	Part-to-Part Skew <sup>(3)</sup>			250	800	ps
$t_R$	Output Rise Time <sup>(4)</sup>	$V_{DDO} = 2.5V$	100	350	500	ps
$t_F$	Output Fall Time <sup>(4)</sup>	$V_{DDO} = 2.5V$	100	350	500	ps
odc	Output Duty Cycle <sup>(5)</sup>	$f \leq 133\text{MHz}$	48		52	%
		$133\text{MHz} < f \leq 200\text{MHz}$	47		53	%
		$200\text{MHz} < f \leq 250\text{MHz}$	42		58	%
$t_{jit}$	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.1		ps
		125MHz (@12kHz to 20MHz)		0.07		ps

**Note:**

Parameters measured at  $f_{MAX}$  unless otherwise noted.

1. Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .
4. Defined from 20% to 80%
5. Measured at  $V_{DDO}/2$

**Part Marking**


\*: Die Rev (2 or 3)

YY: Year

WW: Workweek

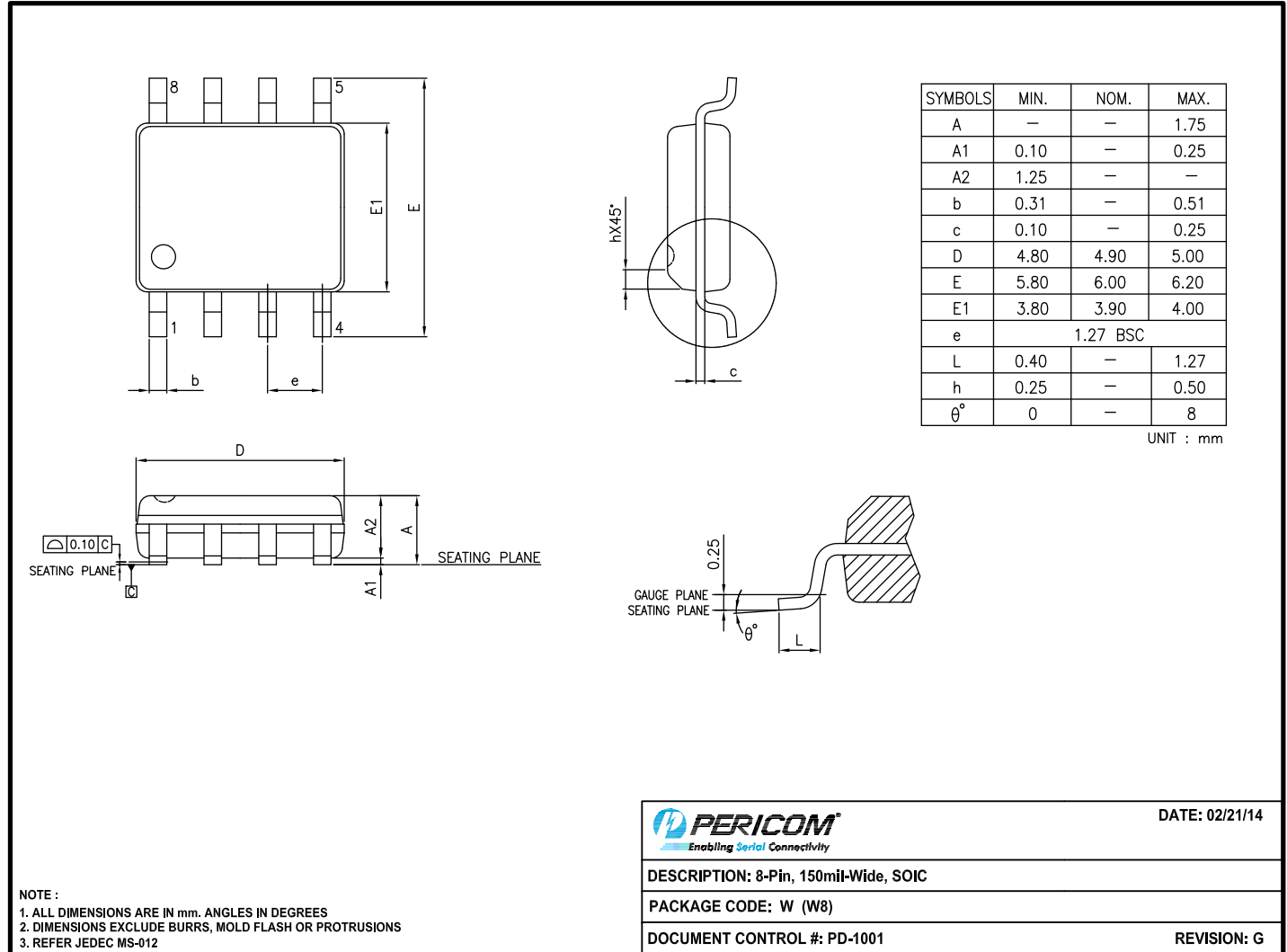
1st X: Assembly Site Code

2nd X: Wafer Site Code



**PI6C49CB02Q**

## Packaging Mechanical: 8-SOIC (W)



15-0103

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

## Ordering Information

Ordering Code	Package Code	Operating Temperature	Package Description
PI6C49CB02Q2WEX	W	-40 to 105°C	8-pin, 150mil-Wide (SOIC)
PI6C49CB02Q3WEX	W	-40 to 85°C	8-pin, 150mil-Wide (SOIC)

### Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Q = Automotive Compliant
5. 2 and 3 = AEC-Q100 Grade Level
6. E = Pb-free and Green
7. X suffix = Tape/Reel

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