

CoolGaN™ Gen2
650 V CoolGaN™ enhancement-mode Power Transistor

Infineon's CoolGaN™ is a highly efficient GaN (gallium nitride) transistor technology for power conversion in the voltage range up to 650 V. With extensive experience on the semiconductor market, Infineon's GaN technology brought the e-mode concept to maturity with end-to-end production in high volumes. The pioneering quality ensures the highest standards and offers the most reliable and performing solution among all GaN HEMTs on the market.

Features

- Enhancement mode transistor - Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- ESD (HBM/CDM) JEDEC standards

Benefits

- Improves system efficiency
- Improves power density
- Enables highest operating frequency
- System cost reduction savings
- Reduces EMI

Potential applications

Industrial, telecom, datacenter SMPS, charger and adapter based on half-bridge topologies (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC).

Product validation

Fully qualified according to JEDEC for Industrial Applications
Please note: Target Datasheet to change without further notice

Table 1 Key Performance Parameters

Table with 3 columns: Parameter, Value, Unit. Rows include V\_DS,max (650 V), R\_DS(on),max (66 mΩ), Q\_g,typ (6.6 nC), I\_D,pulse (60 A), Q\_oss @ 400 V (36 nC), and Q\_rr (0 nC).

Table with 4 columns: Type/Ordering Code, Package, Marking, Related Links. Row 1: IGOT65R055D2, PG-DSO-20, 65R055D2, see Appendix A.

PG-DSO-20

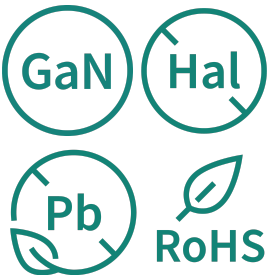
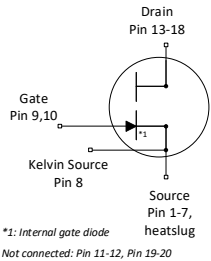
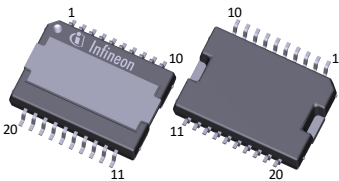




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Datasheet

## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

**Table 2 Maximum ratings**

| Parameter                                         | Symbol          | Values     |      |          | Unit | Note/ Test Condition                                                                                                                                                                                 |
|---------------------------------------------------|-----------------|------------|------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                   |                 | Min.       | Typ. | Max.     |      |                                                                                                                                                                                                      |
| Drain source voltage, continuous                  | $V_{DS,max}$    | -          | -    | 650      | V    | $V_{GS} = 0\text{ V}$ , derating recommendation acc. JEDEC JEP198                                                                                                                                    |
| Leakage current at drain source transient voltage | $I_{DS,trans}$  | -          | -    | 12       | mA   | $V_{GS} = 0\text{ V}$ , $V_{DS,trans} = 900\text{ V}$                                                                                                                                                |
| Drain source voltage transient                    | $V_{DS,trans}$  | -          | -    | 900      | V    | <1 % duty cycle, <1 $\mu\text{s}$ , 1 M pulses                                                                                                                                                       |
| Drain source voltage, pulsed                      | $V_{DS,pulse}$  | -          | -    | 750      | V    | $T_j = 25\text{ °C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$                                                                                                            |
|                                                   | $V_{DS,pulsed}$ | -          | -    | 650      |      | $T_j = 125\text{ °C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$                                                                                                           |
| Switching surge voltage, pulsed                   | $V_{DS,surge}$  | -          | -    | 750      | V    | DC bus voltage = 700 V; turn off V <sub>DS,pulse</sub> = 750 V; turn on $I_{D,pulse} = 27\text{ A}$ ; $T_j = 105\text{ °C}$ ; $f \leq 100\text{ kHz}$ , $t \leq 100\text{ sec.}$ (10 million pulses) |
| Continuous current, drain source <sup>1)</sup>    | $I_D$           | -          | -    | 28       | A    | $T_c = 25\text{ °C}$ ; $T_j = T_{j,max}$                                                                                                                                                             |
| Pulsed current, drain source                      | $I_{D,pulse}$   | -60<br>-35 | -    | 60<br>35 | A    | $T_j = 25\text{ °C}$ ; $I_G = 26\text{ mA}$ ; See Diagram 3, 5<br>$T_j = 125\text{ °C}$ ; $I_G = 26\text{ mA}$ ; See Diagram 4, 6                                                                    |
| Gate current, continuous <sup>2)</sup>            | $I_{G,avg}$     | -          | -    | 20       | mA   | $T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; See Table 9                                                                                                                                         |
| Gate current, pulsed <sup>2)</sup>                | $I_{G,pulsed}$  | -2         | -    | 2        | A    | $T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; $t_{PULSE} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; See Table 9                                                                                     |
| Gate source voltage, continuous <sup>2)</sup>     | $V_{GS}$        | -10        | -    | -        | V    | $T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; See Diagram 12                                                                                                                                      |
| Gate source voltage, pulsed <sup>2)</sup>         | $V_{GS,pulse}$  | -25        | -    | -        | V    | $T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; $t_{PULSE} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; open drain                                                                                      |
| Power dissipation                                 | $P_{tot}$       | -          | -    | 83       | W    | $T_c = 25\text{ °C}$                                                                                                                                                                                 |
| Operating junction temperature                    | $T_j$           | -55        | -    | 150      | °C   | -                                                                                                                                                                                                    |
| Storage temperature                               | $T_{stg}$       | -55        | -    | 150      | °C   | Max shelf life depends on storage conditions                                                                                                                                                         |
| Drain-source voltage slew-rate                    | $dv/dt$         | -          | -    | 200      | V/ns | -                                                                                                                                                                                                    |

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.75$

<sup>2)</sup> We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter                                              | Symbol     | Values |      |      | Unit | Note/ Test Condition                                                                                                                                    |
|--------------------------------------------------------|------------|--------|------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                        |            | Min.   | Typ. | Max. |      |                                                                                                                                                         |
| Thermal resistance, junction - case                    | $R_{thJC}$ | -      | -    | 1.5  | °C/W | -                                                                                                                                                       |
| Thermal resistance, junction - ambient                 | $R_{thJA}$ | -      | -    | 70   | °C/W | Device on PCB, minimum footprint                                                                                                                        |
| Thermal resistance, junction - ambient for SMD version | $R_{thJA}$ | -      | -    | 61   | °C/W | Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm <sup>2</sup> (one layer, 70 µm thickness) copper area. PCB is vertical without air stream cooling. |
| Reflow soldering temperature                           | $T_{sold}$ | -      | -    | 260  | °C   | reflow MSL3                                                                                                                                             |

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless specified otherwise

**Table 4 Static characteristics**

| Parameter                            | Symbol          | Values   |                |            | Unit          | Note/ Test Condition                                                                                                                      |
|--------------------------------------|-----------------|----------|----------------|------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------|
|                                      |                 | Min.     | Typ.           | Max.       |               |                                                                                                                                           |
| Gate threshold voltage               | $V_{GS(th)}$    | 0.9<br>- | 1.2<br>1       | 1.6<br>-   | V             | $I_{DS}=2.6\text{ mA}$ ; $V_{DS}=10\text{ V}$ ; $T_j=25\text{ °C}$<br>$I_{DS}=2.6\text{ mA}$ ; $V_{DS}=10\text{ V}$ ; $T_j=150\text{ °C}$ |
| Gate-Source reverse clamping voltage | $V_{GS, clamp}$ | -        | -              | -8         | V             | $I_{GS}=-1\text{ mA}$                                                                                                                     |
| Drain-Source leakage current         | $I_{DSS}$       | -        | 1<br>20        | 100<br>-   | $\mu\text{A}$ | $V_{DS}=650\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$<br>$V_{DS}=650\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=150\text{ °C}$     |
| Drain-Source on-state resistance     | $R_{DS(on)}$    | -        | 0.055<br>0.120 | 0.066<br>- | $\Omega$      | $I_G=26\text{ mA}$ ; $I_D=7.9\text{ A}$ ; $T_j=25\text{ °C}$<br>$I_G=26\text{ mA}$ ; $I_D=7.9\text{ A}$ ; $T_j=150\text{ °C}$             |
| Gate resistance                      | $R_{G,int}$     | -        | tbd            | -          | $\Omega$      | LCR impedance measurement; $f=f_{res}$ , open drain;                                                                                      |

**Table 5 Dynamic characteristics**

| Parameter                                                  | Symbol       | Values |      |      | Unit | Note/ Test Condition                                                                                                                                        |
|------------------------------------------------------------|--------------|--------|------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                            |              | Min.   | Typ. | Max. |      |                                                                                                                                                             |
| Input capacitance                                          | $C_{iss}$    | -      | 330  | -    | pF   | $V_{GS}=0\text{ V}$ ; $V_{DS}=400\text{ V}$ , $f=1\text{ MHz}$                                                                                              |
| Output capacitance                                         | $C_{oss}$    | -      | 53   | -    | pF   | $V_{GS}=0\text{ V}$ , $V_{DS}=400\text{ V}$ , $f=1\text{ MHz}$                                                                                              |
| Reverse Transfer capacitance                               | $C_{rss}$    | -      | 0.63 | -    | pF   | $V_{GS}=0\text{ V}$ , $V_{DS}=400\text{ V}$ , $f=1\text{ MHz}$                                                                                              |
| Effective output capacitance, energy related <sup>3)</sup> | $C_{o(er)}$  | -      | tbd  | -    | pF   | $V_{DS}=0\text{ to }400\text{ V}$                                                                                                                           |
| Effective output capacitance, time related <sup>4)</sup>   | $C_{o(tr)}$  | -      | tbd  | -    | pF   | $V_{GS}=0\text{ V}$ ; $V_{DS}=0\text{ to }400\text{ V}$ ; $I_D=\text{const}$                                                                                |
| Output charge                                              | $Q_{oss}$    | -      | 36   | -    | nC   | $V_{DS}=0\text{ to }400\text{ V}$                                                                                                                           |
| Turn-on delay time                                         | $t_{d(on)}$  | -      | tbd  | -    | ns   | $I_D=8\text{ A}$ ; $R_{ON}=5.6\text{ Ohm}$ ; $R_{OFF}=5.6\text{ Ohm}$ ; $R_{SS}=330\text{ Ohm}$ ; $C_C=3.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8 |
| Turn-off delay time                                        | $t_{d(off)}$ | -      | tbd  | -    | ns   | $I_D=8\text{ A}$ ; $R_{ON}=5.6\text{ Ohm}$ ; $R_{OFF}=5.6\text{ Ohm}$ ; $R_{SS}=330\text{ Ohm}$ ; $C_C=3.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8 |
| Rise time                                                  | $t_r$        | -      | tbd  | -    | ns   | $I_D=8\text{ A}$ ; $R_{ON}=5.6\text{ Ohm}$ ; $R_{OFF}=5.6\text{ Ohm}$ ; $R_{SS}=330\text{ Ohm}$ ; $C_C=3.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8 |
| Fall time                                                  | $t_f$        | -      | tbd  | -    | ns   | $I_D=8\text{ A}$ ; $R_{ON}=5.6\text{ Ohm}$ ; $R_{OFF}=5.6\text{ Ohm}$ ; $R_{SS}=330\text{ Ohm}$ ; $C_C=3.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8 |

<sup>3)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

<sup>4)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

**Table 6 Gate charge characteristics**

| Parameter   | Symbol | Values |      |      | Unit | Note/ Test Condition                         |
|-------------|--------|--------|------|------|------|----------------------------------------------|
|             |        | Min.   | Typ. | Max. |      |                                              |
| Gate charge | $Q_G$  | -      | 6.6  | -    | nC   | $V_{GS}=0$ to 3 V; $V_{DS}=400$ V, $I_D=8$ A |

**Table 7 Reverse conduction characteristics**

| Parameter                             | Symbol         | Values |      |      | Unit | Note/ Test Condition         |
|---------------------------------------|----------------|--------|------|------|------|------------------------------|
|                                       |                | Min.   | Typ. | Max. |      |                              |
| Source-Drain reverse voltage          | $V_{SD}$       | -      | 2.2  | 2.5  | V    | $V_{GS}=0$ V; $I_{SD}=8$ A   |
| Pulsed current, reverse               | $I_{SD,pulse}$ | -      | -    | 60   | A    | $I_G=26$ mA                  |
| Reverse recovery charge <sup>5)</sup> | $Q_{rr}$       | -      | 0    | -    | nC   | $I_{SD}=8$ A; $V_{DS}=400$ V |

<sup>5)</sup> Excluding  $Q_{oss}$

4 Electrical characteristics diagrams

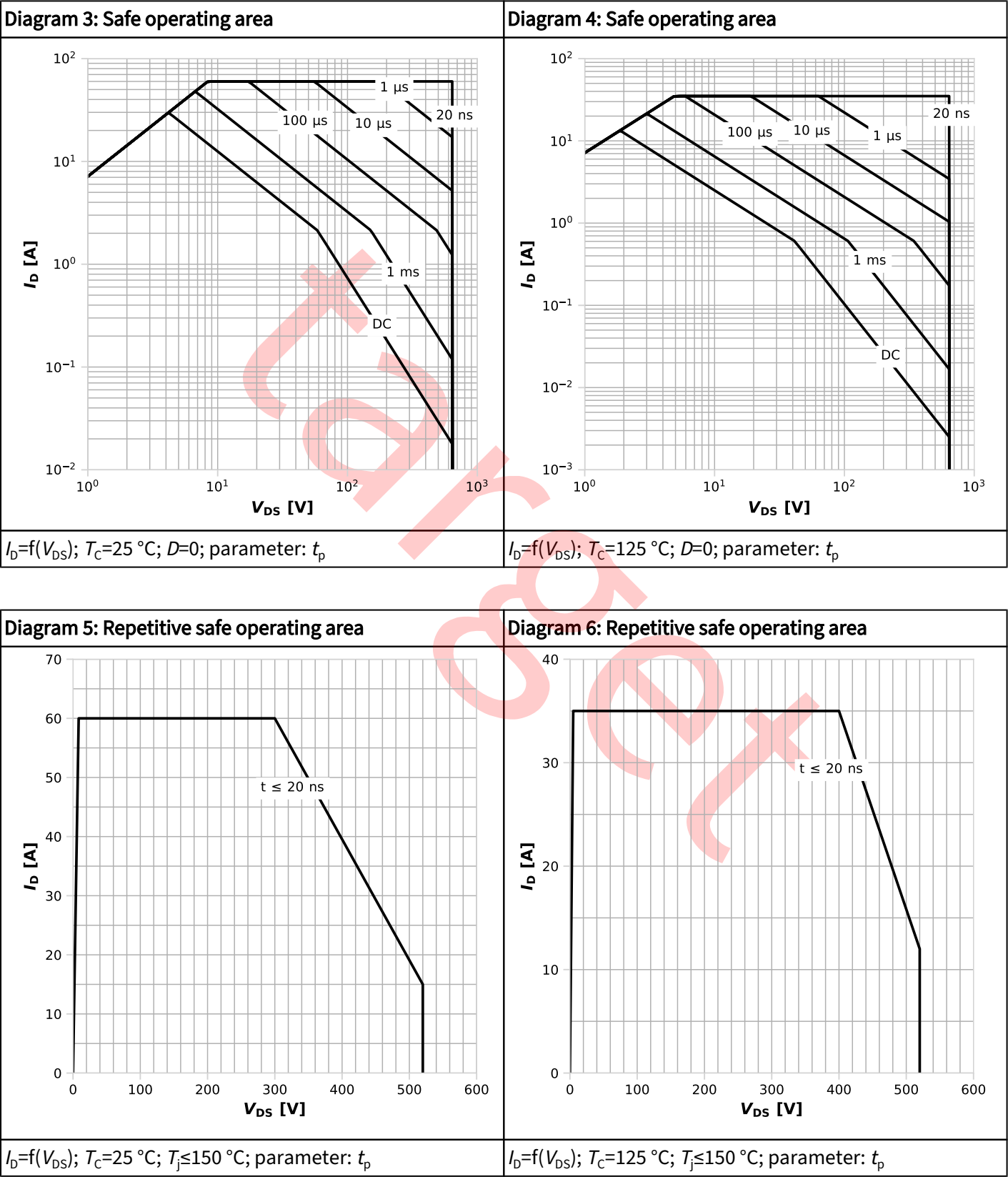
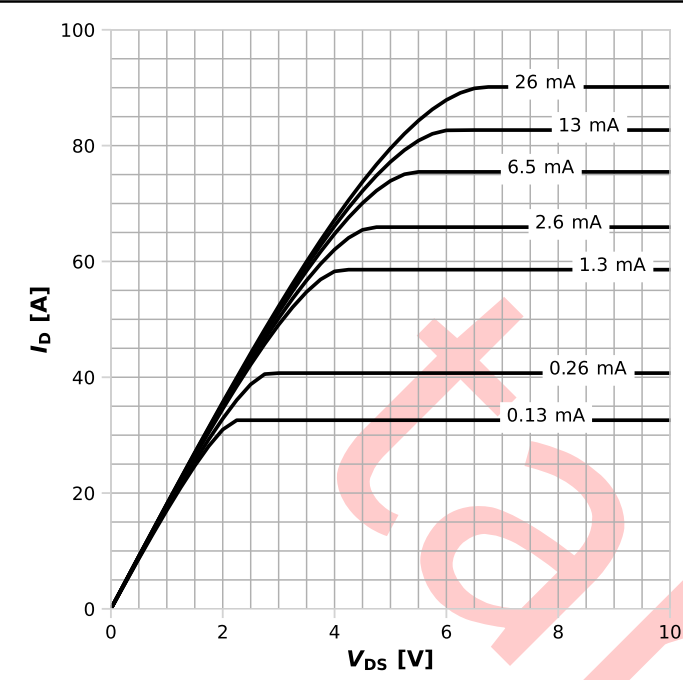


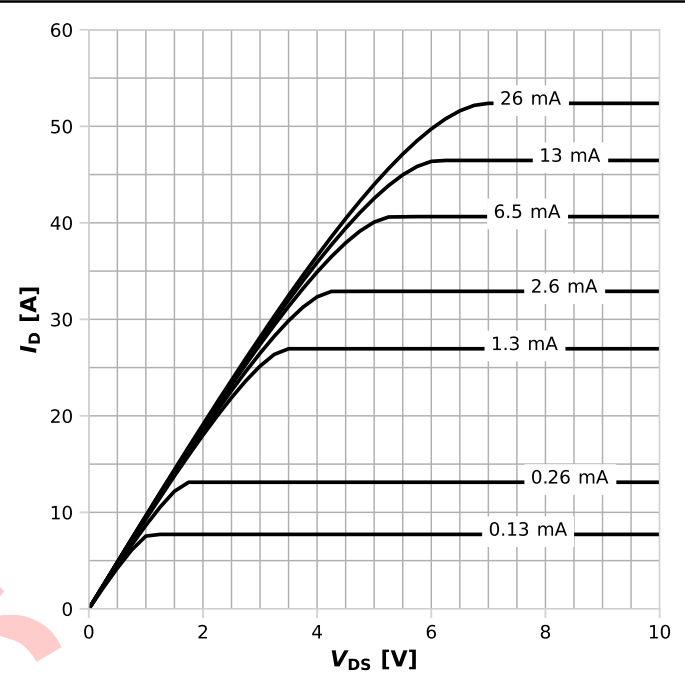


Diagram 7: Typ. output characteristics



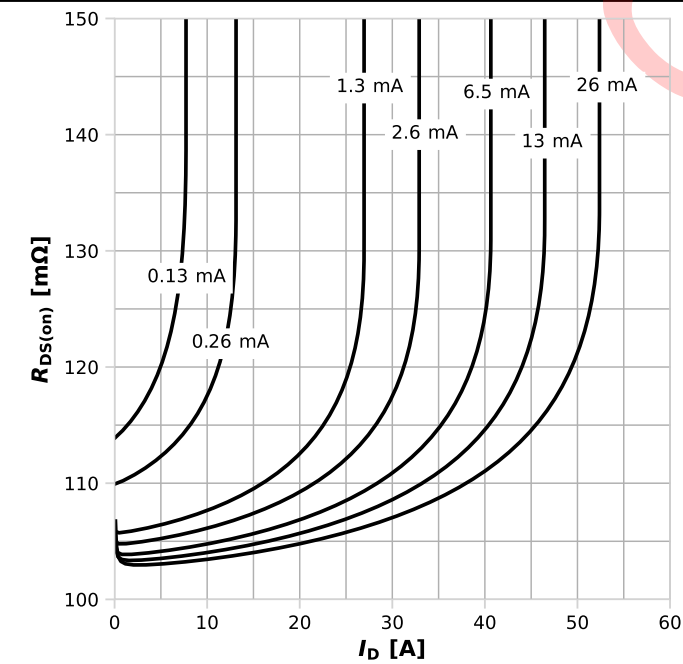
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } I_{GS}$

Diagram 8: Typ. output characteristics



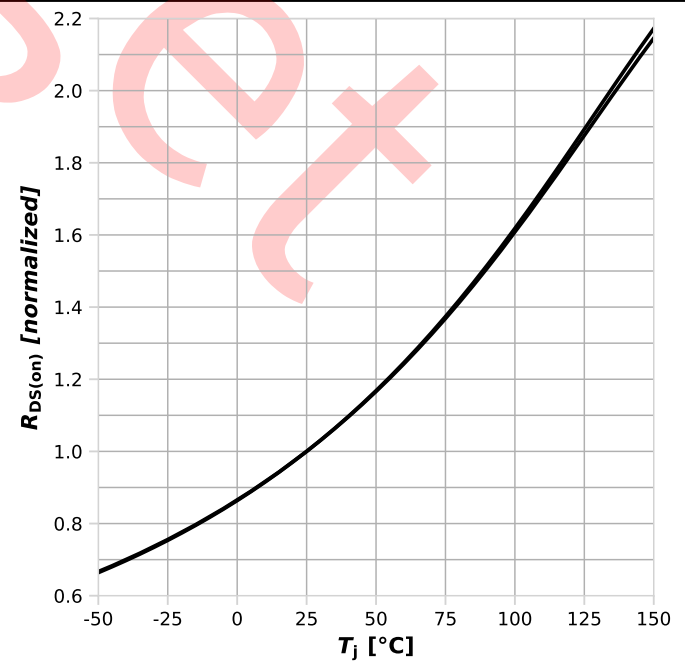
$I_D = f(V_{DS}); T_j = 125\text{ °C}; \text{parameter: } I_{GS}$

Diagram 9: Typ. Drain-source on-state resistance



$R_{DS(on)} = f(I_D); T_j = 125\text{ °C}; \text{parameter: } I_{GS}$

Diagram 10: Drain-source on-state resistance



$R_{DS(on)} = f(T_j); I_D = 7.9\text{ A}$

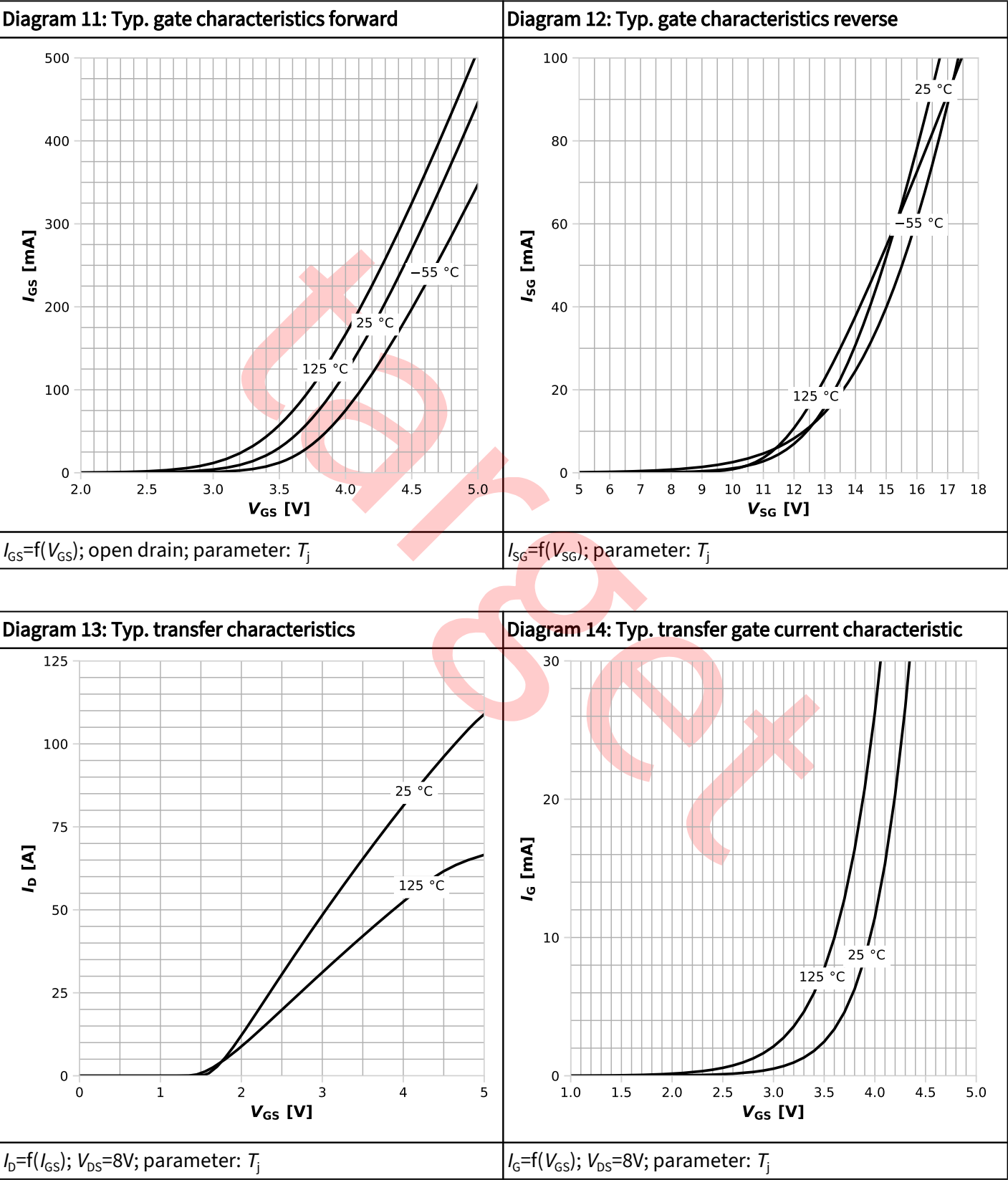
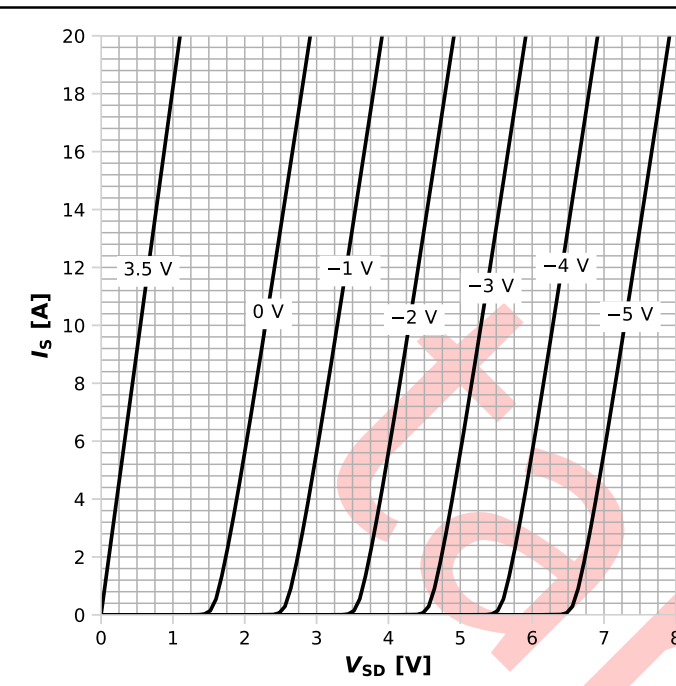
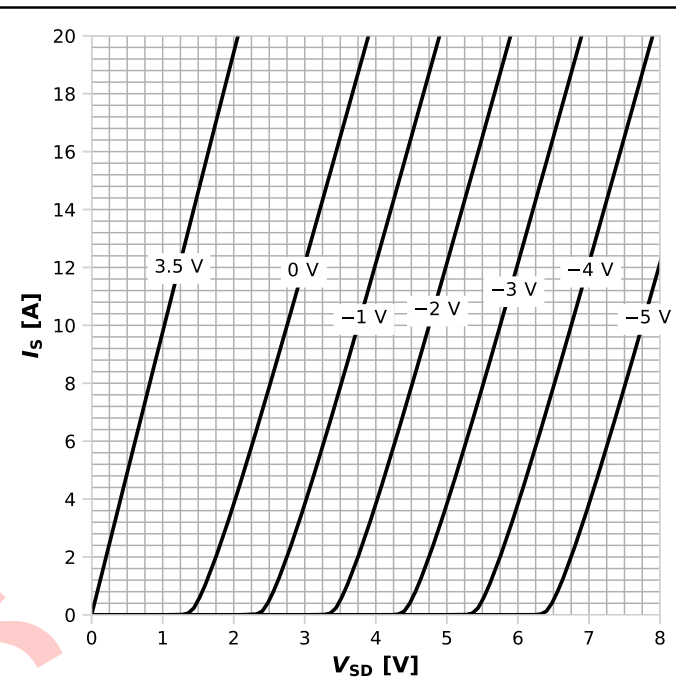


Diagram 15: Typ. channel reverse characteristics



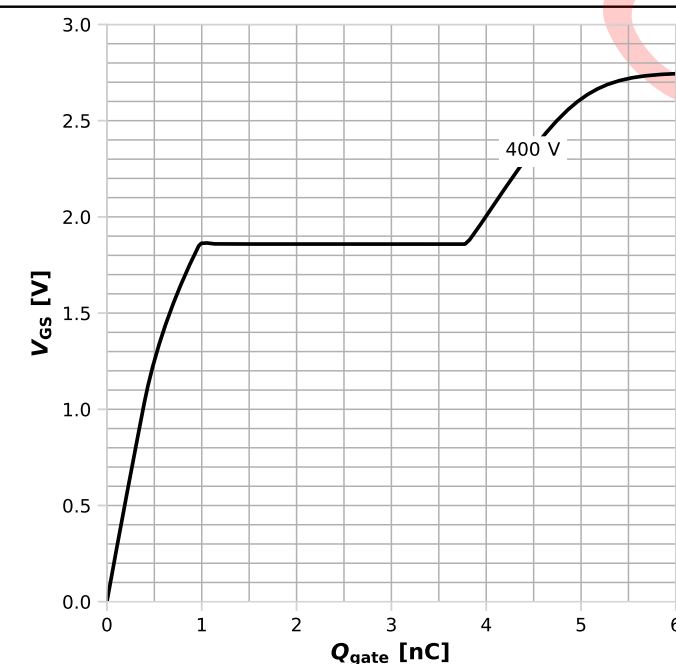
$I_S=f(V_{SD})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 16: Typ. channel reverse characteristics



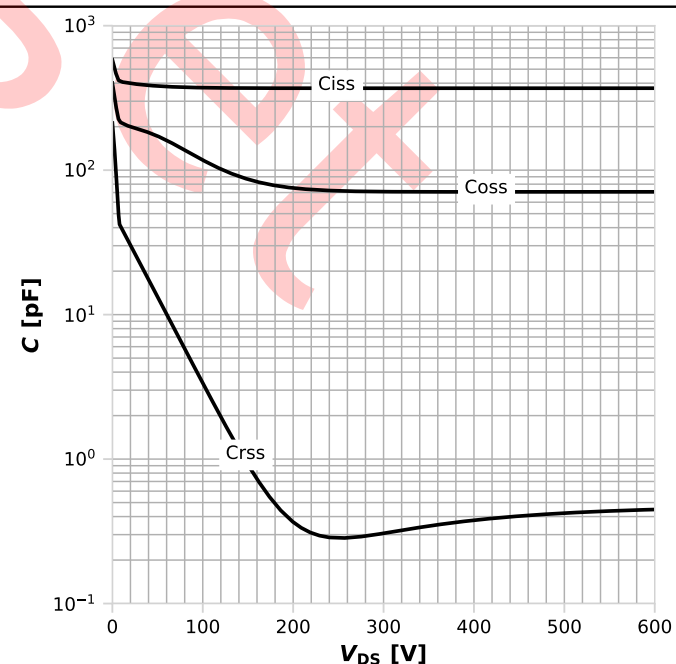
$I_S=f(V_{SD})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 17 Typ. gate charge



$V_{GS}=f(Q_{gate})$ ;  $I_D=8\text{ A}$  pulsed; parameter:  $V_{DD}$

Diagram 18: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$

5 Test Circuits

Table 8 Reverse Channel Characteristics Test

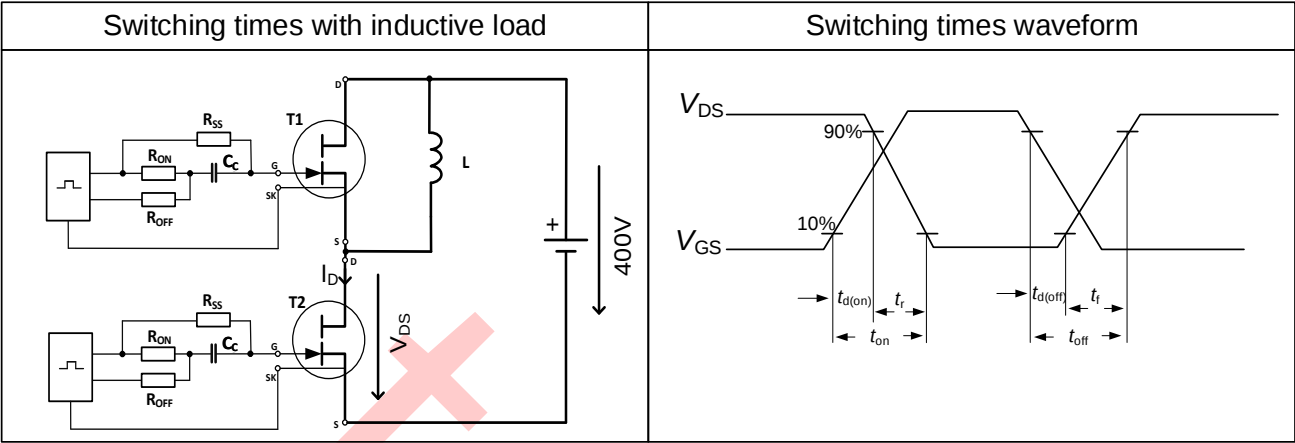
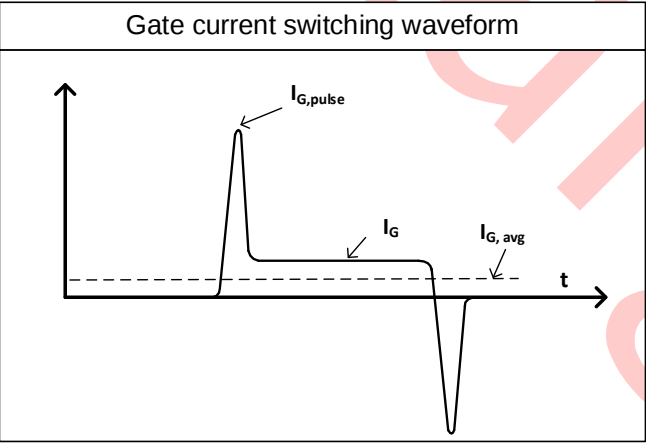
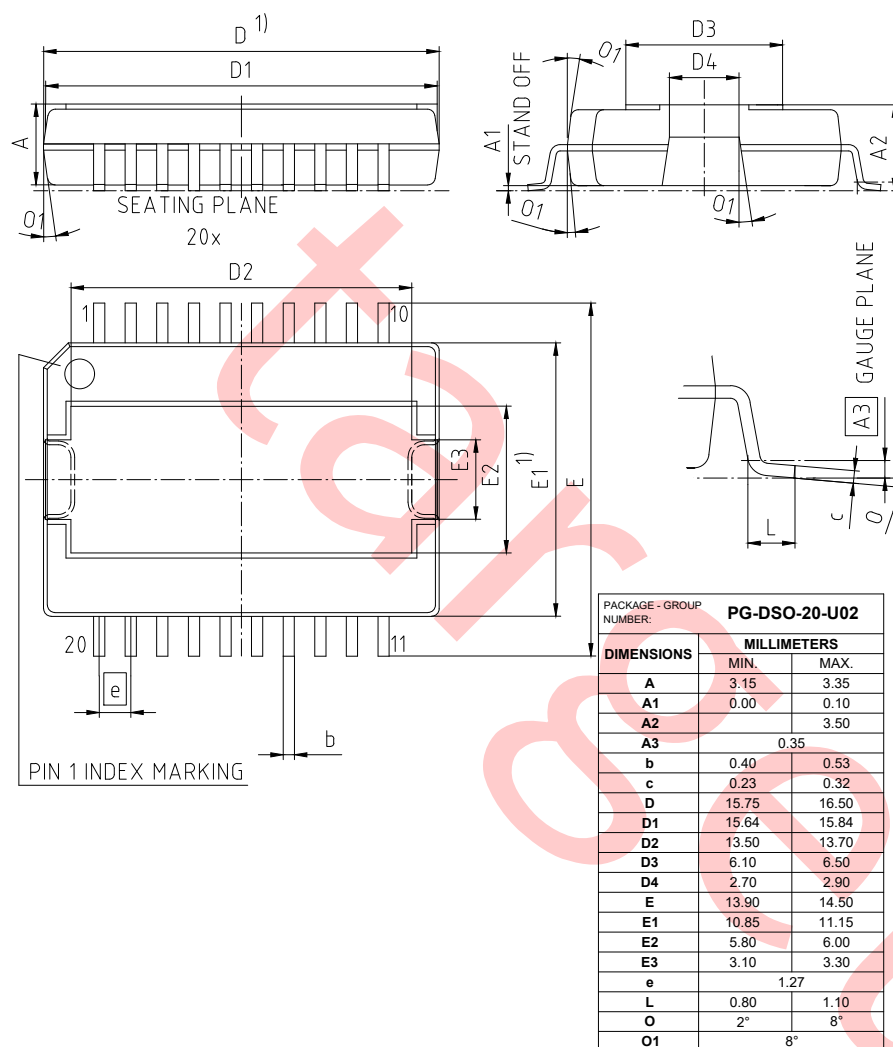


Table 9 Gate current switching waveform



## 6 Package Outlines



1) DOES NOT INCLUDE PLASTIC OR METAL PRUTRUSION OF 0.15 MAX. PER SIDE

**Figure 1** Outline PG-DSO-20, dimensions in mm

## 7 Appendix A

**Table 10**    **Related Links**

- [IFX CoolGaN™ GaN 650 V webpage](#)
- [IFX CoolGaN™ GaN 650 V reliability white paper](#)
- [IFX CoolGaN™ GaN 650 V gate driver application note](#)
- [IFX CoolGaN™ GaN 650 V applications information](#)

datasheet

Revision History

IGOT65R055D2

Revision 2024-04-15, Rev. 0.1

Previous Revision

| Revision | Date       | Subjects (major changes since last revision) |
|----------|------------|----------------------------------------------|
| 0.1      | 2024-04-15 | Release of target                            |

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