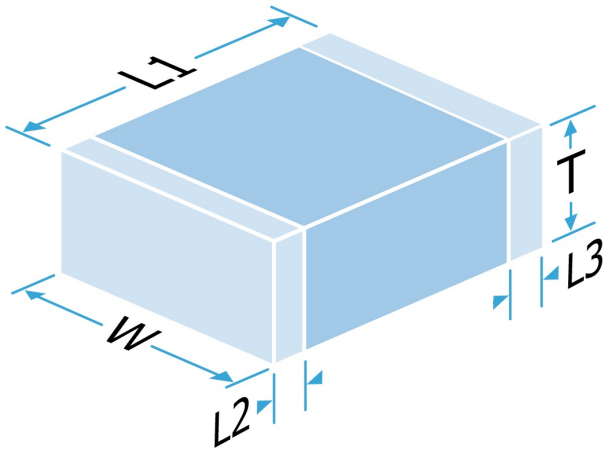
Multilayer Ceramic Chip Capacitor

Part Number: 0603J2500101GUT

Description: 0603 250Vdc 100pF ±2% C0G - Hi Q/Ultra-Low ESR (CTI ≥ 600)

Ultra stable HighQ Low ESR multi-layer ceramic capacitors offering a very stable C0G High Q material system that provides excellent low loss performance. Optimised for lowest possible ESR, the electrode system provides low metal losses, resulting in flatter performance curves and reduced losses at higher frequencies.

H17 suffix coded parts allow operation at temperatures up to 175°C. All other parts in the range are rated up to 125°C.



Mechanical Specification

Size Code	0603
Length (L1) in mm (")	1.6 ± 0.20 (0.063 ± 0.008)
Width (W) in mm (")	0.8 ± 0.20 (0.032 ± 0.008)
Thickness (T) in mm (")	0.8 Max (0.032 Max)
Minimum Termination Band (L2,L3) in mm (")	0.20 (0.008)
Maximum Termination Band (L2,L3) in mm (")	0.40 (0.016)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 4000 per reel

General Electrical Specification

Rated Voltage	250Vdc
Nominal Capacitance Value	100pF
Capacitance Tolerance	±2%
Tangent of Loss Angle (Tan δ)	≤0.0005
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	500Vdc
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G - Hi Q/Ultra-Low ESR (CTI ≥ 600)
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Tuesday, June 03, 2025
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Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	247 compliant
California Proposition 65	No exposure risk

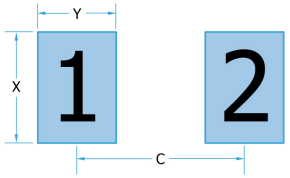
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

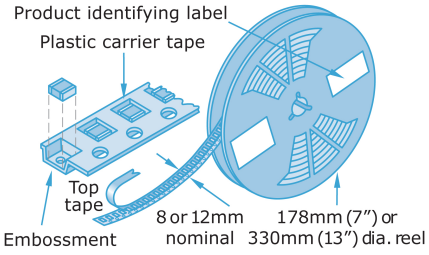
	0603	
C	1.60mm	0.063"
Y	0.85mm	0.033"
X	1.00mm	0.039"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



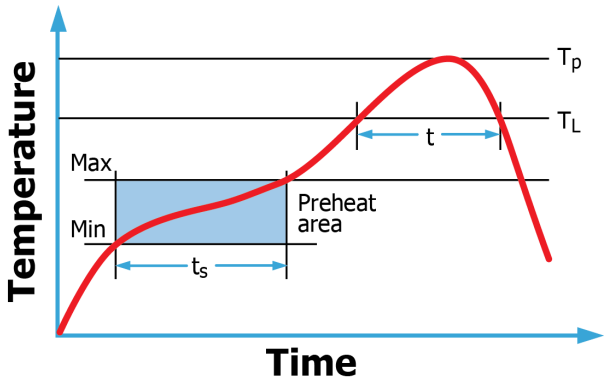
Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.



Application notes with mounting and handling guidance are available on request.

Compex DLI Johanson MFG Novacap Syfer Voltronics

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