



# PHK31NQ03LT

N-channel TrenchMOS logic level FET

Rev. 3 — 11 March 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies
- Notebook computers
- Voltage regulators

### 1.4 Quick reference data

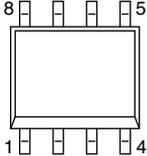
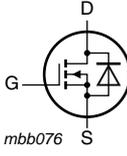
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	30.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	6.9	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	3.45	4.4	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 12\text{ V};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	7.7	-	nC

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## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT96-1 (SO8)</p>	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 3. Ordering information

Table 3. Ordering information

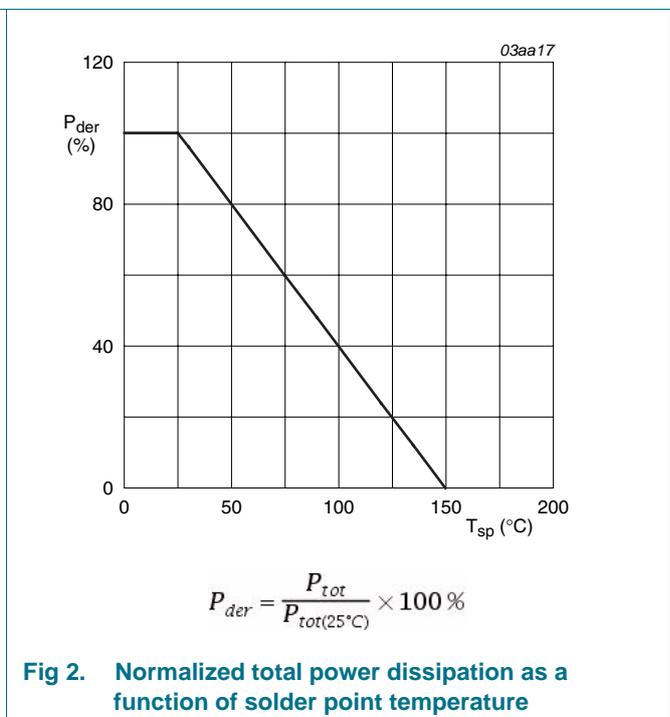
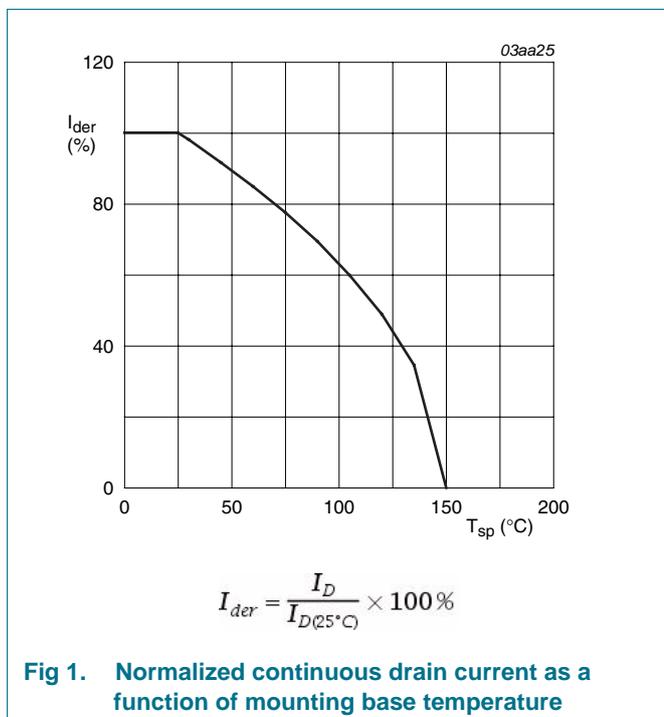
Type number	Package		
	Name	Description	Version
PHK31NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

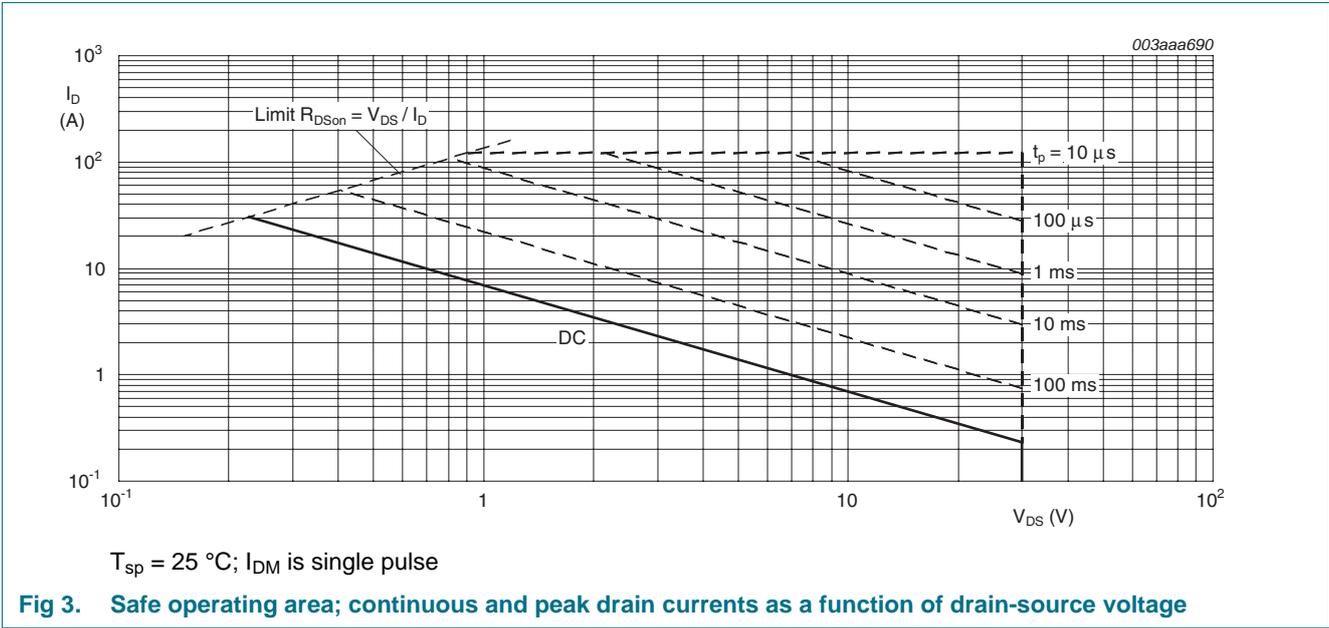
### 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	30	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C; R <sub>GS</sub> = 20 kΩ	-	30	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	T <sub>sp</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	30.4	A
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	-	17.2	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; see <a href="#">Figure 3</a>	-	121.8	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see <a href="#">Figure 2</a>	-	6.9	W
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	5.7	A
I <sub>SM</sub>	peak source current	T <sub>sp</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs	-	23.1	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 35 A; V <sub>sup</sub> ≤ 25 V; unclamped; t <sub>p</sub> = 0.16 ms; R <sub>GS</sub> = 50 Ω	-	120	mJ

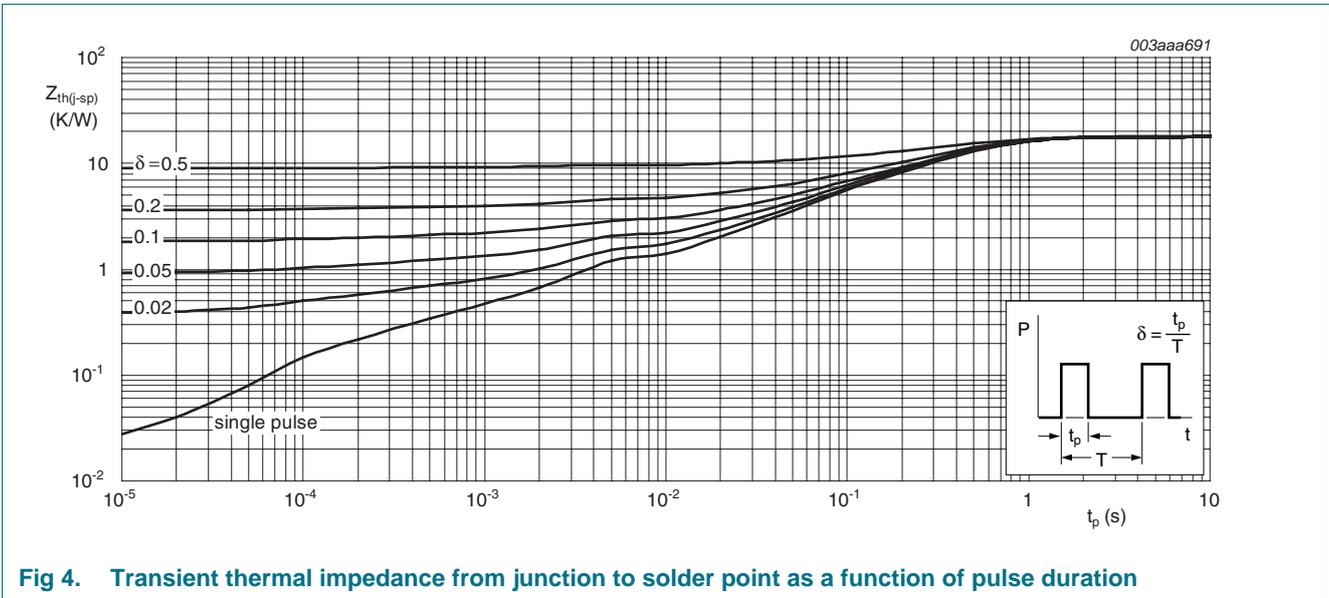




## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	18	K/W



## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	0.8	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	-	2.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu A$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	3.45	4.4	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	5.85	7.5	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	4.25	5.6	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; V_{GSS(AC)} = 150 \text{ mV}$	-	1.2	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	33	-	nC
$Q_{GS}$	gate-source charge		-	13.6	-	nC
$Q_{GS1}$	pre-threshold gate-source charge		-	6.5	-	nC
$Q_{GS2}$	post-threshold gate-source charge		-	7.1	-	nC
$Q_{GD}$	gate-drain charge		-	7.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V};$ see <a href="#">Figure 12</a>	-	2.85	-	V
$C_{iss}$	input capacitance	$V_{DS} = 0 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$	-	4900	-	pF
		$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	4235	-	pF
$C_{oss}$	output capacitance		-	840	-	pF
$C_{rss}$	reverse transfer capacitance		-	370	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega$	-	37	-	ns
$t_r$	rise time		-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	54	-	ns
$t_f$	fall time		-	26	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	0.94	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 30\text{ V}$	-	52	-	ns
$Q_r$	recovered charge	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$	-	30	-	nC

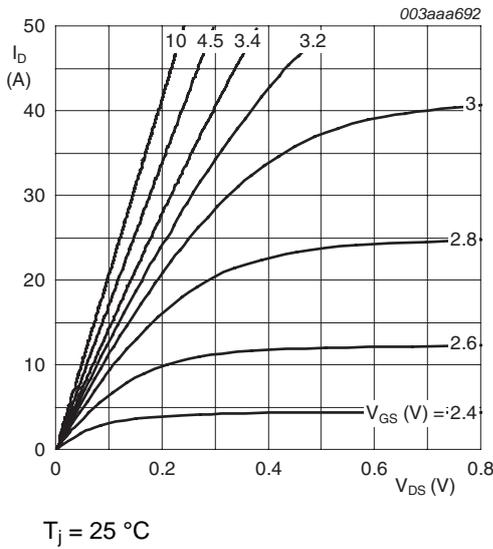


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

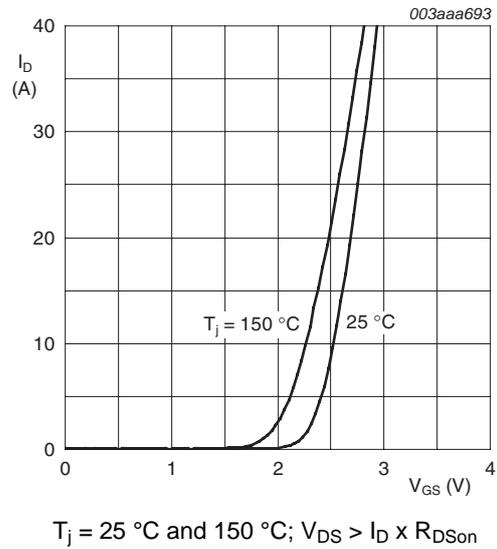


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

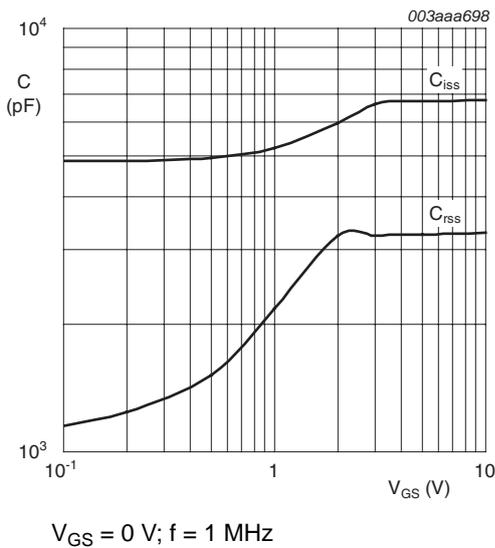


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

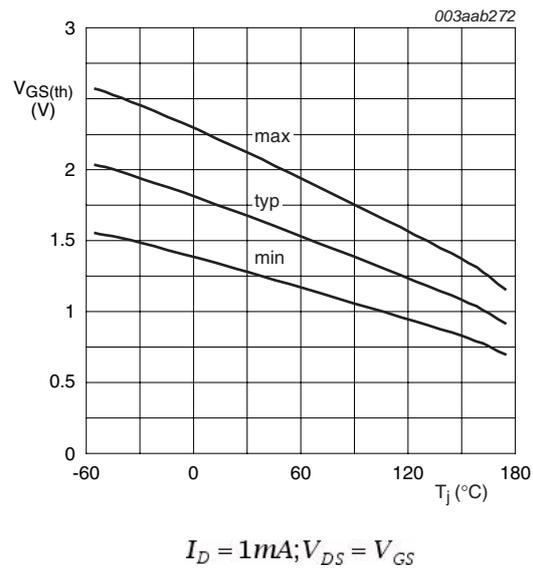
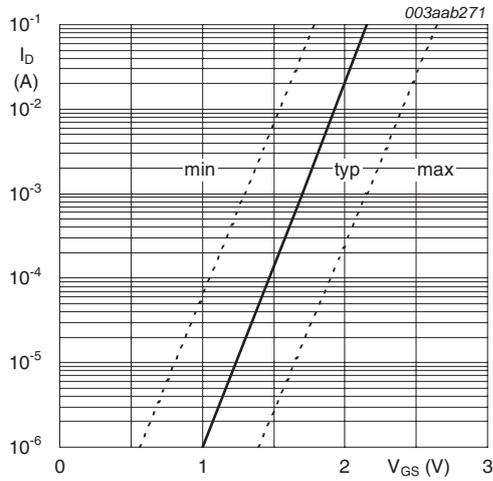
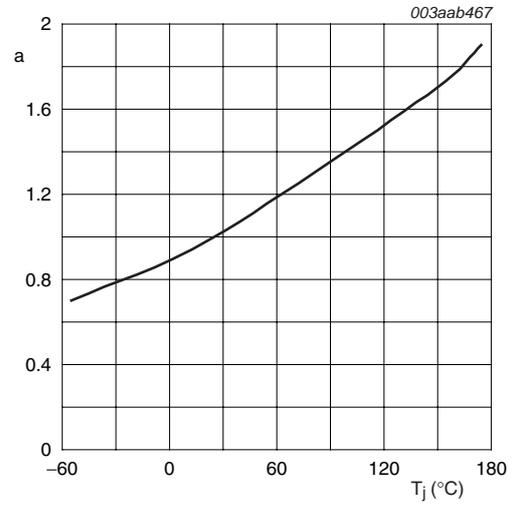


Fig 8. Gate-source threshold voltage as a function of junction temperature



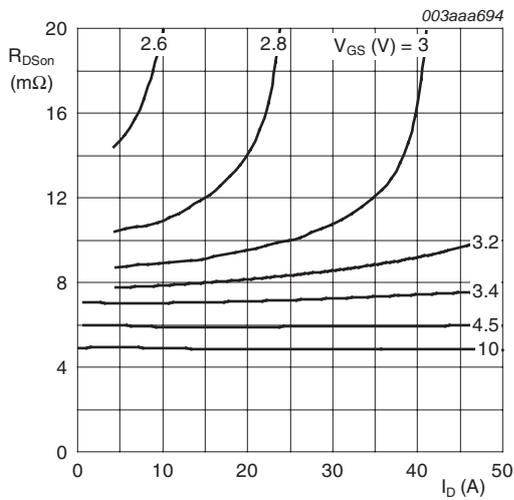
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



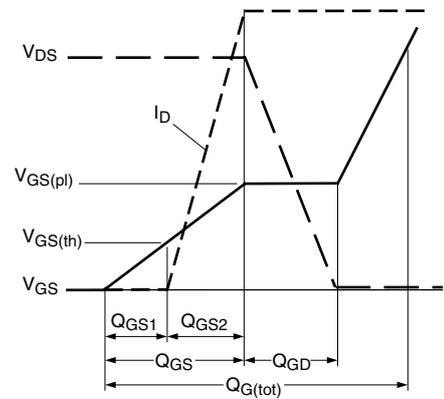
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



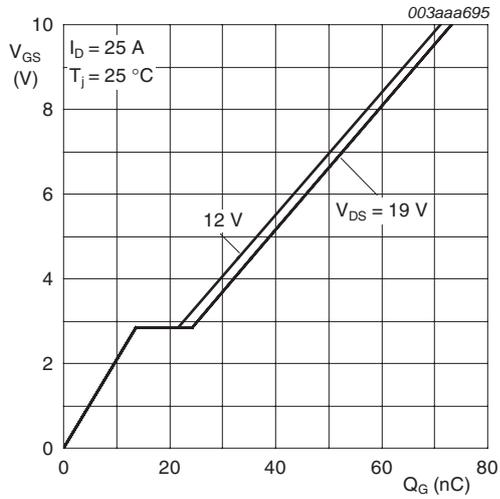
$T_j = 25^\circ\text{C}$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



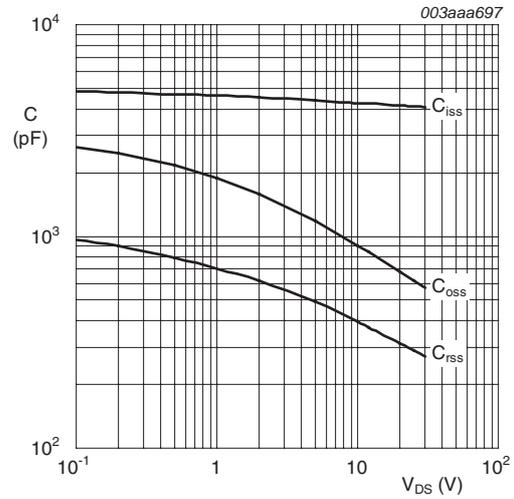
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Fig 12. Gate charge waveform definitions



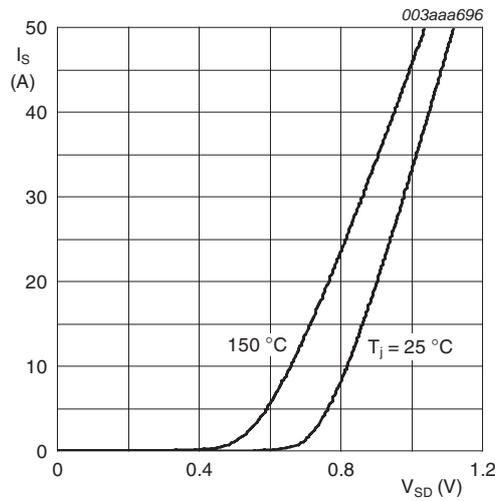
$I_D = 25 \text{ A}$ ;  $V_{DS} = 12 \text{ V}$  and  $19 \text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$T_j = 25 \text{ }^\circ\text{C}$  and  $150 \text{ }^\circ\text{C}$ ;  $V_{GS} = 0 \text{ V}$

**Fig 15. Source current as a function of source-drain voltage; typical values**

7. Package outline

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

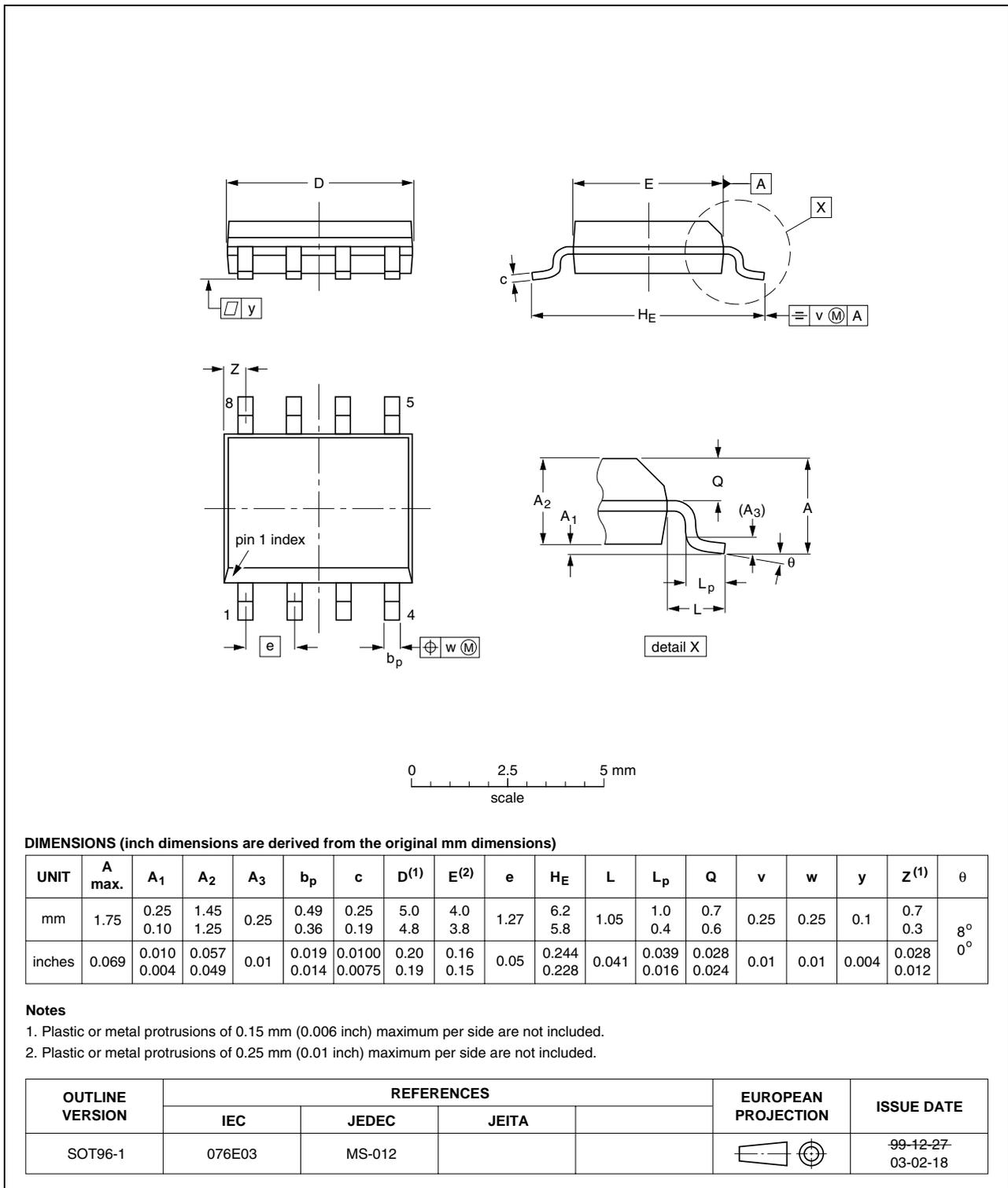


Fig 16. Package outline SOT96-1 (S08)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK31NQ03LT v.3	20110311	Product data sheet	-	PHK31NQ03LT v.2
Modifications:	• Various changes to content.			
PHK31NQ03LT v.2	20101220	Product data sheet	-	PHK31NQ03LT v.1

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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