Single LNB Supply and Control Voltage Regulators

FEATURES AND BENEFITS

- Integrated boost MOSFET, current sensing, compensation, and output LDO
- Configurable boost capacitor option:
  - □ A8300: ceramic
  - □ A8300-1: electrolytic
- Sleep mode with shutdown current < 15 µA (typ)
- Early Power Failure (EPF) warning function
- Backfeed current control
- Robust output pin voltage rating for surge and backfeed protection
- Adjustable LNB output current limit from 300 to 950 mA
  - □ Selectable overcurrent disable timer
  - □ Covers a wide array of application requirements
  - □ Minimizes component sizing to fit each application
  - □ For startup, reconfiguration, and continuous output (maximum value depends on PCB thermal design)

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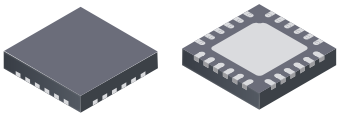
PACKAGE:



24-contact MLP/QFN with exposed thermal pad (suffix ES)
4 mm × 4 mm × 0.75 mm

DESCRIPTION

Intended for analog and digital satellite receivers, these single low noise block converter regulators (LNBR) consist of a monolithic boost converter followed by a low-drop linear regulator. They are specifically designed to provide the power and the interface signals to an LNB down converter via coaxial cable in satellite TV receiver systems.

The A8300 and A8300-1 require few external components, with the boost switch and compensation circuitry integrated inside of the devices. The 563 kHz switching frequency is chosen to minimize the size of the passive filtering components.

For DiSEqC™ communication the ICs provide an internal 22 kHz tone that is gated with a control pin, or can accept an external 22 kHz through this same pin. In addition, these devices have integrated tone detection capability for full two-way DiSEqC™ communications, as well as an integrated gate drive for the filter bypass FET.

The I²C™-compatible interface provides control capabilities for complex system requirements, as well as diagnostic capabilities for system fault reporting. A sleep pin is also available to maximize power savings and to quickly shut down the device if needed, without using I²C™ control.

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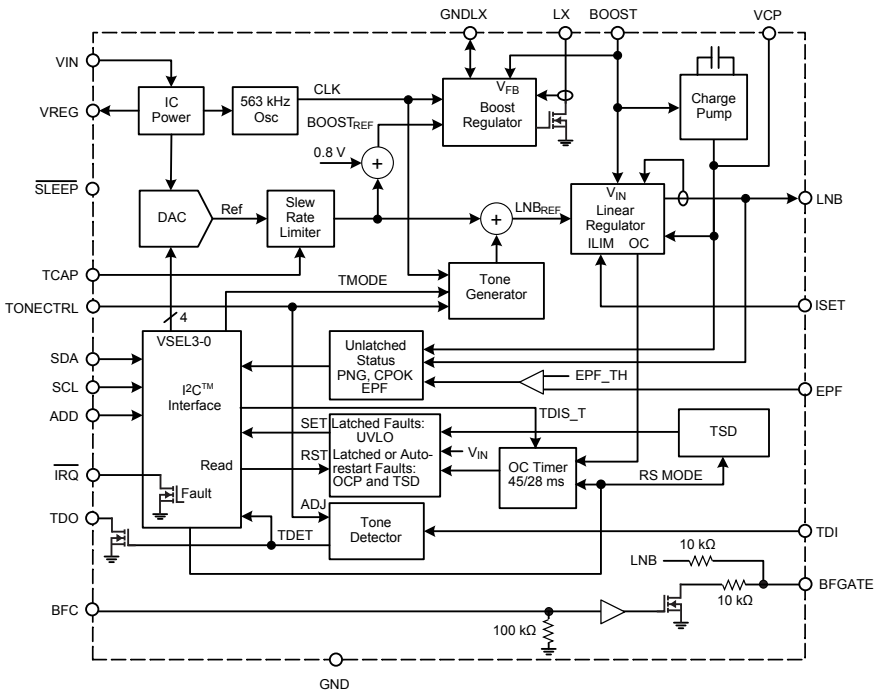
Functional Block Diagram



FEATURES AND BENEFITS (CONTINUED)

- Boost peak current limit scales with LNB current limit setting
- LNB overcurrent limit protection and TSD can be either latched or auto-restart
- Full DiSEqC™ compatibility
- Dynamic tone detect amplitude and frequency transmit/receive thresholds
- Diagnostic features: PNG, TDET, and EPF
- Extensive protection features: UVLO, TSD, CPOK, and OCP

DESCRIPTION (CONTINUED)

The devices also offer an Early Power Failure (EPF) function, which helps to verify the status of the 12 V rail as well as initiate shutdown routines.

The A8300 and A8300-1 are supplied in a 4 mm × 4 mm, 24-contact, lead (Pb) free QFN package (suffix ES) with 100% matte-tin-plated leadframe.

SELECTION GUIDE

Part Number	Boost Capacitor	Packing [1]	Package
A8300SESTR-T	Ceramic	7-inch reel, 1500 pieces/reel 12 mm carrier tape	ES package [2], QFN surface mount 4 mm × 4 mm × 0.75 mm nominal height
A8300SESTR-T-1	Electrolytic		

[1] Contact Allegro for additional packing options.
[2] Leadframe plating 100% matte tin.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Conditions	Rating	Unit
VIN Pin	V_{IN}		25	V
Output Current [1]	I_{LNB}		Internally Limited	A
BOOST and BFGATE Pins			–0.3 to 43	V
LNB Pin [2]		Surge	–1.0 to 43	V
LX Pin			–0.3 to 30	V
VCP Pin			–0.3 to 48	V
All Other Pins			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.
[2] See application schematics 3 and 4 on pages 33 and 34.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	37	°C/W

*Additional thermal information available on the Allegro website

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Table of Contents

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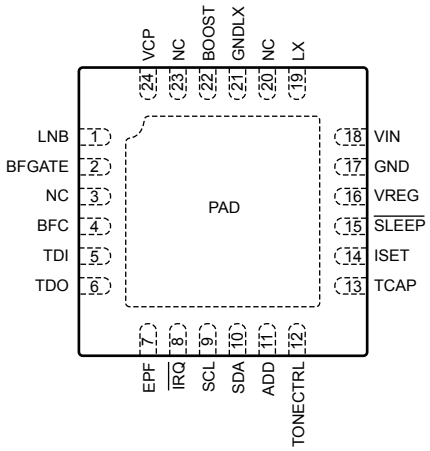
Pinout Diagram



Terminal List Table

Number	Name	Function
1	LNB	Output voltage to the LNB
2	BFGATE	Gate driver pin for the external P-channel bypass MOSFET
3, 20, 23	NC	No connection
4	BFC	Bypass FET control logic
5	TDI	Connect to output for 22 kHz tone verification function
6	TDO	Open-drain logic output that transitions low when a 22 kHz tone is present at TDI
7	EPF	Early Power Failure warning comparator input
8	$\overline{\text{IRQ}}$	Interrupt request output
9	SCL	I²C™-compatible clock input
10	SDA	I²C™-compatible data input/output
11	ADD	Address select
12	TONECTRL	Apply an external 22 kHz tone or tone on-and-off signal to enable/disable internal tone
13	TCAP	Capacitor for setting the rise and fall time of the LNB output
14	ISET	Terminal for external resistor that sets the output current limit
15	$\overline{\text{SLEEP}}$	Disables LNB output, boost, I²C™ communication, and charge pump, to reduce input quiescent current to < 15 µA
16	VREG	Analog supply
17	GND	Signal ground
18	VIN	Input supply voltage
19	LX	Internal MOSFET drain node
21	GNDLX	Boost switch ground
22	BOOST	Tracking supply voltage to linear regulator
24	VCP	Gate supply voltage
–	PAD	Exposed pad for thermal dissipation; connect to the ground plane

ELECTRICAL CHARACTERISTICS [1]: Valid at T_A = 25°C, V_{IN} = 10 to 16 V, $\overline{SLEEP}$ = 1, ● as noted [2], unless noted otherwise

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
GENERAL							
Output Voltage Accuracy	V_{LNB}	V_{IN} = 12 V, I_{LNB} = 10 mA, see table 3a for DAC settings	●	–2	–	2	%
Load Regulation	$\Delta V_{LNB(Load)}$	V_{IN} = 12 V, V_{LNB} = 13.667 V, ΔI_{LNB} = 10 to 700 mA	●	–	75	120	mV
		V_{IN} = 12 V, V_{LNB} = 19.000 V, ΔI_{LNB} = 10 to 700 mA	●	–	85	150	mV
Line Regulation	$\Delta V_{LNB(Line)}$	V_{IN} = 10 to 16 V, V_{LNB} = 13.667 V, I_{LNB} = 10 mA	●	–10	0	10	mV
		V_{IN} = 10 to 16 V, V_{LNB} = 19.000 V, I_{LNB} = 10 mA	●	–10	0	10	mV
Supply Current	$I_{IN(OFF)}$	$\overline{SLEEP}$ = 0 V, V_{IN} = 12 V, TONECTRL = 0, EPF pin open		–	–	15	µA
		ENB bit = 0, V_{IN} = 12 V		–	4.5	–	mA
	$I_{IN(ON)}$	ENB bit = 1, V_{IN} = 12 V, V_{LNB} = 19 V, I_{LOAD} = 0 mA, TONECTRL = 0		–	18	–	mA
		ENB bit = 1, V_{IN} = 12 V, V_{LNB} = 19 V, I_{LOAD} = 0 mA, TONECTRL = 1		–	44	–	mA
Boost Switch On Resistance	$R_{DS(on)}$ BOOST	I_{SW} = 450 mA		–	300	–	mΩ
Switching Frequency	f_{SW}			507	563	619	kHz
Linear Regulator Voltage Drop	ΔV_{LR}	$V_{BOOST} - V_{LNB}$, no tone signal, I_{LOAD} = 700 mA		600	800	1000	mV
TCAP Pin Current	I_{CHG}	TCAP capacitor (C12) charging		–13	–10	–7	µA
	I_{DISCHG}	TCAP capacitor (C12) discharging		7	10	13	µA
Output Voltage Rise Time [3]	$t_{r(VLNB)}$	For V_{LNB} 13→19 V; C_{12} = 100 nF, I_{LOAD} = 700 mA		–	10	–	ms
Output Voltage Pull-Down Time [3]	$t_{f(VLNB)}$	For V_{LNB} 19→13 V; C_{LOAD} = 100 µF, I_{LOAD} = 0 mA, SINK_DIS bit = 0		–	25	–	ms
Output Reverse Current	I_{RLNB}	ENB bit = 0		–	2	4	mA
		SINK_DIS bit = 1, ENB bit = 1, TONECTRL = 0		–	7	10	mA
		SINK_DIS bit = 0, ENB bit = 1, TONECTRL = 0, $\lvert V_{LNB} - V_{SEL} \rvert$ < 1.5 V		–	25	40	mA
		SINK_DIS bit = 0, ENB bit = 1, TONECTRL = 1, $\lvert V_{LNB} - V_{SEL} \rvert$ <1.5 V		–	60	85	mA
		SINK_DIS bit = 0, ENB bit = 1, TONECTRL = 0 or 1, $\lvert V_{LNB} - V_{SEL} \rvert$ > 1.5 V		–	7	10	mA

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ELECTRICAL CHARACTERISTICS [1] **(continued): Valid at T_A = 25°C, V_{IN} = 10 to 16 V, $\overline{SLEEP}$ = 1, ● as noted** [2]**, unless noted otherwise**

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
GENERAL (continued)							
Ripple and Noise on LNB Output [4]	$V_{ripn(pp)}$	20 MHz BWL; reference circuit shown in Functional Block diagram; contact Allegro for additional information on application circuit board design		–	30	–	mV_{PP}
VREG Voltage	V_{VREG}	V_{IN} = 10 V		4.97	5.25	5.53	V
ISET Voltage	V_{ISET}	V_{IN} = 10 V		3.4	3.5	3.6	V
TCAP Voltage	V_{TCAP}	V_{IN} = 10 V, V_{LNB} = 13.667 V		–	2.28	–	V
		V_{IN} = 10 V, V_{LNB} = 19.000 V		–	3.17	–	V
PROTECTION CIRCUITRY							
Output Overcurrent Limit [5]	$I_{LNB(MAX)}$	R_{SET} = 100 kΩ	●	250	300	350	mA
		R_{SET} = 37.4 kΩ	●	720	800	880	mA
Overcurrent Disable Time	t_{DIS}	TDIS_T bit = 1		–	45	–	ms
		TDIS_T bit = 0		–	28	–	ms
Overcurrent Re-Enable Time	t_{REN}	RSMODE bit = 1		–	1	–	s
Boost MOSFET Current Limit	$I_{BOOST(MAX)}$	R_{SET} = 100 kΩ		1300	1800	2300	mA
		R_{SET} = 37.4 kΩ		2800	3300	3800	mA
VIN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling		8.05	8.35	8.65	V
VIN Turn-On Threshold	$V_{IN(th)}$	V_{IN} rising		8.40	8.70	9.00	V
Undervoltage Hysteresis	$V_{UVLOHYS}$			–	350	–	mV
I²C™ Undervoltage Lockout Threshold	V_{UVLO_I2C}	V_{IN} falling		–	5.5	–	V
I²C™ Turn-On Threshold	$V_{IN(th)\_I2C}$	V_{IN} rising		–	5.7	–	V
Thermal Shutdown Threshold [3]	T_J			–	165	–	°C
Thermal Shutdown Hysteresis [3]	ΔT_J			–	20	–	°C
Power Not Good (Low)	PNG_{LOSET}	With respect to V_{LNB} setting; V_{LNB} low, PNG bit set to 1		88	91	94	%
	$PNG_{LORESET}$	With respect to V_{LNB} setting; V_{LNB} low, PNG bit reset to 0		92	95	98	%
Power Not Good (Low) Hysteresis	PNG_{LOHYS}	With respect to V_{LNB} setting		–	4	–	%
Power Not Good (High)	PNG_{HISET}	With respect to V_{LNB} setting; V_{LNB} high, PNG bit set to 1		106	109	112	%
	$PNG_{HIRESET}$	With respect to V_{LNB} setting; V_{LNB} high, PNG bit reset to 0		102	105	108	%
Power Not Good (High) Hysteresis	PNG_{HIHYS}	With respect to V_{LNB} setting		–	4	–	%

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ELECTRICAL CHARACTERISTICS [1] **(continued): Valid at T_A = 25°C, V_{IN} = 10 to 16 V, $\overline{SLEEP}$ = 1, ● as noted** [2]**, unless noted otherwise**

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
TONE							
Amplitude	$V_{TONE(PP)}$	I_{LNB} = 0 mA , C_{LNB} = 100 nF or I_{LNB} = 700 mA, C_{LNB} = 750 nF	●	500	700	900	mV_{PP}
Frequency	f_{TONE}		●	20	22	24	kHz
Duty Cycle	D_{TONE}			40	50	60	%
Rise Time	$t_{r(TONE)}$			5	10	15	µs
Fall Time	$t_{f(TONE)}$			5	10	15	µs
TONE DETECTION							
Amplitude	$V_{TDX(PP)}$	Tone transmit		500	700	900	mV_{PP}
	$V_{TDR(PP)}$	Tone receive, 22 kHz sine wave		250	650	900	mV_{PP}
Reject Amplitude, Low	$V_{TD(XMT)L}$	Tone transmit		–	–	250	mV_{PP}
	$V_{TD(RCV)L}$	Tone receive, 22 kHz sine wave		–	–	100	mV_{PP}
Reject Amplitude, High	$V_{TD(XMT)H}$	Tone transmit		–	–	1.1	V_{PP}
	$V_{TD(RCV)H}$	Tone receive, 22 kHz sine wave		–	–	1.1	V_{PP}
Frequency Capture	$f_{TD(RCV)}$	Tone receive, 650 mV_{PP} sine wave		17	22	27	kHz
	$f_{TD(XMT)}$	Tone transmit, 650 mV_{PP} sine wave		20	22	24	kHz
Frequency Reject, Low	$f_{TD(RCV)L}$	Tone receive, 650 mV_{PP} sine wave		12	14	–	kHz
	$f_{TD(XMT)L}$	Tone transmit, 650 mV_{PP} sine wave		15	17	–	kHz
Frequency Reject, High	$f_{TD(RCV)H}$	Tone receive, 650 mV_{PP} sine wave		–	34	37	kHz
	$f_{TD(XMT)H}$	Tone transmit, 650 mV_{PP} sine wave		–	30	33	kHz
Detection Delay	t_{DET}	Tone receive, 650 mV_{PP}, 22 kHz sine wave		–	1.5	3	cycle
TDI Input Impedance	Z_{TDI}			–	8.6	–	kΩ
TDO Output Voltage	$V_{TDO(L)}$	Tone present, I_{LOAD} = 3 mA		–	–	0.4	V
TDO Output Leakage	I_{TDO}	Tone absent, 0 V < V_{TDO} < 5 V		–	–	10	µA
EPF Pin Threshold	V_{EPF_TH}	V_{IN} voltage falling		–	3.325	–	V
EPF Threshold Hysteresis	$V_{EPF\_TH\_hys}$			–	175	–	mV
BFGATE/LNB Voltage	V_{BFG_ON}	BFC = high		–	50	–	%
	V_{BFG_OFF}	BFC = low		–	99	–	%
BYPASS FET CONTROL (BFC PIN)							
Logic Input	$V_{BFC(H)}$			2.0	–	–	V
	$V_{BFC(L)}$			–	–	0.8	V
Input Leakage Current	$I_{BFC(lkg)}$	V_{BFC} = 5 V		–	50	–	µA

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ELECTRICAL CHARACTERISTICS [1] **(continued): Valid at T_A = 25°C, V_{IN} = 10 to 16 V, $\overline{SLEEP}$ = 1, ● as noted** [2]**, unless noted otherwise**

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
TONE CONTROL (TONECTRL PIN)							
Logic Input	$V_{TNCTL(H)}$			2.0	–	–	V
	$V_{TNCTL(L)}$			–	–	0.8	V
Input Leakage Current	$I_{TNCTL(lkg)}$			–1	–	1	µA
SLEEP MODE CONTROL ($\overline{SLEEP}$ PIN)							
Logic Input	$V_{SLP(H)}$			2.0	–	–	V
	$V_{SLP(L)}$			–	–	0.8	V
Input Leakage Current	$I_{SLP(lkg)}$			–	50	–	µA
I²C™- COMPATIBLE INTERFACE							
Logic Input (SDA and SCL pins)	$V_{SCL(L)}$			–	–	0.8	V
	$V_{SCL(H)}$			2.0	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$			–	150	–	mV
Logic Input Current	I_{I2CI}	V_{I2CI} = 0 to 5 V		–10	<±1.0	10	µA
Logic Output Voltage (SDA and $\overline{IRQ}$ pins)	V_{SDA}, V_{IRQ}	I_{LOAD} = 3 mA		–	–	0.4	V
Logic Output Leakage Current (SDA and $\overline{IRQ}$ pins)	I_{LEAK}	$V_{I2COUT(L)}$ = 0 to 5 V		–	–	10	µA
SCL Clock Frequency	f_{CLK}			–	–	400	kHz
I²C™ ADDRESS SETTING							
ADD Pin Voltage for Address 0001 000	VADD1			0	–	0.7	V
ADD Pin Voltage for Address 0001 001	VADD2			1.3	–	1.7	V
ADD Pin Voltage for Address 0001 010	VADD3			2.3	–	2.7	V
ADD Pin Voltage for Address 0001 011	VADD4			3.0	–	5.0	V

[1] Operation at 16 V may be limited by power loss in the linear regulator.

[2] Indicates specifications for 0 ≤ T_J ≤ 125°C (min), design goal is 0 ≤ T_J ≤ 150°C.

[3] Ensured by worst case process simulations and system characterization. Not production tested.

[4] LNB output ripple and noise are dependent on component selection and PCB layout. Refer to the application schematic drawings and the PCB layout recommendations. Not production tested.

[5] Current from the LNB output may be limited by the choice of BOOST components.

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FUNCTIONAL DESCRIPTION

Boost Converter/Linear Regulator

The A8300/A8300-1 solution contains a tracking current-mode boost converter and linear regulator. The boost converter tracks the requested LNB voltage to within 800 mV, to minimize power dissipation. Under conditions where the input voltage, V_{BOOST}, is greater than the output voltage, V_{LNB}, the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the A8300/A8300-1 is not exceeded.

The boost converter operates at 563 kHz typical. Current sensing and slope compensation functions are provided internally.

The A8300/A8300-1 has internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against short circuits.

In the case that two or more set top box LNB outputs are connected together by the customer (such as with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (for example, 19 V on the output of a 13 V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the A8300/A8300-1 output will auto-recover to the programmed level.

BOOST CONVERTER OPERATION UNDER LIGHT LOAD

At extremely light load or no load, if the BOOST voltage tries to exceed the BOOST target voltage, the boost converter operates with minimum on-time. The BOOST settling voltage depends on supply voltage, boost inductance, minimum on-time, switching frequency, output power, and power loss in boost inductor, capacitor, and the A8300/A8300-1. If the BOOST voltage settles below the pulse skipping threshold (26.8 V), the boost converter continues to operate with minimum on-time. If the BOOST voltage tries to exceed 26.8 V, pulse skipping occurs and pulse skipping stops when the BOOST voltage drops to 26.5 V.

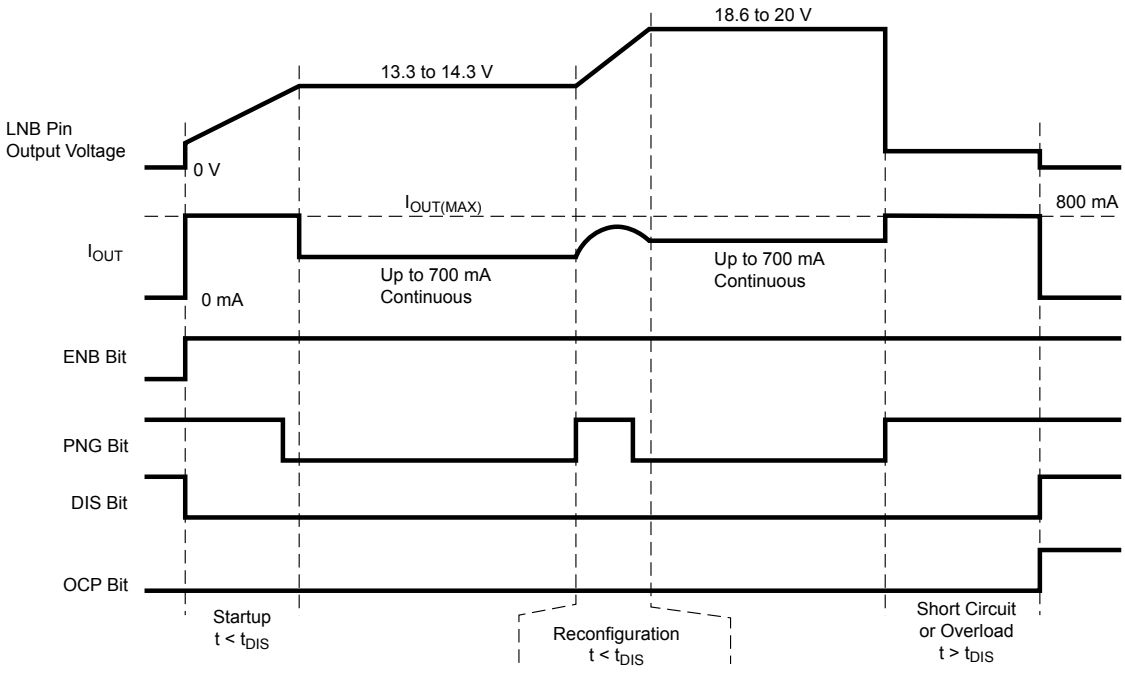

Figure 1: Startup, Reconfiguration, and Short Circuit Operation Using R_{SET} = 37.4 kΩ, and a Capacitive Load

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Under normal operating conditions the A8300/A8300-1 will not enter into pulse skipping mode. Of course A8300/A8300-1 pulse skipping operation depends on multiple factors such as: supply voltage, BFC signal, boost inductance, minimum on-time, switching frequency, and output power, as well as power losses in the boost inductor, capacitor, and the A8300/A8300-1. If it is possible that the A8300/A8300-1 might enter into pulse skipping mode, the below options can be used to avoid pulse skipping operation.

- Option 1: Shut down the A8300/A8300-1 when the device enters into pulse skipping. When V_{BOOST} exceeds a certain threshold, the EPF bit can be set using a potential divider on the BOOST pin. The host controller should read the Status register bit continuously, if EPF is set to shut down the device.
- Option 2: Add a Zener diode and resistor series circuit from the BOOST pin to GND. The Zener diode helps to clamp V_{BOOST} at a predefined level such that the deivce does not go into pulse skipping.

CHARGE PUMP

Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

LNB AND BOOST CURRENT LIMITS SETTING

The LNB output current limit, $I_{LNB(MAX)}$ can be set by connecting a resistor (RSET) from the ISET pin to GND as shown in the applications schematics. The LNB current limit can be set from 300 to 1000 mA, corresponding to an R_{SET} value of 100 to 30 kΩ, respectively. See figure 1 for a typical circuit timing example.

The LNB output current limit can be set as high as 1000 mA (by selecting an R_{SET} of 30 kΩ), but care should be taken not to exceed the thermal limit of the package, or thermal shutdown (TSD) will occur. The A8300/A8300-1 supports $I_{LNB} \geq 720$ mA continuously at 70°C ambient with $V_{IN} = 10.8$ V and $V_{LNB} = 19$ V. The typical LNB output current limit can be set according to the following equation:

$$I_{LNB(MAX)} = 29{,}925 / R_{SET} \ ,$$

where $I_{LNB(MAX)}$ is in mA and R_{SET} is in kΩ.

If the voltage at the ISET pin is 0 V (that is, shorted to GND), $I_{LNB(MAX)}$ will be clamped to a moderately high value, 1.1 A. Care should be taken to ensure that ISET is not inadvertently grounded. If no resistor is connected to the ISET pin (that is, if ISET is open-circuit), $I_{LNB(MAX)}$ will be set to approximately 0 A and the A8300/A8300-1 will not support any load (OCP will occur prematurely).

The BOOST pulse-by-pulse current limit, $I_{BOOST(MAX)}$, is automatically scaled along with the LNB output current limit. The typical BOOST current limit is set according to the following equation:

$$I_{BOOST(MAX)} = 3.0 \times I_{LNB(MAX)} + 900 \text{ (mA)} \ ,$$

where both $I_{BOOST(MAX)}$ and $I_{LNB(MAX)}$ are in mA.

Automatically scaling the BOOST current limit allows the designer to choose the lowest possible saturation current of the boost inductor, reducing its physical size and PCB area, thus minimizing cost.

Protection

The A8300/A8300-1 has a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

UNDERVOLTAGE LOCKOUT (UVLO)

The Undervoltage Lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold, $V_{IN(th)}$. The UVLO comparator incorporates enough hysteresis, $V_{UVLOHYS}$, to prevent on-off cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup.

OVERLOAD AND SHORT CIRCUIT HANDLING

The A8300/A8300-1 protects the IC against output overload and short circuit. The short circuit disable timer is controlled with the TDIS_T bit. If this bit is set to 1, the IC allows an overcurrent condition to persist up to 45 ms and if this bit is set to 0, the maximum overcurrent time allowed is 28 ms. The A8300/A8300-1 provides the option either to latch or to auto-restart on fault. If the RSMODE bit is set to 1, with an overcurrent condition that exceeds typically 45 ms (TDIS_T set to 1) or 28 ms (TDIS_T set to 0), the IC turns off output for 1 s and then auto-restarts with the previous settings. This hiccup mode continues as long as output current is greater than the OCP level. The device returns to normal operation when the fault is removed. If RSMODE is set to 0, the IC turns off after t_{DIS} time expires, and remains latched. Figures 2a and 2b explain overcurrent protection operation with RSMODE at 1 and at 0.

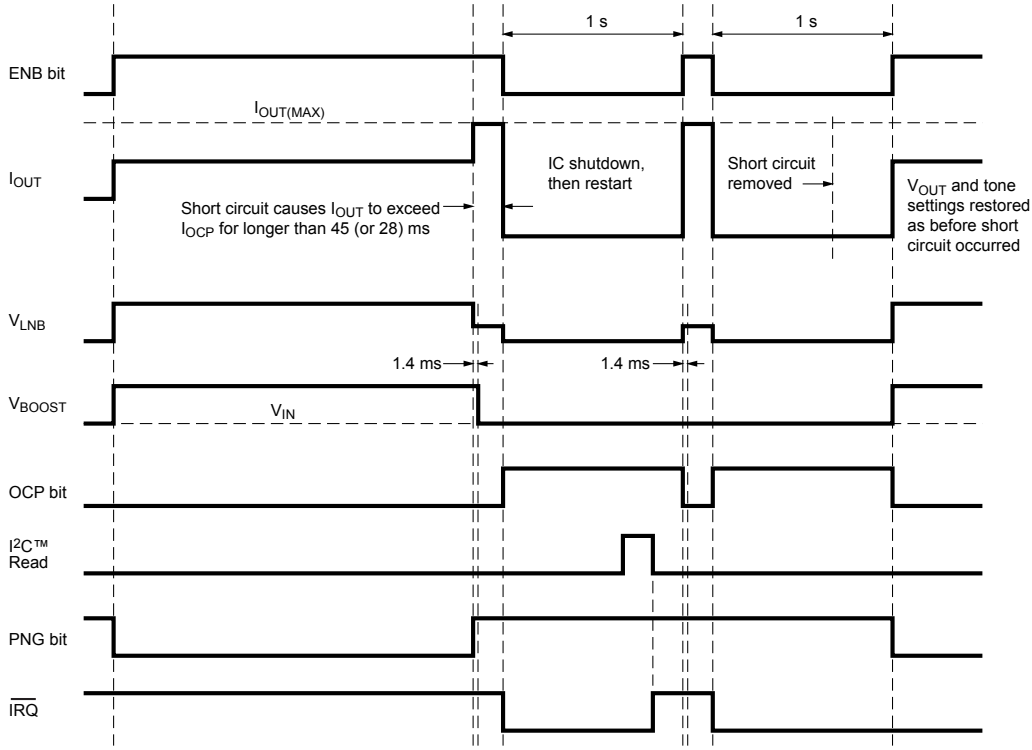

Figure 2a: IRQ and Fault Clearing in Response to Overcurrent (OCP) with auto-retry enabled (RSMODE = 1) and an OCP delay of 45 (or 28) ms (TDIS_T = 1 (or 0)). $\overline{IRQ}$ transitions to low at an OCP fault and is reset by an I²C™ Read sequence. The OCP bit clears automatically after 1 s, and the device restarts with the previous settings. This hiccup mode continues as long as the output current is greater than the OCP level. The device returns to normal operation when the fault is removed.

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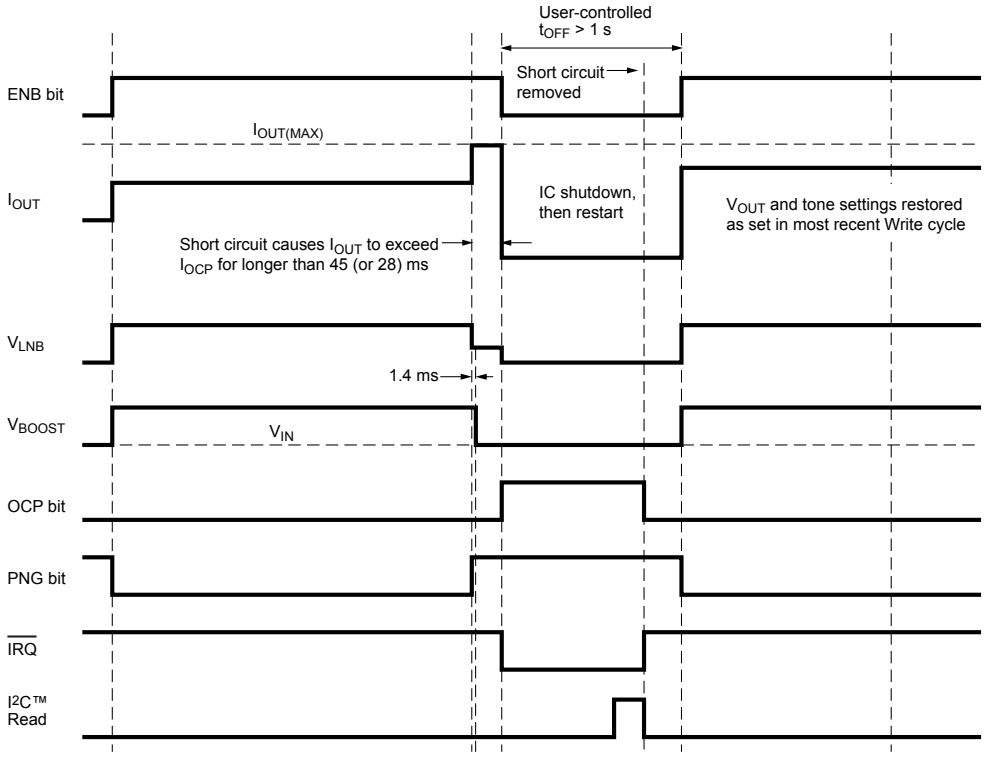

Figure 2b: IRQ and Fault Clearing in Response to Overcurrent (OCP) with latch mode (RSMODE = 0) and an OCP delay of 45 (28) ms (TDIS_T = 1(or 0)). $\overline{IRQ}$ transitions low at an overcurrent fault, and an I²C™ Read sequence clears the OCP bit and $\overline{IRQ}$. An I²C™ Write sequence is required to reenable the part. The retry wait time should be longer than 1 s, to prevent TSD.

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SLEW RATE CONTROL

During either startup, or when the output voltage at the LNB pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAP pin to GND (C12 in the applications schematics). Note that during start-up, the BOOST pin is pre-charged to the input voltage minus a diode voltage drop. As a result, the slew rate control for the BOOST pin occurs from this voltage. See Figure 3.

The value of C12 can be calculated using the following formula:

$$C_{12} = (I_{TCAP} \times 6) / SR ,$$

where SR is the required slew rate of the LNB output voltage, in V/s, and I_{TCAP} is the TCAP pin current specified in the Electrical Characteristics table. The recommended value for C_{12}, 100 nF, should provide satisfactory operation for most applications.

The minimum value of C_{12} is 10 nF. There is no theoretical maximum value of C_{12} however too large a value will probably cause the voltage transition specification to be exceeded. Tone generation is unaffected by the value of C_{12} .

PULL-DOWN RATE

In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), set the SINK_DIS bit to 0, so the output linear stage provides approximately 25 mA of pull-down capability. This ensures that the LNB output voltage is ramped from 18 to 13 V in a reasonable amount of time. When the tone is on, the output linear stage increases its pull-down capability to approximately 60 mA. This ensures that the tone signal meets all specifications, even with no load on the on the LNB output.

THERMAL SHUTDOWN (TSD)

The A8300/A8300-1 protects the IC against overheating. If junction temperature exceeds 165°C (typ), LNB output and the boost converter output are disabled until T_J cools below 145°C. The A8300/A8300-1 provides the option either to latch or to auto-restart on fault. If the RSMODE bit is set to 1, the A8300/A8300-1 IC attempts to restart at 1-second intervals, but restart is successful only with $T_J < 145°C$. This hiccup mode continues as long as $T_J > 145°C$. The device returns to normal operation when the fault is removed. If RSMODE is set to 0, the IC turns off, and remains latched. Figures 4a and 4b explain thermal shutdown protection operation with RSMODE at 1 and at 0.

OUTPUT REVERSE CURRENT CONTROL

When the SINK_DIS bit is set to 1, the maximum LNB back feed current, I_{RLNB}, is less than 10 mA. When the outputs of two LNB converters are shorted, a 10 mA back feed current will prevent loading of one converter output by another converter output.

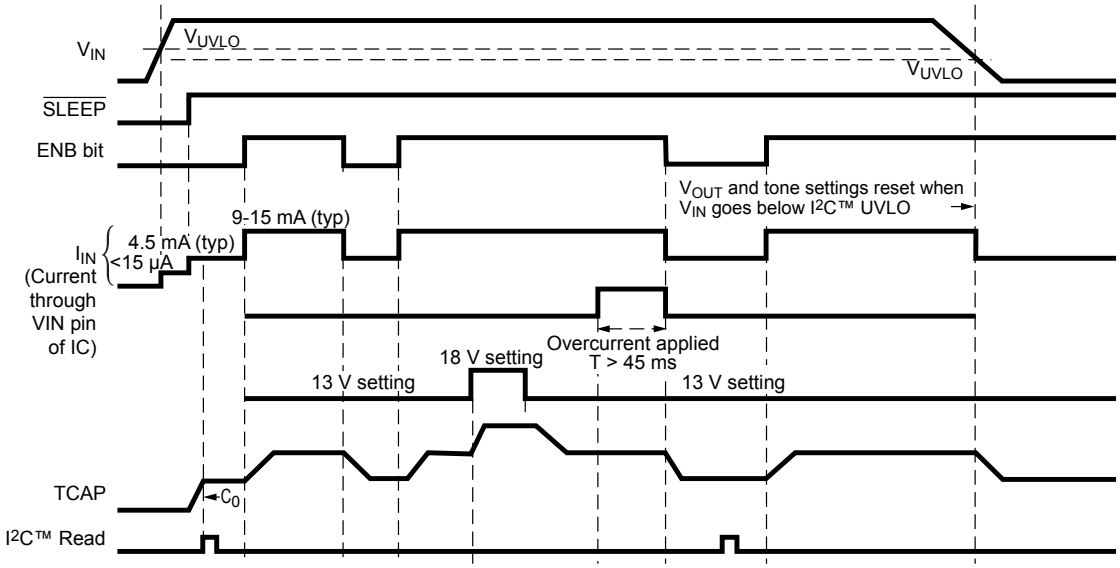

Figure 3: TCAP Timing at Startup, Transition, and OCP Faults. In latch mode (RSMODE = 0).

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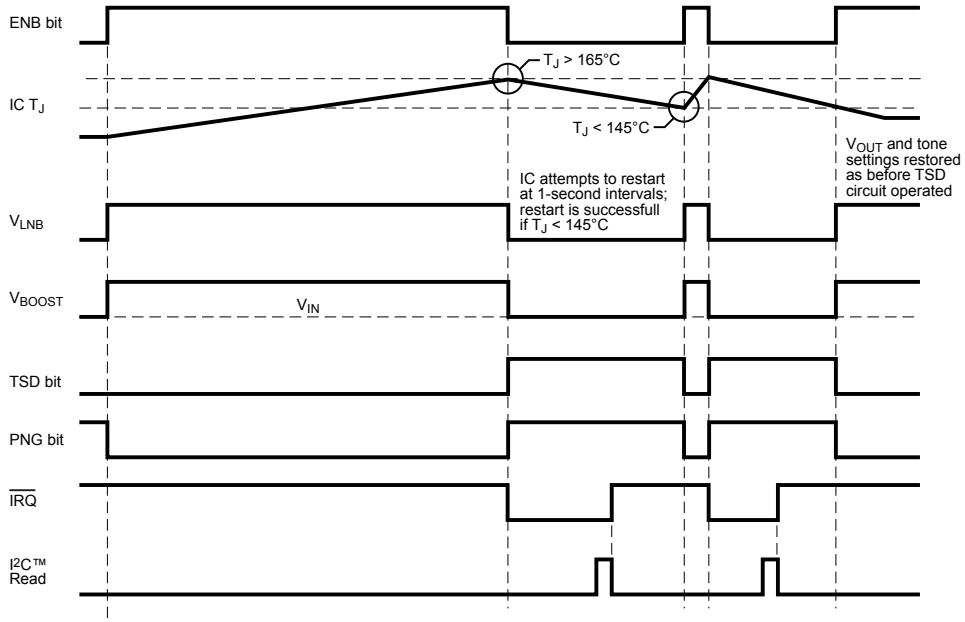

Figure 4a: IRQ and Fault Clearing in Response to Overtemperature (TSD) with auto-retry (RSMODE = 1). If for any reason the junction temperature exceeds 165°C (typ), the device LNB output and the boost converter are disabled. The IC attempts to restart at 1-second intervals, but the LNB output restarts only when T_J cools below 145°C. The $\overline{IRQ}$ pin resets on an I²C™ Read sequence, and the TSD bit resets along with an LNB output restart.

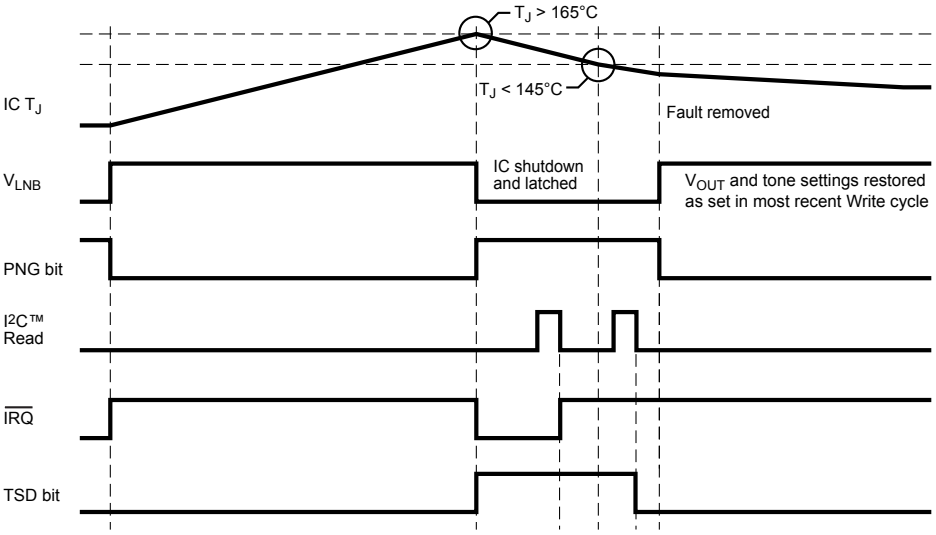

Figure 4b: IRQ and Fault Clearing in Response to Overtemperature (TSD) with latch mode (RSMODE = 0). $\overline{IRQ}$ transitions low after TSD fault, and an I²C™ Read sequence immediately resets the $\overline{IRQ}$ pin. The TSD bit is cleared by an I²C™ Read sequence only after the device has cooled to a T_J below 145°C. An I²C™ Write sequence is required to reenable the device.

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SLEEP MODE

The A8300/A8300-1 includes a sleep mode that instantly turns off the LNB output and resets the internal Control register to its default (power-on) state. When the $\overline{\text{SLEEP}}$ pin is low, the A8300/A8300-1 will draw $I_{IN(OFF)}$ less than 15 µA from the input supply.

IN-RUSH CURRENT

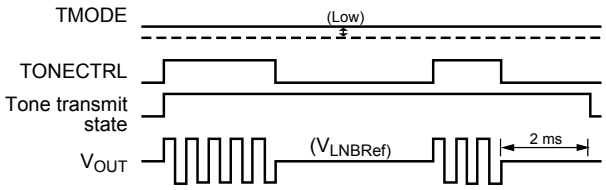
At startup or during an LNB Reconfiguration event, a transient surge current above the normal DC operating level can be provided by the A8300/A8300-1. This current increase can be as high as the set output current.

TONE GENERATION

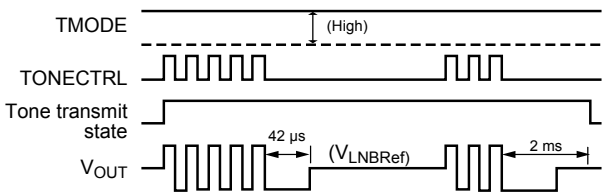
The A8300/A8300-1 offers two options for tone generation (Figure 5). The TONECTRL pin with the TMODE control bit provides the necessary control. The TMODE bit controls whether the tone source is internal or external.

When the internal source is used (TMODE bit set to 0), the tone is gated with the TONECTRL pin. The internal tone frequency is 22 kHz. Note: This tone can be generated under no-load conditions and does not require an external DiSEqC™ filter.

When the TMODE bit is set to 1, an external 22-kHz tone signal can be applied to the TONECTRL pin. This tone frequency appears at the LNB output. V_{LNB} reaches the V_{LNBref} level after TONECTRL has been low for longer than 42 µs.



Option 1. TMODE = 0, internal tone gated with TONECTRL.



Option 2. TMODE = 1, external tone as applied on TONECTRL pin
V_{OUT} reaches set level if external tone low for > 42 µs.

Figure 5: Options for Tone Generation

Tone Detection

A 22-kHz tone detector is provided in the A8300/A8300-1. The detector extracts the 22 kHz signal from the AC-coupled TDI pin and provides it as an open-drain logic output at the TDO pin. Also, when a tone is present, the TDET bit in the Status register is set to 1 and can be seen via the I²C interface. The tone detection delay is typically shorter than 1.5 cycles.

The tone detector dynamically adjusts its amplitude and frequency thresholds depending on whether the A8300/A8300-1 is transmitting or receiving a tone signal. If the A8300/A8300-1 is transmitting, the tone detect amplitude threshold is relatively high and the acceptable frequency range is tight. This ensures a high quality tone signal is always generated by the A8300/A8300-1. Conversely, if the A8300/A8300-1 is receiving, the tone detect amplitude threshold is reduced and the acceptable frequency range is increased slightly. This ensures the A8300/A8300-1 has maximum sensitivity to remotely generated tone signals that may be degraded by long lengths of coaxial cable. The Electrical Characteristics table of this datasheet documents the specifications of the tone detector and how they are adjusted by tone transmission or receiving mode.

To help in the understanding, typical tone detector operation is shown graphically in Figures 6a and 6b. The shaded areas in figure 6a indicate the accept range of the detector when

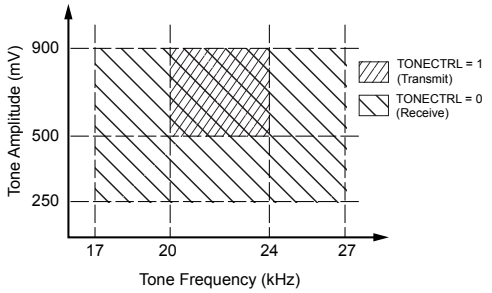


Figure 6a: Accept ranges of Tone Detection feature

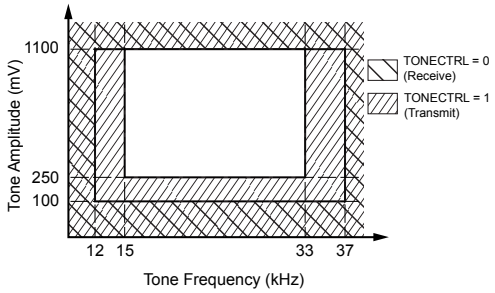


Figure 6b: Reject ranges of Tone Detection feature

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TONECTRL is a logic high (transmit) and a logic low (receive). The shaded areas in Figure 6b indicate the reject range of the detector when TONECTRL is a logic high (transmit) and a logic low (receive).

Early Power Failure Warning (EPF)

The EPF signal gives the microcontroller early warning that the supply voltage is falling below the EPF threshold value, so the microcontroller can start to shed non-critical loads (such as the LNBR) and begin its shutdown routines.

When the voltage on the EPF pin falls below V_{EPF_TH}, the EPF bit is set and IRQ is pulled low. When the EPF pin voltage goes above $V_{EPF\_TH} + V_{EPF\_TH\_hys}$, the EPF bit is reset after the programmed delay. The EPF bit resets automatically when the EPF pin voltage goes above $V_{EPF\_TH} + V_{EPF\_TH\_hys}$.

The delay between when the EPF pin voltage goes to $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ and when the EPF bit is reset, is programmed by the EPF0 and EPF1 bits. See table 3b for description.

The following examples explain selection of resistors R1 and R2 to set the EPF warning when V_{IN} falls to 10.5 V or 7 V.

Case 1: EPF warning when V_{IN} falls to 10.5 V

Assume:

Nominal Input Voltage = 12 V,

V_{EPF_TH} = 3.5 V,

$V_{EPF\_TH\_hys}$ = 0.175 V, and

EPF_TH1 (V_{IN} corresponding to setting EPF bit) = 10.5 V.

Given:

$V_{EPF\_TH} = EPF\_TH1 \times R_2 / (R_1 + R_2)$, where

$R_2/(R_1 + R_2) = 3.5/10.5 = 1/3$, then

choose R2 = 10 kΩ, R1 = 20 kΩ.

Given:

$V_{EPF\_TH} = EPF\_TH2 \times R_2 / (R_1 + R_2)$, then

EPF_TH2 (V_{IN} corresponding to resetting EPF bit) = 11 V

Case2: EPF warning when V_{IN} falls to 7 V

Assume:

Nominal Input Voltage = 12 V,

V_{EPF_TH} = 3.5 V,

$V_{EPF\_TH\_hys}$ = 0.175 V, and

EPF_TH1 (V_{IN} corresponding to setting EPF bit) = 7 V.

Given:

$V_{EPF\_TH} = EPF\_TH1 \times R_2 / (R_1 + R_2)$, where

$R_2/(R_1 + R_2) = 3.5/7 = 1/2$, then

choose R2 = 10 kΩ, R1 = 10 kΩ.

Given:

$V_{EPF\_TH} + V_{EPF\_TH\_hys} = EPF\_TH2 \times R_2 / (R_1 + R_2)$

EPF_TH2 (V_{IN} corresponding to resetting EPF bit) = 7.35 V

Cable Disconnect Test

At extremely light load or no load, the boost converter operates with minimum on-time and BOOST voltage allowed to rise up to 26.8 V before the part enters into pulse skipping operation. The BOOST settling voltage depends on supply voltage, boost inductance, minimum on-time, switching frequency, output power, and power loss in boost inductor, capacitor, and the A8300/A8300-1. This feature is used to detect a cable disconnect, with the help of the EPF bit.

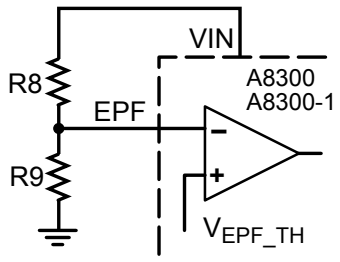

Figure 7: Example Circuit for Early Power Failure Feature

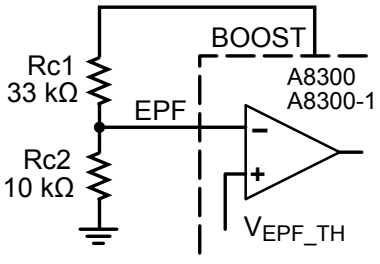

Figure 8: Optional Cable Disconnect Detection Circuit

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A simple potential divider connection on BOOST, as shown in Figure 8, is used to sense the BOOST voltage . When the voltage on EPF pin is below V_{EPF_TH}, the EPF bit is set to 1. When voltage on the EPF pin exceeds $V_{EPF\_TH} + V_{EPF\_TH\_hys}$, the EPF bit is reset to 0. The combination of Rc1 and Rc2 is selected such that, when the cable is disconnected, the voltage on the EPF pin exceeds $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ and resets the EPF bit to 0; otherwise the EPF bit is set to 1.

To enable the cable disconnect test, set the LNB output voltage to 13.333 V and read the Status register bit. If the EPF bit is reset, the cable is disconnected, otherwise the cable is connected. When the cable disconnect feature is used, the EPF pin senses the BOOST voltage, so the Early Power Failure warning (EPF) feature cannot be used.

Component Selection

BOOST INDUCTOR

The A8300/A8300-1 is designed to operate with a boost inductor value of 10 µH ±30% with a DCR less than 75 mΩ. The error amplifier loop compensation, current sense gain, and PWM slope compensation were chosen for this value of inductor. The boost inductor must be able to support the peak currents required to maintain the maximum LNB output current without saturating. Figure 9 can be used to determine the peak current in the inductor given the LNB load current. The curve labeled *Typical* uses V_{IN} = 12 V, V_{LNB} = 20 V, L = 10 µH, and f = 563 kHz, while the curve labeled *Maximum* assumes V_{IN} = 10.8 V, V_{LNB} = 21 V, L = 7 µH, and f = 506 kHz.

A8300 BOOST CERAMIC CAPACITOR

The A8300 is designed to operate with two or three, high-quality ceramic capacitors on the boost node. Allegro recommends capacitors that are rated at least 35 V, ±10%, X7R, 1210 size. Physically smaller capacitors, such as the 0603 and 0805, with lower temperature ratings, such as X5R and Z5U, should be avoided.

The nominal boost capacitance should total 14.1 to 20 µF. Allegro recommends either three 4.7 µF or two 10 µF capacitors, with the characteristics shown in table 1. Figure 10 provides typical and maximum values of rms current required for a given LNR current:

Rating	V_{IN} (V)	V_{LNB} (V)	L (µH)	f_{SW} (kHz)
Typical	12	19	10	563
Maximum	9	20	7	507

Two possible ceramic based capacitor solutions have been presented. Other capacitor combinations are certainly possible, such as a very low ESR electrolytic capacitor in parallel with several microfarads of ceramic capacitance. However, there are two critical requirements that must be satisfied: 1) the zero formed by the electrolytic capacitor and its ESR should be at least 1 decade higher than the 0 dB crossover of the boost loop (typically around 25 kHz), and 2) the ceramic capacitors must eliminate the high frequency switching spikes/edges in the boost voltage, or the LNB output noise will be too high.

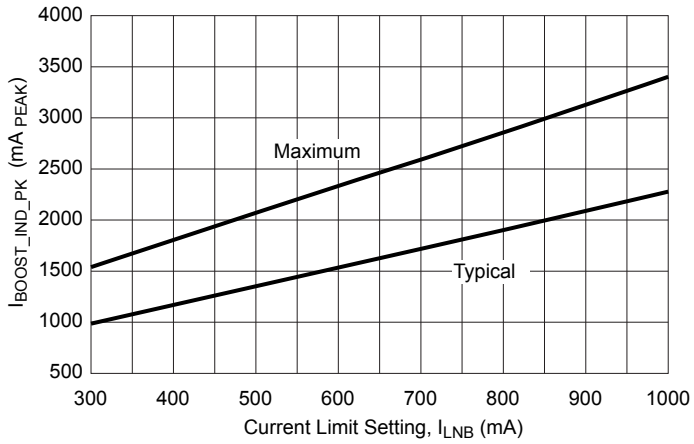

Figure 9: Boost Inductor Peak Current versus I_{LNB}

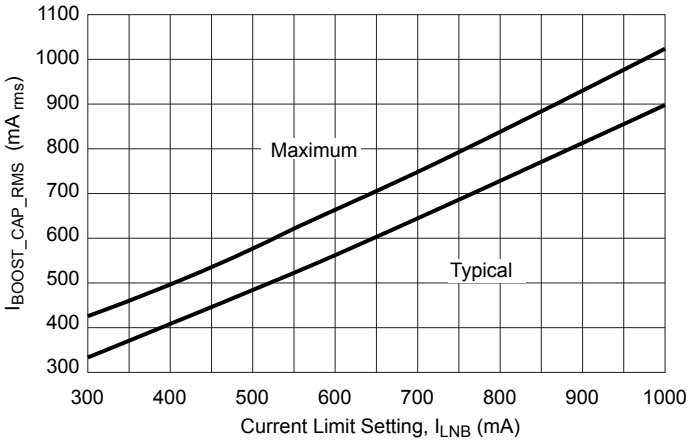

Figure 10: Boost Capacitor RMS Current versus I_{LNB}

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A8300-1 BOOST ELECTROLYTIC CAPACITOR

The A8300-1 is designed to operate with a low-ESR electrolytic boost capacitor of 100 µF ±25%. The ESR of the boost capacitor must be less than 150 mΩ or the boost converter will be unstable. General purpose electrolytic capacitors that do not specify an ESR should be avoided. Allegro recommends an electrolytic capacitor that is rated to support at least 35 V and has an rms current rating to support the maximum LNB load. Figure 10 can be used to determine the necessary rms current rating of the boost capacitor given the LNB load current.

BOOST FILTERING AND LNB NOISE

The LNB output noise depends on the amount of high-frequency noise at the BOOST pin. To minimize the high-frequency noise at the BOOST pin, the ceramic capacitors should be placed as close as possible to the BOOST pin.

SURGE COMPONENTS

The circuit shown in application Schematic 1 includes external diodes for surge protection. The Application Information section includes D2, D3, and D4 component recommendations in Table 6. This configuration and these components have successfully passed surge tests up to ±1000 V at 500 A.

To meet the increased surge requirements. “surge to failure of the TVS,” or ±4000 V, whichever occurs first. these increased surge voltages produce significantly more current in both the external circuitry and the A8300/A8300-1. Allegro surge testing has shown that the LNBTVS6-221 usually fails at approximately 43 V, so all of the LNBR output components (ceramic capacitors, diodes, and so forth) should support at least 50 V.

To protect at these higher voltage/current levels three modifications must be made:

- For increased positive surge, the shunting diode from the LNB pin to the BOOST pin (D3, 3 A/40 V) is no longer adequate to protect the body diode of the output stage. This diode must be increased to a 3 A/50 V device and be located so that it is in series with the BOOST pin as shown in application Schematics 3 and 4. In this position D3 will block surge current to the majority of the boost capacitance, but the 1 µF ceramic capacitor will still filter the high frequency switching noise.
- For increased negative surge, the relatively small clamping diode (D2) from the LNB pin to ground is no longer adequate. This diode must be increased from a 1 A / 40 V, SOD123 device to a 3 A / 50 V, SMA.
- For a DiSEqC 1.0 application, a 0.47 Ω / 1% / 0.25 W series resistor must be added as shown in the application schematics. The 0.47 Ω rating could be reduced if there is enough equivalent resistance in any series output components such as jumpers, inductors, or PCB traces. Every application will have its own surge requirements and the surge solution can be changed. However, Allegro strongly recommends incorporating a form of surge protection to prevent any pin of the A8300/A8300-1 from exceeding its Absolute Maximum voltage ratings shown in this datasheet.

Table 1a: Recommended Boost Capacitor Characteristics for A8300

Quantity of Capacitors in Parallel	Value of Each Capacitor (µF)	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size
3	4.7	±10	50	X7R	1210
2	10	±10	35	X7R	1210

Table 1b: Recommended Boost Capacitor Characteristics for A8300-1

Quantity of Capacitors in Parallel	Value of Each Capacitor (µF)	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size
1	100	±25	35	–	–

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I²C™-Compatible Interface

The I²C™ interface is used to access the internal Control and Status registers of the A8300/A8300-1. This is a serial interface that uses two lines, serial clock (SCL) and serial data (SDA), connected to a positive supply voltage via a current source or a pull-up resistor. Data is exchanged between a microcontroller (master) and the A8300/A8300-1 (slave). The master always generates the SCL signal. Either the master or the slave can generate the SDA signal. The SDA and SCL lines from the A8300/A8300-1 are open-drain signals, so multiple devices may be connected to the I²C™ bus. When the bus is free, both the SDA and the SCL lines are high.

SDA AND SCL SIGNALS

SDA can only be changed while SCL is low. SDA must be stable while SCL is high. However, an exception is made when an I²C™ Start or Stop condition is encountered. See the I²C™ Communications section for further details.

ACKNOWLEDGE (AK) BIT

The Acknowledge (AK) bit indicates a valid transmission and can be used in two ways. First, if the slave successfully receives eight bits of either an address or control data, it pulls the SDA line low (AK set to 0) for the ninth SCL pulse to signal a valid transmission to the master. Second, if the master successfully receives eight bits of status data from the A8300/A8300-1, it pulls the SDA line low for the ninth SCL pulse to signal a valid transmission to the slave. The recipient (either the master or the slave) should set the AK bit high (AK set to 1, also referred to as NAK) for the ninth SCL pulse if eight bits of data were not received successfully.

ACKNOWLEDGE BIT DURING A WRITE SEQUENCE

When the master sends control data (writes) to the A8300/A8300-1 there are three cases where AK bits are sent by the A8300/A8300-1. First, the A8300/A8300-1 uses the AK bit to indicate reception of a valid seven-bit chip address plus a Read/Write bit (with R/W set to 0 for a Write). Second, the A8300/A8300-1 uses the AK bit to indicate reception of a valid eight-bit Control register address. Third, the A8300/A8300-1 uses the AK bit to indicate reception of eight bits of control data. This protocol is shown in Figure 11a.

ACKNOWLEDGE BIT DURING A READ SEQUENCE

When the master reads status data from the A8300/A8300-1 there are four cases where AK bits are sent: three are sent by the A8300/A8300-1 and one is sent by the master. First, the A8300/A8300-1 uses the AK bit to indicate reception of a valid seven-bit chip address plus a Read/Write bit (with R/W set to 0 for a Write). Second, the A8300/A8300-1 uses the AK bit to indicate reception of a valid eight-bit Status register address. Third, the A8300/A8300-1 uses the AK bit to indicate reception of a valid seven-bit chip address plus a Read/Write bit (with R/W set to 1 for a Read). Finally, the master uses the AK bit to indicate receiving eight bits of status data from the A8300/A8300-1. This protocol is shown in Figure 11b.

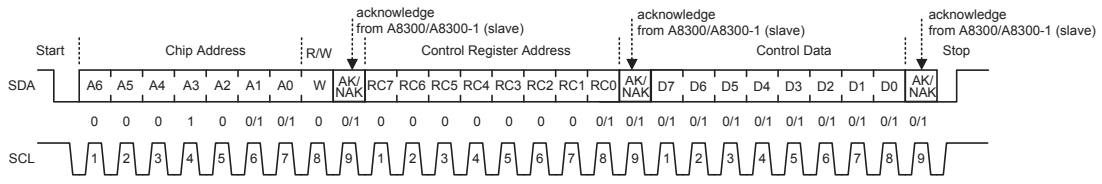

Figure 11a: I²C™ Interface Write to Control Registers Sequence

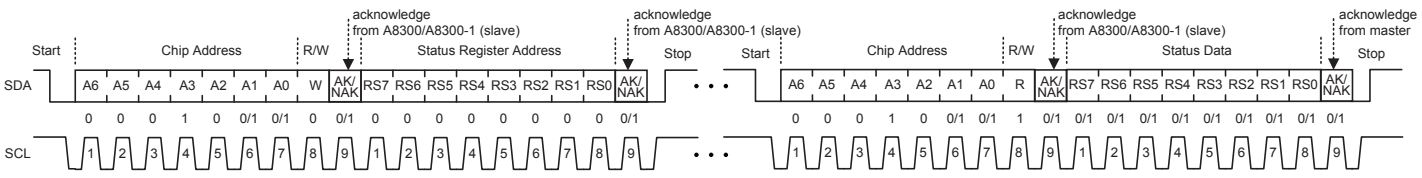

Figure 11b. I²C™ Interface Read from Status Register Sequence

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I²C™ Communications

I²C™ START AND STOP CONDITIONS

The I²C™ Start condition is defined by a negative edge on the SDA line while SCL is high. Conversely, the Stop condition is defined by a positive edge on the SDA line while SCL is high. The Start and Stop conditions are shown in Figures 11a and 11b. It is possible for a Start or Stop condition to occur at any time during a data transfer. If either a Start or Stop condition is encountered during a data transfer, the A8300/A8300-1 will respond by resetting the data transfer sequence.

I²C™ WRITE SEQUENCE DESCRIPTION

Writing to the A8300/A8300-1 Control register requires transmission of a total of 27 bits: three 8-bit bytes of data plus an AK bit after each byte. The Write sequence to the A8300/A8300-1 Control registers is shown in figure 11a. Writing to the A8300/A8300-1 Control registers requires: an I²C™ Start condition, a chip address with the R/W bit set to 0, the Control register address, the control data, and an I²C™ Stop condition as follows:

- The Chip Address cycle consists of a total of nine bits: seven bits of chip address (A6 to A0) plus one R/W bit (set to 0 to indicate a Write) from the master, followed by an AK bit (set to 0 to indicate reception of a valid chip address) from the slave. The cycle begins with a Start condition. The chip address must be transmitted MSB (A6) first. The first five bits of the A8300/A8300-1 chip address (A6 to A2) are fixed as 00010. The remaining two bits (A1 and A0) are used to select one of four possible A8300/A8300-1 chip addresses. The DC voltage on the ADD pin programs the chip address. See the Electrical Characteristics table for the ADD pin voltages and the corresponding chip addresses.
- The Control Register Address cycle consists of a total of nine bits: eight bits of Control register address (RC7 to RC0) from the master followed by an AK bit (set to 0 to indicate reception of a valid register address) from the slave. The Control register address must be transmitted MSB (RC7) first. The A8300/A8300-1 has two Control registers, with register addresses of 0000 0000 and 0000 0001.
- The Control Data cycle consists of a total of nine bits: eight bits of control data (D7 to D0) from the master, followed by an AK bit (set to 0 to indicate reception of eight valid bits) from the slave. The control data must be transmitted MSB (D7) first. The Control registers bits are identified in the Control Registers section of this datasheet. The cycle concludes with a Stop condition.

I²C™ READ SEQUENCE DESCRIPTION

Reading from the A8300/A8300-1 Status register requires transmission of a total of 36 bits: four 8-bit bytes of data, plus an AK bit after each byte. The Read sequence from the A8300/A8300-1 Status register is shown in figure 11b. Reading the A8300/A8300-1 Status register requires: an I²C™ Start condition, a chip address with the R/W bit set to 0, the Status register address, an I²C™ Stop condition, an I²C™ Start condition, a repeat of the chip address with the R/W bit set to 1, the status data, and an I²C™ Stop condition, as follows:

- The Chip Address cycle is identical to the Chip Address cycle previously described for the Write sequence.
- The Status Register Address cycle consists of a total of nine bits: eight bits of Status register address (RS7 to RS0) from the master, followed by an AK bit from the slave. The Status register address must be transmitted MSB (RS7) first. The A8300/A8300-1 has only one Status register, so the Status register address is fixed at 0000 0000. The cycle concludes with a Stop condition.
- The Repeat Chip Address cycle is identical to the Chip Address cycle previously described for the Write sequence.
- The Status Data cycle consists of a total of nine bits: eight bits of status data (RD7 to RD0) from the slave, followed by an AK bit from the master. The status data is transmitted MSB (RD7) first. The Status register bits are identified in the Status Register section of this datasheet. The cycle concludes with a Stop condition.

Interrupt Request ($\overline{\text{IRQ}}$) Pin

The A8300/A8300-1 provides an interrupt request pin, $\overline{\text{IRQ}}$, which is an open-drain, active low output. This output may be connected to a common IRQ line with a suitable external pull-up resistor and can be used with other I²C™ compatible devices to request attention from the master controller.

The $\overline{\text{IRQ}}$ output becomes active (logic low) when the A8300/A8300-1 recognizes a fault condition. The fault conditions that will force $\overline{\text{IRQ}}$ active include Early Power Failure (EPF), undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal shutdown (TSD). The UVLO, OCP (RSMODE bit set to 0), and TSD (RSMODE bit set to 0) faults are latched in the Status register and are not unlatched until the A8300/A8300-1 Status register is successfully transmitted to the master controller (an AK bit must be received from the master). See the description in the Status Register section and Figure 12 for further details.

When the master device receives an interrupt, it should address all slaves connected to the interrupt line in sequence and read the Status register of each to determine which device is requesting attention.

The LNB output disable (DIS bit set to 1) and Power Not Good (PNG bit set to 1) conditions do not cause an interrupt. and are not latched in the Status register.

Figures 13, 14, 15, and 16 show the fault handling timing for UVLO in various conditions: startup and shutdown, and relative V_{REF}, V_{IN}, and EPF conditions.

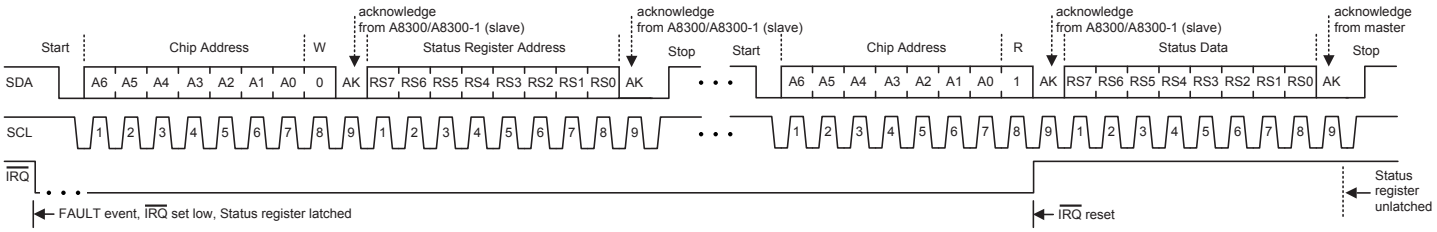

Figure 12: I²C™ Interface Read from Status Register Sequence.
The $\overline{\text{IRQ}}$ pin is reset to high when the A8300/A8300-1 acknowledges it is being read.
The Status register is unlatched when the master acknowledges the status data from the A8300/A8300-1.

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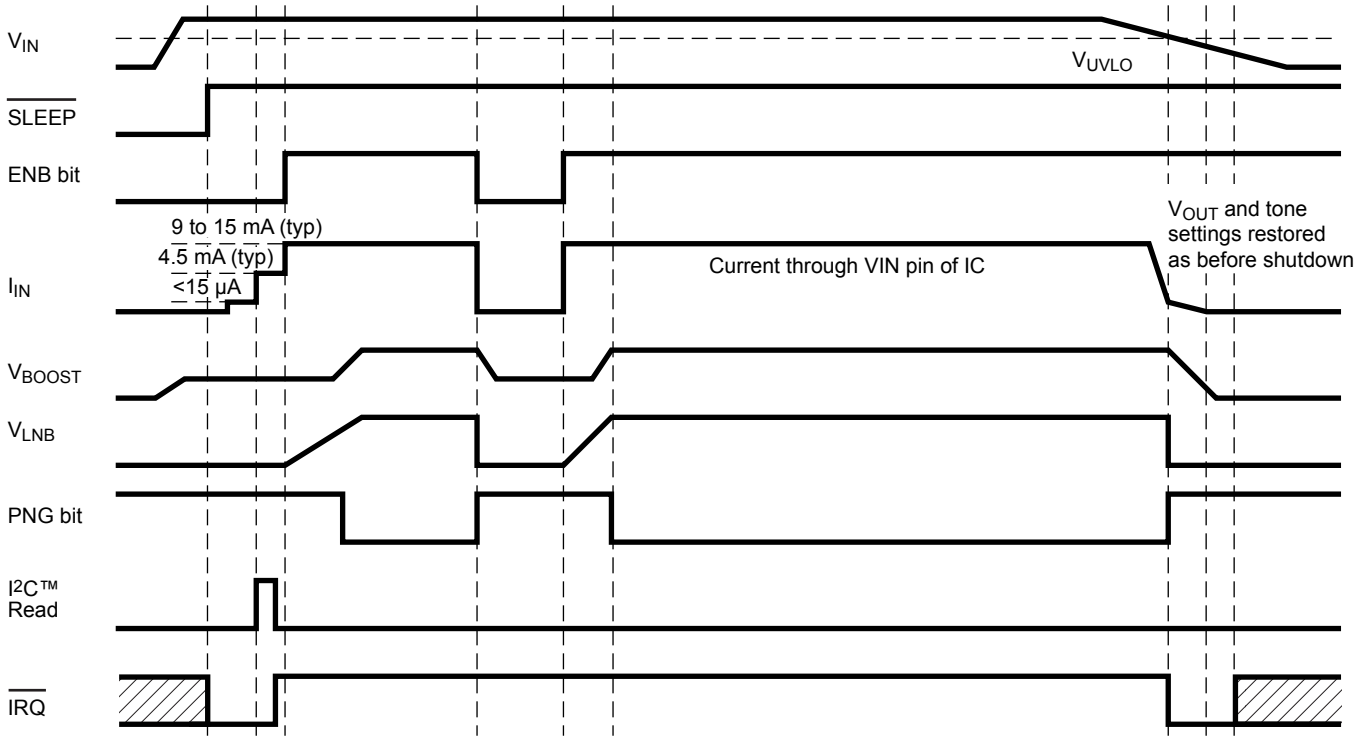

Figure 13: Startup and Shutdown Cases. IRQ and Fault Clearing in Response to Undervoltage at VIN (UVLO).
If $\overline{IRQ}$ transitions low because of a latched fault, the LNB output does not respond to the ENB bit.
An I²C™ Read sequence is required to clear any latched fault and reset the $\overline{IRQ}$ to logic high.
An I²C™ Read is required after a UVLO fault.

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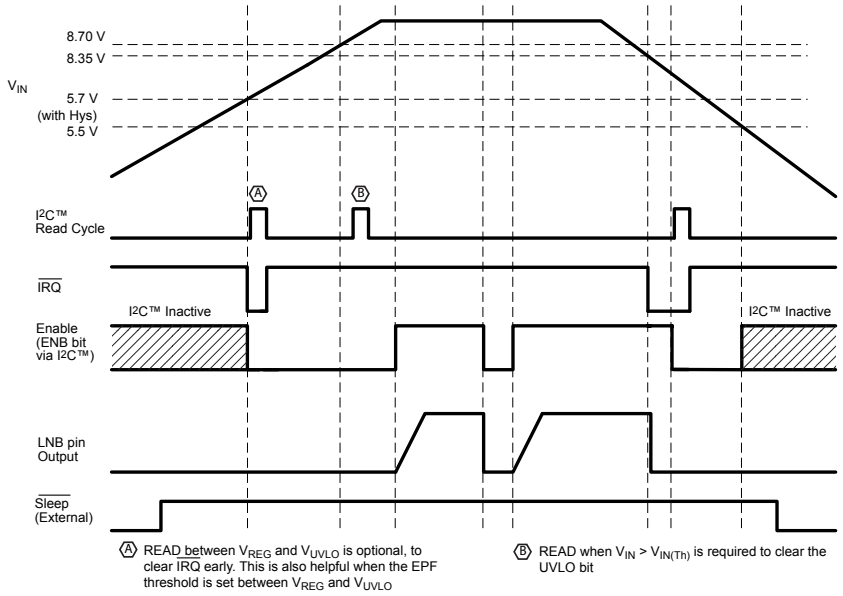

Figure 14a: I²C™ and $\overline{IRQ}$ Operate Down to $V_{IN} > V_{REG}$ (V_{REG} is 5.25 V typical), LNB and BOOST Operate from $V_{IN(th)}$. When V_{IN} exceeds V_{REG} (5.25 V typical), $\overline{IRQ}$ transitions low because of the UVLO fault, and an I²C™ Read sequence will clear the $\overline{IRQ}$ fault. While powering down, when V_{IN} falls below V_{UVLO}, $\overline{IRQ}$ becomes low, LNB and BOOST turn off, and I²C™ becomes inactive when V_{IN} falls below V_{REG}.

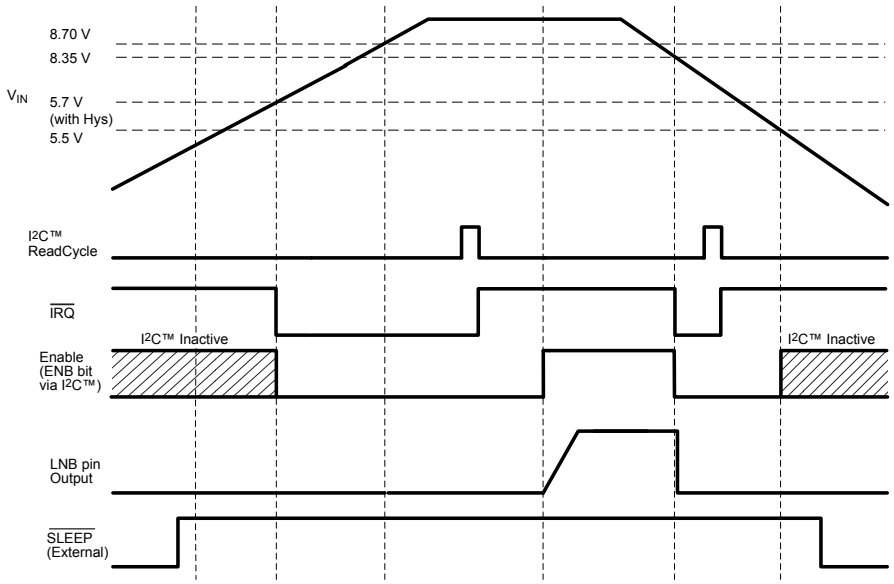

Figure 14b: $\overline{IRQ}$ is Cleared when V_{IN} is Already Above $V_{IN(th)}$.
As the ENB bit is already set high, LNB starts rising immediately after an I²C™ Read sequence.

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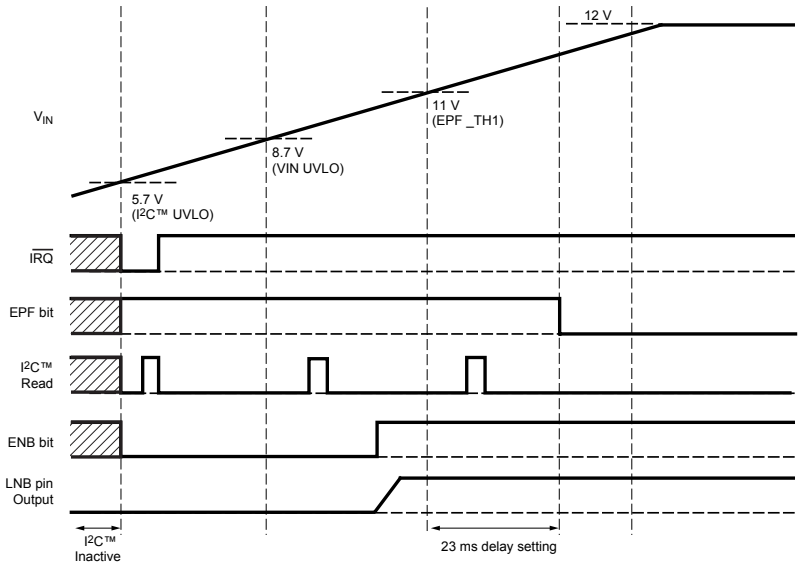


Figure 15a: EPF Pin Threshold Greater than V_{UVLO}.

When V_{IN} is rising, $\overline{IRQ}$ transitions low immediately after V_{IN} goes above V_{REG} (typical), and $\overline{IRQ}$ is cleared immediately by an I²C™ Read sequence. After V_{IN} goes above $V_{IN(th)}$ and is followed by an I²C™ Read sequence, the UVLO bit is cleared and the LNB voltage goes up. After V_{IN} goes above EPF_TH1, the EPF bit is cleared, after the delay specified by the EPF0 and EPF1 bits.

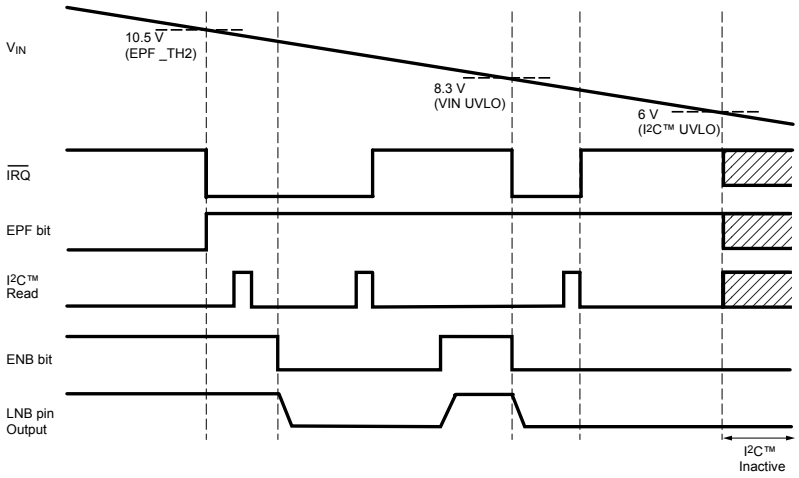


Figure 15b: EPF pin threshold greater than V_{UVLO}.

When V_{IN} falls below EPF_TH2, $\overline{IRQ}$ transitions low and the EPF bit is set high. The I²C™ Read sequence releases $\overline{IRQ}$. When V_{IN} falls below V_{UVLO}, $\overline{IRQ}$ transitions low, LNB voltage goes down, and once again the I²C™ Read sequence clears $\overline{IRQ}$.

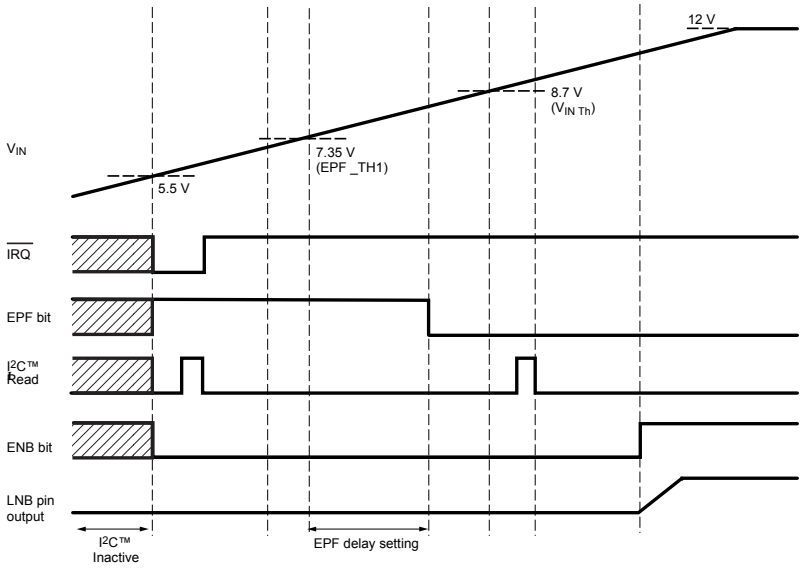


Figure 16a: EPF pin threshold greater than V_{REG} and less than V_{UVLO}.
When V_{IN} is rising, $\overline{IRQ}$ transitions low immediately after V_{IN} goes above V_{REG}, and $\overline{IRQ}$ is cleared immediately by an I²C™ Read sequence. After V_{IN} goes above EPF_TH1, the EPF bit is cleared after the delay specified by the EPF0 and EPF1 bits. When V_{IN} goes above $V_{IN(th)}$ and is followed by an I²C™ Read sequence, the UVLO bit is cleared and LNB voltage goes up.

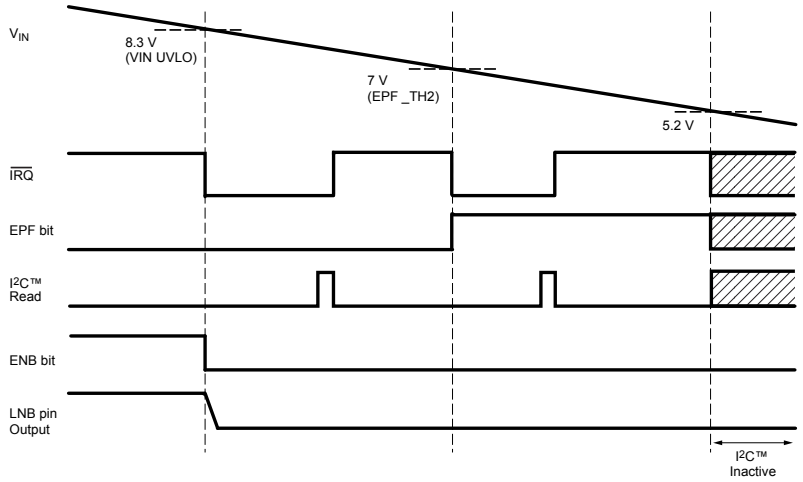
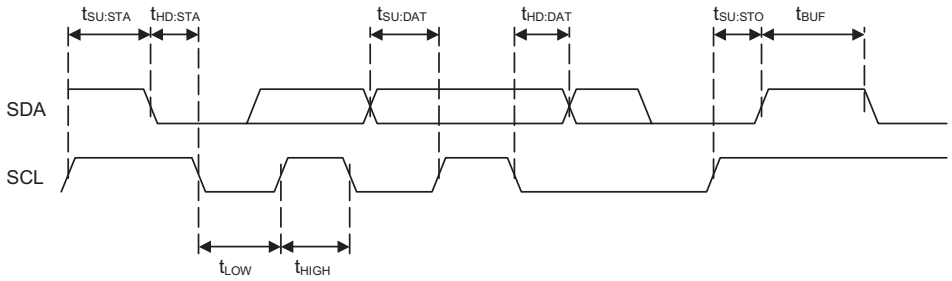


Figure 16b. EPF pin threshold greater than V_{REG} and less than V_{UVLO}.
When V_{IN} falls below V_{UVLO}, $\overline{IRQ}$ transitions low and an I²C™ Read sequence releases $\overline{IRQ}$. When V_{IN} falls below EPF_TH , $\overline{IRQ}$ will not go low.

I²C™-Compatible Interface Timing Diagram



I²C™-Compatible Timing Requirements

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Bus Free Time Between Stop/Start	t_{BUF}	1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$	0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$	0.6	–	–	µs
SCL Low Time	t_{LOW}	1.3	–	–	µs
SCL High Time	t_{HIGH}	0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$	100	–	–	ns
Data Hold Time*	$t_{HD:DAT}$	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$	0.6	–	–	µs
Output Fall Time ($V_{fI2COut(H)}$ to $V_{fI2COut(L)}$)	$t_{fI2COut}$	–	–	250	ns

*For $t_{HD:DAT}$(min), the master device must provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the SCL signal falling edge. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

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Control Registers (I²C™-Compatible Write Register)

All main functions of the A8300/A8300-1 are controlled through the I²C™ compatible interface via the 8-bit Control register. Tables 2a and 2b show the functionality and bit definitions of the Control register. At power-up, the Control register is initialized to all 0s. The LNB output will be programmed according the status of the VSEL3, VSEL2, VSEL1, and VSEL0 bits in the I²C™ Control register 0 as outlined in table 3a.

Table 2a: Control Register Definition
Control (Write) Register Address [RC7:RC0] = 0000 0000

Bit	Name	Function	Description
0	VSEL0	LNB output voltage control (see table 3a for available output voltage selections)	The available voltages provide levels for all the common standards plus the ability to add line compensation; VSEL0 is the LSB and VSEL3 is the MSB to the internal DAC
1	VSEL1		
2	VSEL2		
3	VSEL3		
4	ENB	Turns the LNB output on or off	0: Disable LNB output 1: Enable LNB output
5	TMODE	Controls tone mode	0: Internal tone, gated with TONECTRL pin 1: External 22 kHz logic pulse, on TONECTRL pin
6	TDIS_T	Controls overcurrent disable delay	1: Set overcurrent disable timeout to 45 ms 0: Set overcurrent disable timeout to 28 ms
7	RSMODE	Fault restart mode	0: Latch mode. IC latches after TDIS period on OCP or TSD; user enable required to restart 1: Auto restart mode if OCP or TSD cleared

Table 2b: Control Register Definition
Control (Write) Register Address [RC7:RC0] = 0000 0001

Bit	Name	Function	Description
0	EPF0	When V_{IN} is rising, these two bits determine the EPF bit setting delay. (See table 3b for EPF bit delay setting options.)	
1	EPF1		
2	SINK_DIS		0: Maximum Output Reverse Current, I_{RLNB}, is 85 mA 1: Maximum Output Reverse Current, I_{RLNB}, is 10 mA
3	–	Unused	–
4	–	Unused	–
5	–	Unused	–
6	–	Unused	–
7	–	Unused	–

Table 3a: Output Voltage Amplitude Selection

VSEL3	VSEL2	VSEL1	VSEL0	LNB (V)
0	0	0	0	11.000
0	0	1	0	13.333
0	0	1	1	13.667
0	1	0	1	14.333
0	1	1	1	15.667
1	0	1	1	18.667
1	1	0	0	19.000
1	1	0	1	19.333
1	1	1	0	19.667
1	1	1	1	20.000

Table 3b: EPF Delay Selection

EPF0	EPF1	Delay (ms)
0	0	0
0	1	11.5
1	0	46
1	1	92

Status Register (I²C™-Compatible Read Register)

The Status register bits are described in Tables 4 and 5. The main fault conditions: Early Power Failure (EPF), undervoltage (UVLO), overcurrent (OCP), and thermal shutdown (TSD) are all indicated by setting the relevant bits in the Status register. For these fault cases (for OCP and TSD, only if the RSMODE bit is set to 0), after the bit is set, it remains latched until the I²C™ master has successfully read the A8300/A8300-1, assuming the fault has been resolved.

The undervoltage lockout (UVLO) bit indicates either V_{IN} is below V_{UVLO}, or V_{REG} is out of regulation. UVLO disables the LNB output and forces $\overline{IRQ}$ low. UVLO is a latched fault, and can only be cleared by performing an I²C™ Read sequence.

The Disable bit (DIS) indicates the status of the LNB output. The DIS bit is set when either a fault occurs (UVLO, OCP, TSD, or CPOK) or when the LNB output is turned off using the Enable bit (ENB) via the I²C™ interface. The DIS bit is latched and is only reset when there are no faults and the A8300/A8300-1 output is turned back on using the Enable (ENB) bit via the I²C™ interface.

The Power Not Good (PNG), Charge Pump OK (CPOK), and Tone Detect (TDET) bits are set based on the conditions sensed at the LNB output, VCP, and Tone Detect Input (TDI) pins, respectively. These bits are not latched and, unlike the other fault bits, may become reset without an I²C™ read sequence. The PNG, CPOK, and TDET bits are continuously updated.

There are three methods to detect when the Status register changes: responding to the interrupt request ($\overline{IRQ}$) pin going low, continuously polling the Status register via the I²C™ interface, or detecting a fault condition external to the A8300/A8300-1 and performing a diagnostic poll of the A8300/A8300-1. In any case, the master should read and re-read the Status register until the status changes.

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Table 4: Status Register Definition and IRQ Operation

Status (Read) Register Address [RC7:RC0] = 0000 0000

Bit	Name	Function	Latched?	Reset Condition	Effect on $\overline{IRQ}$ Pin
0	DIS	LNB output disabled	Yes	LNB enabled and no faults	None
1	CPOK	Charge pump OK	No	$V_{CP} > V_{BOOST} + 5$ V	None
2	OCP	Overcurrent	Auto-retry (RSMODE = 1)	OCP reset after every 1 s; IC enabled if fault is removed	$\overline{IRQ}$ set low; I²C™ Read sequence resets to high
			Latch (RSMODE = 0)	I²C™ Read sequence required after removing the fault	
3	EPF	Early Power Failure warning (V_{IN} < EPF threshold)	No	$V_{IN} >$ EPF_TH1	$\overline{IRQ}$ set low; I²C™ Read sequence resets to high
4	PNG	Power Not Good	No	LNB voltage within range	None
5	TDET	Tone detect	No	Tone removed from LNB pin	None
6	TSD	Thermal shutdown	Auto-retry (RSMODE = 1)	TSD reset after every 1 s; reset happens only if fault is removed	$\overline{IRQ}$ set low; I²C™ Read sequence resets to high
			Latch (RSMODE = 0)	I²C™ Read sequence required after removing the fault	
7	UVLO	V_{IN} or V_{REG} undervoltage	Yes	I²C™ Read sequence and $V_{IN} > 9.0$ V	$\overline{IRQ}$ set low; I²C™ Read sequence resets to high

Table 5: Status Register Bit Descriptions

Bit	Name	Description
0	DIS	The DIS bit is set to 1 when the A8300/A8300-1 is disabled, (ENB bit = 0) or there is a fault: UVLO, OCP, CPOK, or TSD.
1	CPOK	If this bit is set to 0, the internal charge pump is not operating correctly (VCP). If the charge pump voltage is too low, the LNB output is disabled and the DIS bit is set to 1.
2	OCP	This bit will be set to 1 if the LNB output current exceeds the overcurrent threshold ($I_{LNB(MAX)}$) for more than the overcurrent disable time (t_{DIS}). If the OCP bit is set to 1, then the DIS bit is also set to 1.
3	EPF	The EPF bit is set to 1 when the voltage on the EPF pin falls below EPF_TH. Also, $\overline{IRQ}$ is pulled low. When the EPF pin voltage goes above EPF_TH + EPF_TH_Hys, the EPF bit is reset to 0 after the delay selected by the EPF0 and EPF1 bits in the Control registers.
4	PNG	Set to 1 when the A8300/A8300-1 is enabled and the LNB output voltage is either too low or too high (nominally ±9% from the LNB DAC setting). Set to 0 when the A8300/A8300-1 is enabled and the LNB pin voltage is within the acceptable range (nominally ±5% from the LNB DAC setting).
5	TDET	The TDET bit is set to 1 if a tone is detected at the TDI pin that is within the specified voltage and frequency ranges. If a tone is being transmitted by the A8300/A8300-1, the tone detect low threshold is determined by $V_{TD(XMT)L}$. If a tone is being received from an external source, the tone detect low threshold is determined by $V_{TD(RCV)L}$.
6	TSD	The TSD bit is set to 1 if the A8300/A8300-1 has detected an overtemperature condition. If the TSD bit is set to 1,then the DIS bit is also set to 1.
7	UVLO	The UVLO bit is set to 1 if either the voltage at the VIN pin or the voltage at the VREG pin is too low. If the UVLO bit is set to 1, then the DIS bit is also set to 1. (Note: If V_{IN} is in an acceptable range and V_{REG} is too low, this bit cannot be read, and the I²C™ interface is inactive.)

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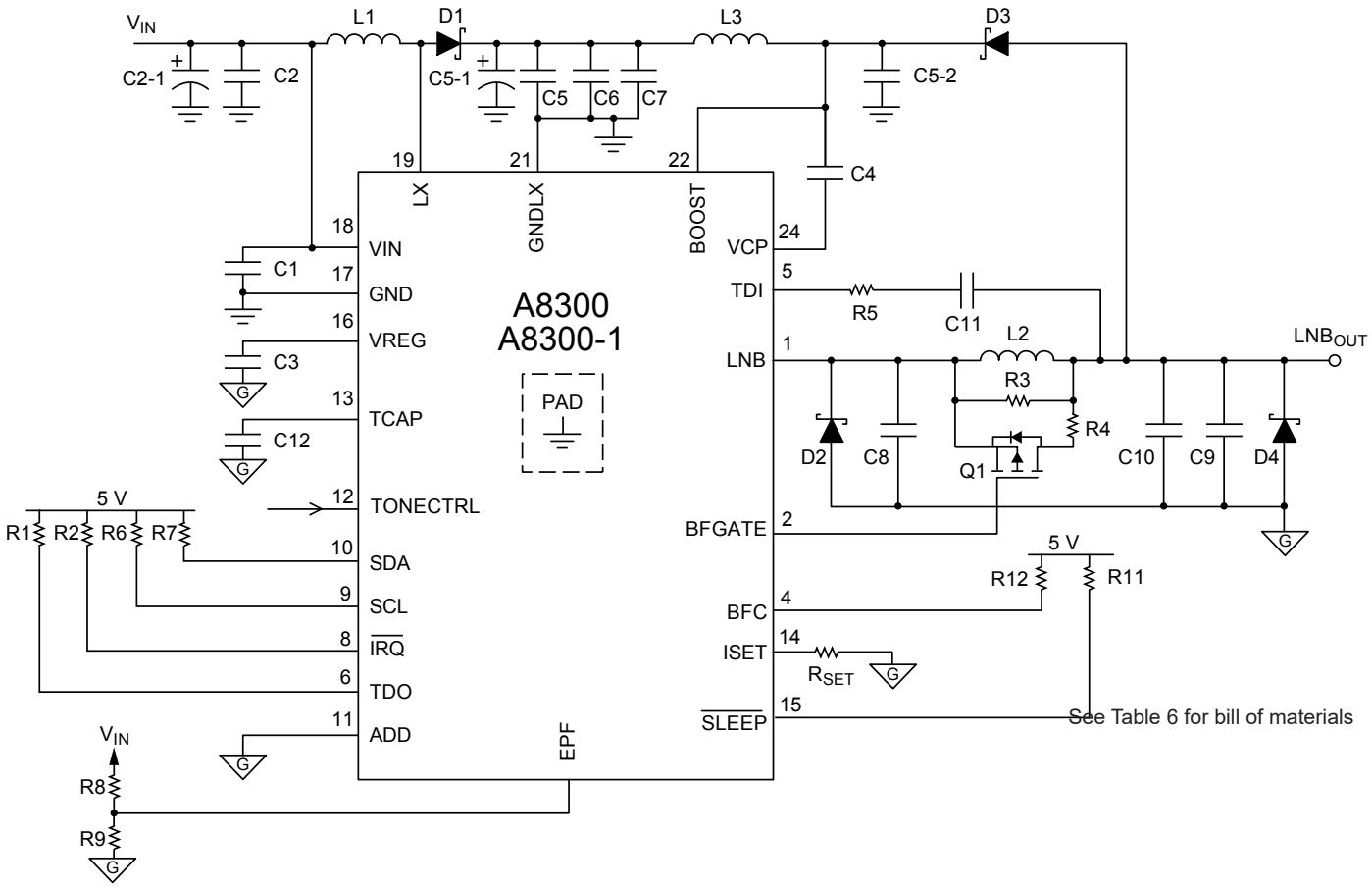
APPLICATION INFORMATION



Schematic 1: DiSEqC 2.0 Applications, V_{IN} = 12 V ±10%, I_{LNB} = 700 mA, surge of ±1000 V, 2 Ω, 1.2 A / 50 µs to 8 A / 20 µs combination wave

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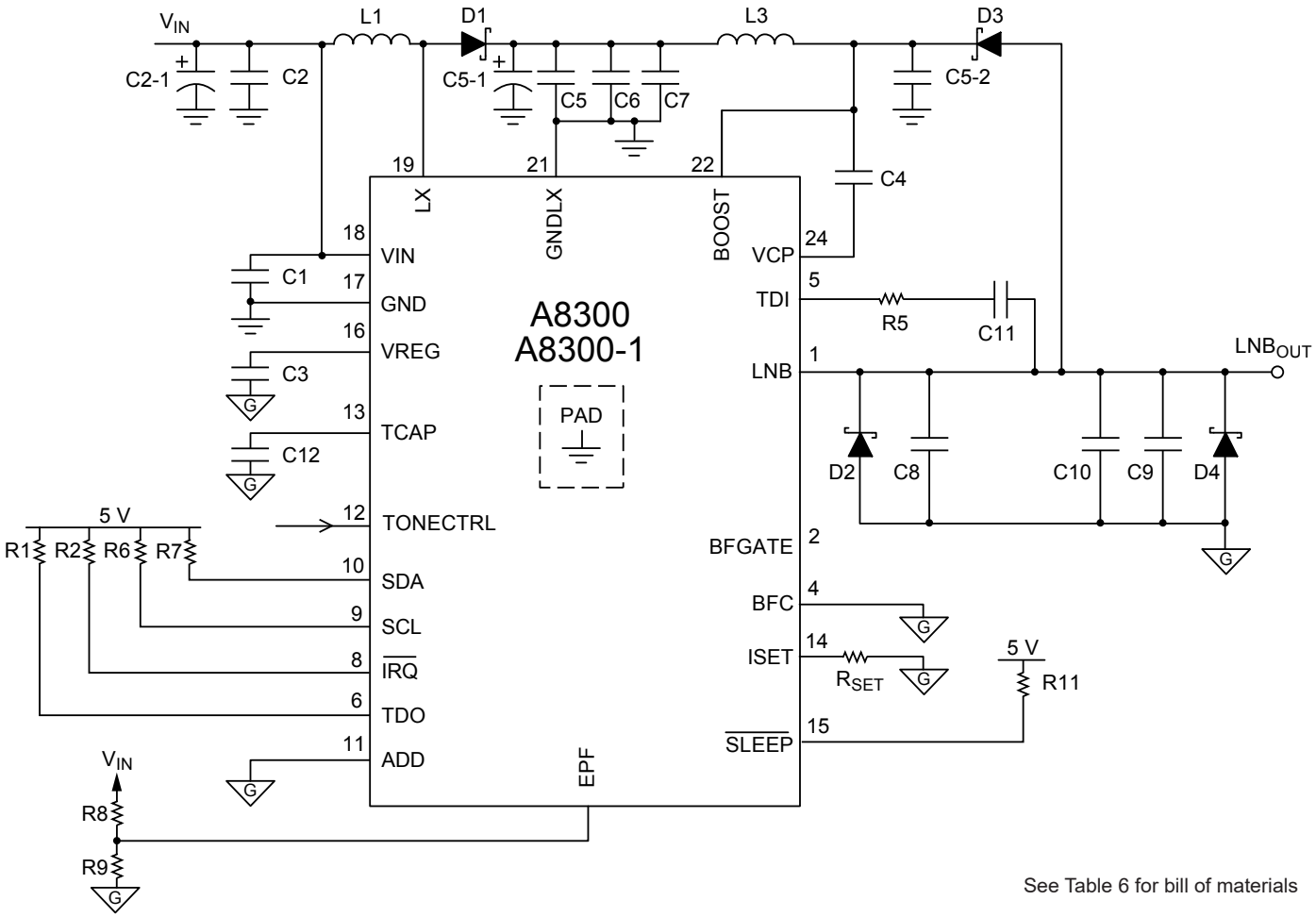

See Table 6 for bill of materials

Schematic 2: DiSEqC 1.0 Applications, V_{IN} = 12 V ±10%, I_{OUT} = 700 mA, surge of ±1000 V, 2 Ω, 1.2 A / 50 µs to 8 A / 20 µs combination wave

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Table 6: Component Selection Table for Schematics 1 and 2

Component	Characteristics	Recommended Devices	Comments
C1, C4, C8, C12	100 nF, 50 V, X5R or X7R, 0603		
C2	2X: 4.7 µF or 1X 10 µF, 25 V, X5R or X7R, 1206		For A8300 only; N.P. for A8300-1
C2-1, C5-1	100 µF / 35 V	Panasonic: EEE-FP1V101AP	For A8300-1 only; N.P. for A8300
C3	220 nF, 10 V (min.), X5R or X7R, 0603		
C5, C6, C7	3X: 4.7 µF, ±10%, 50 V, X7R, 1210, or 2X: 10 µF, ±10%, 35 V, X7R, 1210	4.7 µF: Murata: GRM32ER71H475KA88 Taiyo Yuden: UMK325B7475KM AVX: 12105C475KAT2A 10 µF: Murata: GRM32ER7YA106K	For A8300 only; N.P. for A8300-1
C5-2	1 µF / 50 V	Murata: GRM31CR71H105KA61L	For A8300-1 only; N.P. for A8300
C9, C11	10 nF, 50 V, X5R or X7R, 0603		
C10	220 nF, 50 V, X5R or X7R, 0603		
D1	Schottky diode, 3 A, 40 V, SMA	Sanken: SFPB-74 Vishay: B340A-E3/5AT Diodes, Inc.: B340A-13-F Central Semiconductor: CMSH3-40MA	
D2	Schottky diode, 1 A, 40 V, SOD-123	Diodes, Inc.: B140HW-7 Central Semiconductor: CMMSH1-40	
D3	Schottky diode, 1 A, 40 V, SOD-123	Diodes, Inc.: B140HW-7 Central Semiconductor: CMMSH1-40	For DiSEqC 2.0 applications
	Schottky diode, 3 A, 40 V, SMA	Sanken: SFPB-74 Vishay: B340A-E3/5AT Diodes, Inc.: B340A-13-F Central Semiconductor: CMSH3-40MA	For DiSEqC 1.0 applications
D4	TVS, 20 V_{RM}, 32 V_{CL} at 500 A, 3000 W	Littelfuse: SMDJ20A ST: LNBTVS6-221S	
L1	10 µH, ±30%, I_{SAT} ≥ 3.4 A, DCR < 75 mΩ	Cooper Bussmann: DR1040-100-R Wurth Electronics Inc : 744066100 Sumida America Components Inc: CDRH104RNP-100NC	
L2	220 µH, ±20%, I_{SAT} = 800 mA, DCR < 0.8 Ω	Cooper Bussmann: DR1040-221-R TDK: VLF10045T-221MR90	Short for DiSEqC 1.0 applications
L3	1 µH	Kemet: LB3218-T1R0MK Murata: LQM31PN1R0M00L TDK: MLP3216S1R0L	For A8300-1 only; short L3 with 0 Ω for A8300
Q1	MOSFET, P-channel, 50 V, < 0.5 Ω, SOT-23	Vishay: SI2309DS-T1-E3 Diodes, Inc.: ZXMP6A13FTA	N. P. for DiSEqC 1.0 applications
R1, R2, R6, R7, R11, R12	Resistor, 2 kΩ, 1%, 0402 or 0603		R12 for only DiSEqC 2.0 applications
R3	Resistor, 15 Ω, 1%, 0402 or 0603		N. P. for DiSEqC 1.0 applications
R4	Resistor, 0.47 Ω, 1%, 0402 or 0603		N. P. for DiSEqC 1.0 applications
R5	Resistor, 100 Ω, 1%, 0402 or 0603		
R8	Resistor, 20.5 kΩ, 1%, 0402 or 0603		
R9	Resistor, 10.2 kΩ, 1%, 0402 or 0603		
RSET	Resistor, 37.4 kΩ, 1%, 0402 or 0603		

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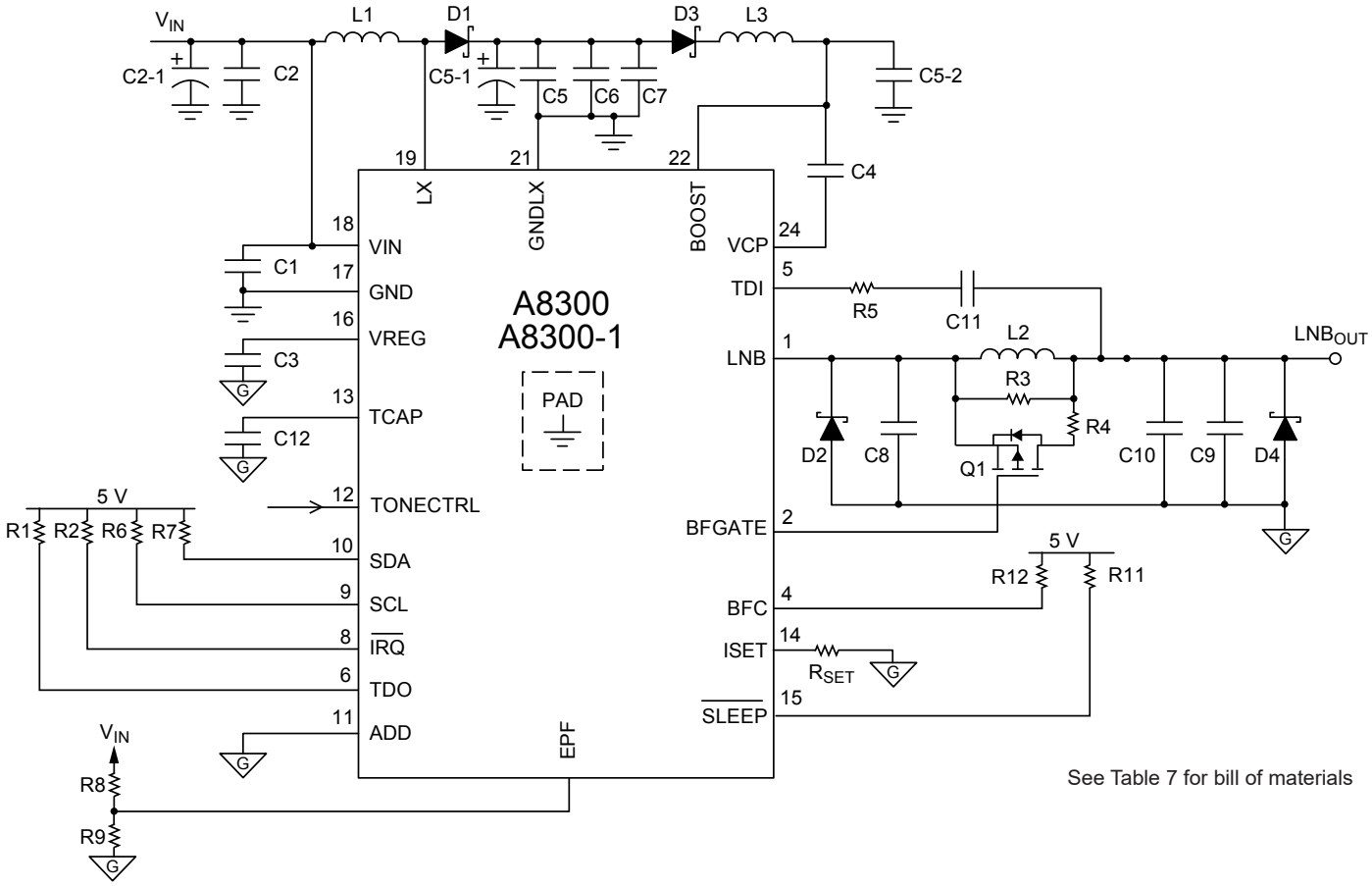

Schematic 3: DiSEqC 2.0 Applications for increased surge requirements,
±1000 V, 2 Ω, 1.2 A / 50 µs to 8 A / 20 µs combination wave and “stress to TVS failure” (or ±4000 V) test

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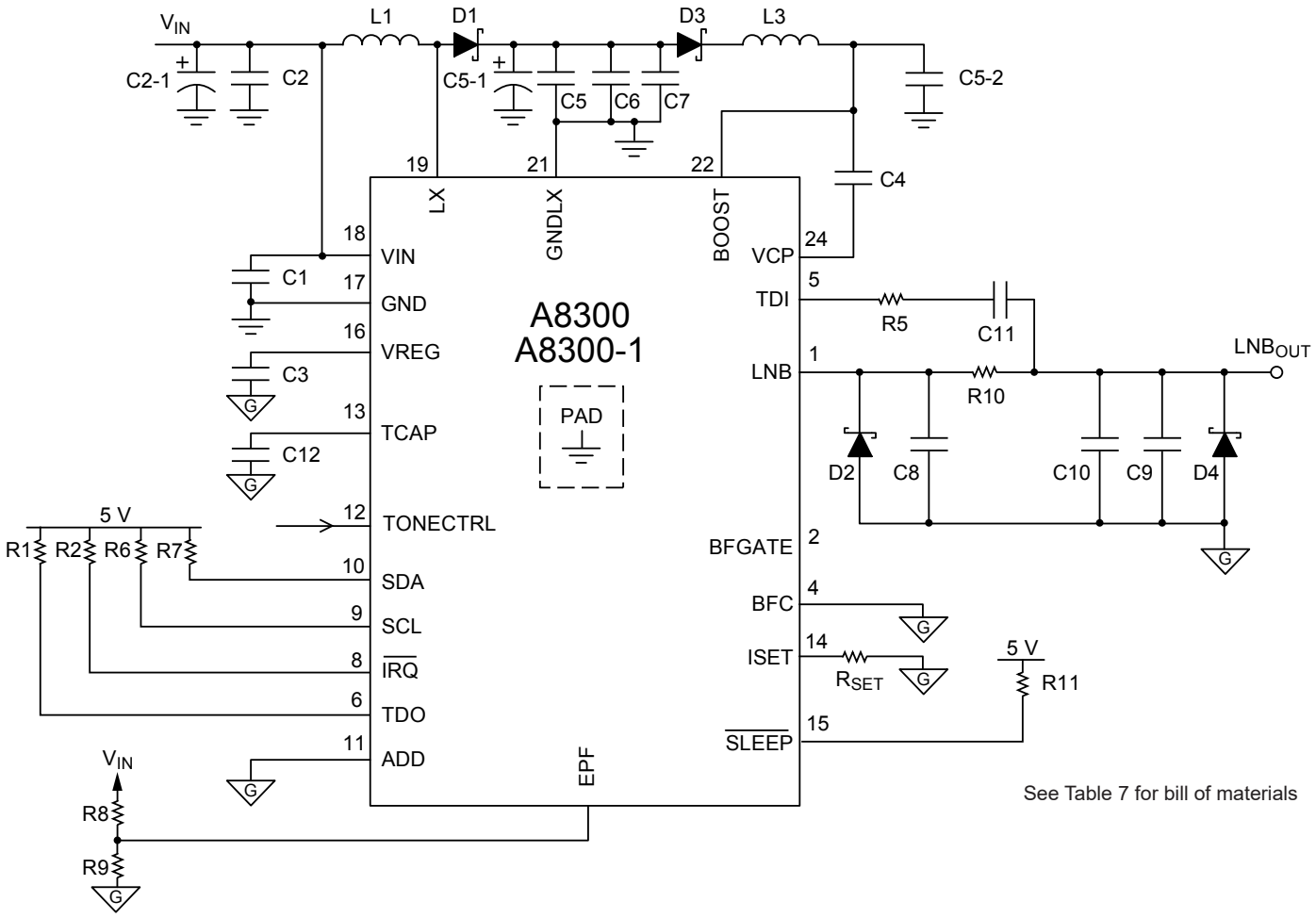

Schematic 4: DiSEqC 1.0 Applications for increased surge requirements, ±1000 V,
2 Ω, 1.2 A / 50 µs to 8 A / 20 µs combination wave and “stress to TVS failure” (or ±4000 V) test

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Table 7: Component Selection Table for Schematics 3 and 4

Component	Characteristics	Recommended Devices	Comments
C1, C4, C8, C12	100 nF, 50 V, X5R or X7R, 0603		
C2	2X: 4.7 µF or 1X 10 µF, 25 V, X5R or X7R, 1206		For A8300 only; N.P. for A8300-1
C2-1, C5-1	100 µF / 35 V	Panasonic: EEE-FP1V101AP	For A8300-1 only; N.P. for A8300
C3	220 nF, 10 V (min.), X5R or X7R, 0603		
C5, C6, C7	3X: 4.7 µF, ±10%, 50 V, X7R, 1210, or 2X: 10 µF, ±10%, 35 V, X7R, 1210	4.7 µF: Murata: GRM32ER71H475KA88 Taiyo Yuden: UMK325B7475KM AVX: 12105C475KAT2A 10 uF: Murata: GRM32ER7YA106K	For A8300 only; N.P. for A8300-1
C5-2	1 µF / 50 V	Murata: GRM31CR71H105KA61L	For A8300-1 only; N.P. for A8300
C9, C11	10 nF, 50 V, X5R or X7R, 0603		
C10	220 nF, 50 V, X5R or X7R, 0603		
D1	Schottky diode, 3 A, 40 V, SMA	Sanken: SFPB-74 Vishay: B340A-E3/5AT Diodes, Inc.: B340A-13-F Central Semiconductor: CMSH3-40MA	
D2, D3	Schottky diode, 3 A, 50 V, SMA	Diodes, Inc.: B350A-13-F Vishay: B350A-E3/5AT	
D4	TVS, 20 V_{RM}, 32 V_{CL} at 500 A, 3000 W	Littelfuse: SMDJ20A ST: LNBTVS6-221S	
L1	10 µH, ±30%, I_{SAT} ≥ 3.4 A, DCR < 75 mΩ	Cooper Bussmann: DR1040-100-R Wurth Electronics Inc : 744066100 Sumida America Components Inc: CDRH104RNP-100NC	
L2	220 µH, ±20%, I_{SAT} = 800 mA, DCR < 0.8 Ω	Cooper Bussmann: DR1040-221-R TDK: VLF10045T-221MR90	Replace L2 with R10 for DiSEqC 1.0 applications
L3	1 µH	Kemet: LB3218-T1R0MK Murata: LQM31PN1R0M00L TDK: MLP3216S1R0L	For A8300-1 only; short L3 with 0 Ω for A8300
Q1	MOSFET, P-channel, 50 V, < 0.5 Ω, SOT-23	Vishay: SI2309DS-T1-E3 Diodes, Inc.: ZXMP6A13FTA	N. P. for DiSEqC 1.0 applications
R1, R2, R6, R7, R11, R12	Resistor, 2 kΩ, 1%, 0402 or 0603		R12 for only DiSEqC 2.0 applications
R3	Resistor, 15 Ω, 1%, 0402 or 0603		N. P. for DiSEqC 1.0 applications
R4	Resistor, 0.47 Ω, 1%, 0402 or 0603		N. P. for DiSEqC 1.0 applications
R5	Resistor, 100 Ω, 1%, 0402 or 0603		
R8	Resistor, 20.5 kΩ, 1%, 0402 or 0603		
R9	Resistor, 10.2 kΩ, 1%, 0402 or 0603		
R10	Resistor, 0.47 Ω, $^1/_4$ W, 1%, 1206	Rohm: MCR18EZHFLR470	Replace R10 with L2 for DiSEqC 2.0 applications
RSET	Resistor, 37.4 kΩ, 1%, 0402 or 0603		

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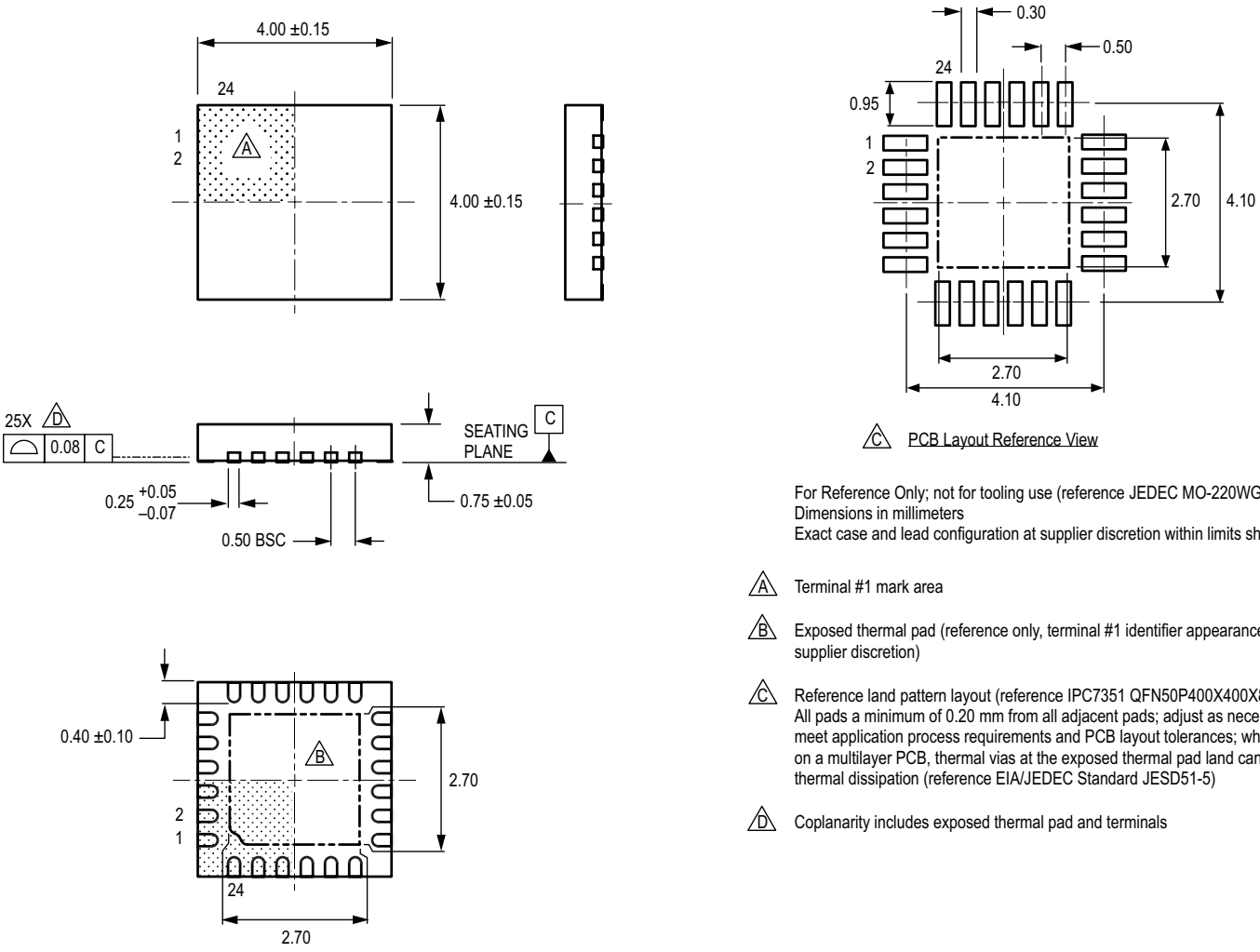
PACKAGE OUTLINE DRAWING



For Reference Only; not for tooling use (reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M) All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package ES 24-Pin QFN
with Exposed Thermal Pad

Revision History

Number	Date	Description
2	March 3, 2014	Corrected typo in selection guide
3	April 29, 2014	Revised Package Drawing
4	January 11, 2016	Corrected Terminal List Table (page 4)
5	July 22, 2016	Updated Component Selection Tables (pages 32 and 35)
6	January 11, 2018	Minor editorial updates
7	January 21, 2019	Minor editorial updates

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