

Ultra low quiescent current linear voltage regulator

Features

- Ultra low quiescent current of 9 µA
- Wide input voltage range of 2.75 V to 42 V
- Output current capacity up to 100 mA
- Off mode current less than 1 µA
- Low drop out voltage of typ. 250 mV @ 100 mA
- Output current limit protection
- Overtemperature shutdown
- Enable
- Reset
- Available in PG-DSO-8 EP package
- Available in PG-TSON-10 package
- Wide temperature range
- Green Product (RoHS-compliant)
- AEC Qualified

Potential applications

- Applications with direct battery connection
- Automotive general ECUs
- On-board sensor supply
- Infotainment, alarm, dashboard
- RKE, immobilizer, gateway

Product validation

Qualified for automotive applications.
Product validation according to AEC-Q100.

Description

The TLS810D1 is a linear voltage regulator featuring wide input voltage range, low drop out voltage and ultra low quiescent current.

With an input voltage range of 2.75 V to 42 V and ultra low quiescent of only 9 µA, the regulator is perfectly suitable for automotive or any other supply systems connected permanently to the battery.

The OPTIREG™ linear TLS810D1xxV33 is the fixed 3.3 V output version with an accuracy of 2% and output current capability up to 100 mA.

The new regulation concept implemented in TLS810D1 combines fast regulation and very good stability while requiring only a small ceramic capacitor of 1 µF at the output.

The tracking region starts already at input voltages of 2.75 V (extended operating range). This makes the TLS810D1 also suitable to supply automotive systems that need to operate during cranking condition.

Internal protection features like output current limitation and overtemperature shutdown are implemented to protect the device against immediate damage due to failures like output short circuit to GND, overcurrent and overtemperature.

The device can be switched on and off by the Enable feature. When the device is switched off, the current consumption is typically less than 1 µA.

The output voltage is supervised by the Reset feature, including undervoltage reset and delayed reset release at power-on.

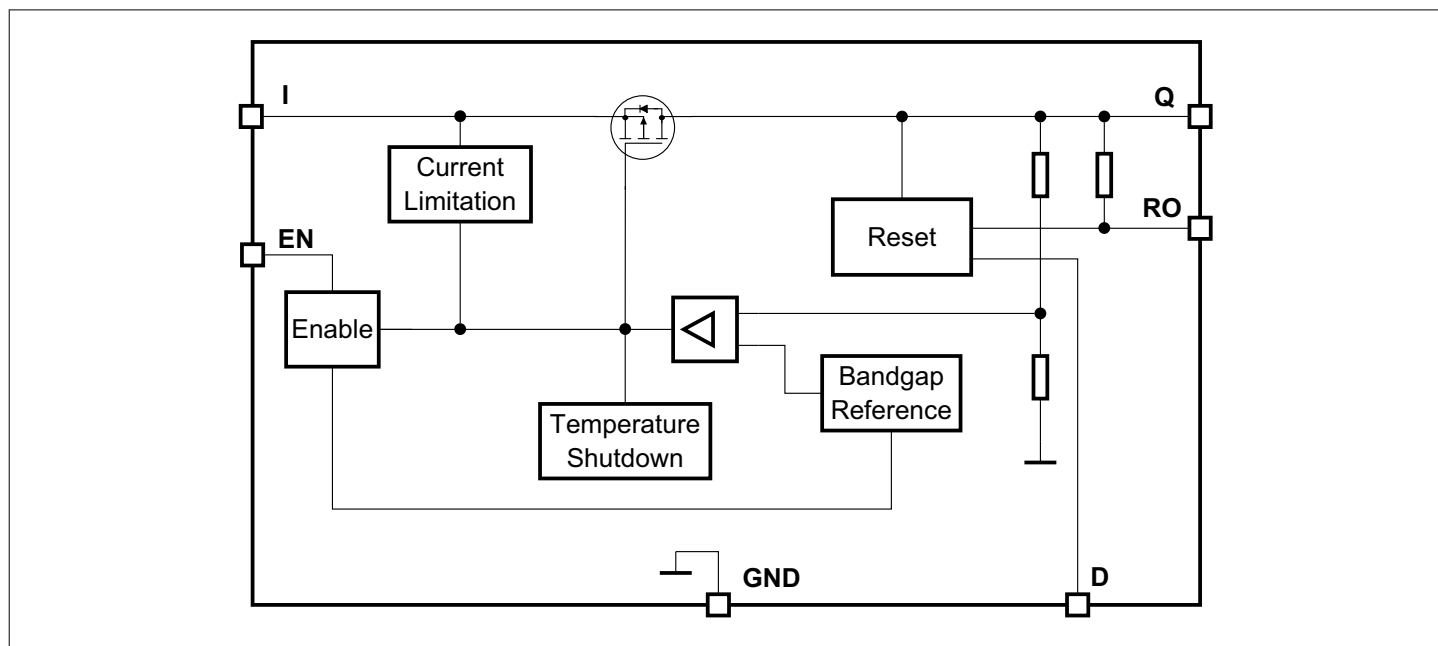


| Type          | Package     | Marking  |
|---------------|-------------|----------|
| TLS810D1EJV33 | PG-DSO-8 EP | 810D1V33 |
| TLS810D1LDV33 | PG-TSON-10  | 810D1V3  |

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## 1 Block diagram



**Figure 1** **Block diagram**

2 Pin configuration

2.1 Pin assignment in PG-DSO-8 EP package

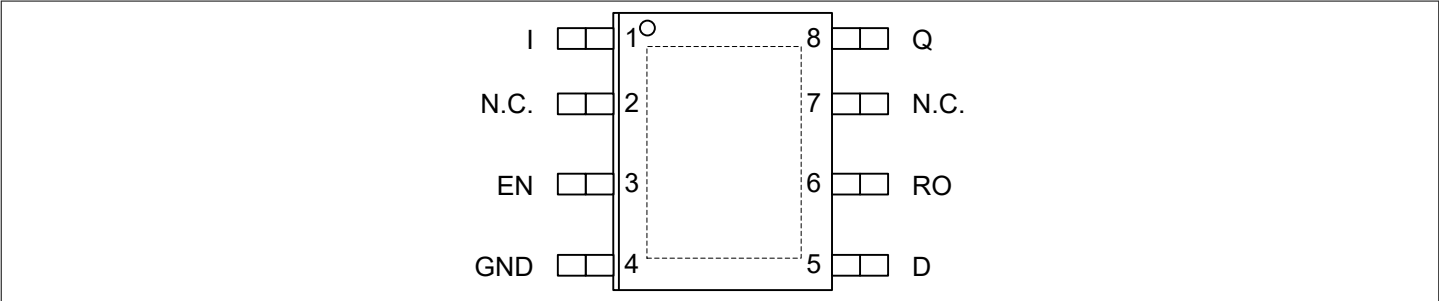


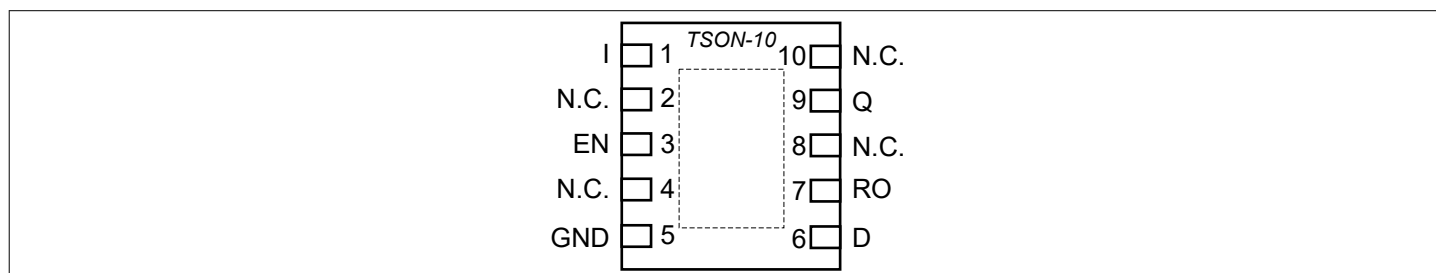
Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

| Pin | Symbol | Function   |
|-----|--------|--|
| 1   | I      | <b>Input</b><br>It is recommended to place a small ceramic capacitor (for example 100 nF) to GND, close to the IC terminals, in order to compensate line influences.                     |
| 2   | N.C.   | <b>Not connected</b>   |
| 3   | EN     | <b>Enable</b><br>Integrated pull-down resistor.<br>Enable the IC with high level input signal.<br>Disable the IC with low level input signal.  |
| 4   | GND    | <b>Ground</b>  |
| 5   | D      | <b>Reset delay timing</b><br>Connect a ceramic capacitor to GND for adjusting the reset delay time.<br>Leave open if the reset function is not needed.                                   |
| 6   | RO     | <b>Reset output</b><br>Integrated pull-up resistor.<br>Open collector output.<br>Leave open if the reset function is not needed.   |
| 7   | N.C.   | <b>Not connected</b>   |
| 8   | Q      | <b>Output</b><br>Connect an output capacitor $C_Q$ to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in <a href="#">Functional range</a> . |
| Pad | –      | <b>Exposed pad</b><br>Connect to heatsink area.<br>Connect to GND.   |

## 2.3 Pin assignment in PG-TSON-10 package



**Figure 3** Pin configuration

## 2.4 Pin definitions and functions

**Table 2** Pin definitions and functions

| Pin | Symbol | Function   |
|-----|--------|--|
| 1   | I      | <b>Input</b><br>It is recommended to place a small ceramic capacitor (for example 100 nF) to GND, close to the IC terminals, in order to compensate line influences.                     |
| 2   | N.C.   | <b>Not connected</b>   |
| 3   | EN     | <b>Enable</b><br>Integrated pull-down resistor.<br>Enable the IC with high level input signal.<br>Disable the IC with low level input signal.  |
| 4   | N.C.   | <b>Not connected</b>   |
| 5   | GND    | <b>Ground</b>  |
| 6   | D      | <b>Reset delay timing</b><br>Connect a ceramic capacitor to GND for adjusting the reset delay time.<br>Leave open if the reset function is not needed.                                   |
| 7   | RO     | <b>Reset Output</b><br>Integrated pull-up resistor.<br>Open collector output.<br>Leave open if the reset function is not needed.   |
| 8   | N.C.   | <b>Not connected</b>   |
| 9   | Q      | <b>Output</b><br>Connect an output capacitor $C_Q$ to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in <a href="#">Functional range</a> . |
| 10  | N.C.   | <b>Not connected</b>   |
| Pad | –      | <b>Exposed pad</b><br>Connect to heatsink area.<br>Connect to GND.   |

## 3 General product characteristics

### 3.1 Absolute maximum ratings

**Table 3** Absolute maximum ratings <sup>1)</sup>

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

| Parameter                      | Symbol        | Values |      |      | Unit | Note or Test Condition    | Number  |
|--------------------------------|---------------|--------|------|------|------|---------------------------|---------|
|                                |               | Min.   | Typ. | Max. |      |                           |         |
| Voltage input I, Enable EN     |               |        |      |      |      |                           |         |
| Voltage                        | $V_I, V_{EN}$ | -0.3   | –    | 45   | V    | –                         | P_4.1.1 |
| Voltage output Q               |               |        |      |      |      |                           |         |
| Voltage                        | $V_Q$         | -0.3   | –    | 7    | V    | –                         | P_4.1.2 |
| Reset output RO, Reset delay D |               |        |      |      |      |                           |         |
| Voltage                        | $V_{RO}, V_D$ | -0.3   | –    | 7    | V    | –                         | P_4.1.3 |
| Temperatures                   |               |        |      |      |      |                           |         |
| Junction temperature           | $T_j$         | -40    | –    | 150  | °C   | –                         | P_4.1.4 |
| Storage temperature            | $T_{stg}$     | -55    | –    | 150  | °C   | –                         | P_4.1.5 |
| ESD robustness                 |               |        |      |      |      |                           |         |
| ESD robustness all pins (HBM)  | $V_{ESD,HBM}$ | -2     | –    | 2    | kV   | <sup>2)</sup>             | P_4.1.6 |
| ESD robustness all pins (CDM)  | $V_{ESD,CDM}$ | -750   | –    | 750  | V    | <sup>3)</sup> at all pins | P_4.1.7 |

1) Not subject to production test, specified by design.

2) ESD robustness, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS001 (1.5 k $\Omega$ , 100 pF)

3) ESD robustness, Charged Device Model (CDM) according JEDEC JESD22-C101

#### Notes:

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

## 3.2 Functional range

**Table 4** Functional range

| Parameter                    | Symbol      | Values               |      |      | Unit | Note or Test Condition | Number  |
|------------------------------|-------------|----------------------|------|------|------|------------------------|---------|
|                              |             | Min.                 | Typ. | Max. |      |                        |         |
| Input voltage range          | $V_I$       | $V_{Q,nom} + V_{dr}$ | –    | 42   | V    | 1)                     | P_4.2.1 |
| Extended input voltage range | $V_{I,ext}$ | 2.75                 | –    | 42   | V    | 2)                     | P_4.2.2 |
| Enable voltage range         | $V_{EN}$    | 0                    | –    | 42   | V    | –                      | P_4.2.3 |
| Output capacitor             | $C_Q$       | 1                    | –    | –    | μF   | 3) 4)                  | P_4.2.4 |
| Output capacitor's ESR       | $ESR(C_Q)$  | –                    | –    | 100  | Ω    | 4)                     | P_4.2.5 |
| Junction temperature         | $T_j$       | -40                  | –    | 150  | °C   | –                      | P_4.2.6 |

1) Output current is limited internally and depends on the input voltage, see Electrical characteristics for more details.

2) When  $V_I$  is between  $V_{I,ext,min}$  and  $V_{Q,nom} + V_{dr}$ ,  $V_Q = V_I - V_{dr}$ . When  $V_I$  is below  $V_{I,ext,min}$ ,  $V_Q$  can drop down to 0 V.

3) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

4) Not subject to production testing, specified by design.

**Note:** Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

### 3.3 Thermal resistance

**Note:** This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 5 Thermal resistance TLS810D1 in PG-DSO-8 EP package<sup>1)</sup>**

| Parameter           | Symbol     | Values |      |      | Unit | Note or Test Condition   | Number  |
|---------------------|------------|--------|------|------|------|--|---------|
|                     |            | Min.   | Typ. | Max. |      |  |         |
| Junction to case    | $R_{thJC}$ | –      | 19   | –    | K/W  | –  | P_4.3.1 |
| Junction to ambient | $R_{thJA}$ | –      | 51   | –    | K/W  | <sup>2)</sup> 2s2p board   | P_4.3.2 |
| Junction to ambient | $R_{thJA}$ | –      | 167  | –    | K/W  | <sup>3)</sup> 1s0p board, footprint only                           | P_4.3.3 |
| Junction to ambient | $R_{thJA}$ | –      | 71   | –    | K/W  | <sup>3)</sup> 1s0p board, 300 mm <sup>2</sup> heatsink area on PCB | P_4.3.4 |
| Junction to ambient | $R_{thJA}$ | –      | 60   | –    | K/W  | <sup>3)</sup> 1s0p board, 600 mm <sup>2</sup> heatsink area on PCB | P_4.3.5 |

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 1 copper layer (1 × 70 μm Cu).

**Table 6 Thermal resistance TLS810D1 in PG-TSON-10 package<sup>1)</sup>**

| Parameter           | Symbol     | Values |      |      | Unit | Note or Test Condition   | Number   |
|---------------------|------------|--------|------|------|------|--|----------|
|                     |            | Min.   | Typ. | Max. |      |  |          |
| Junction to case    | $R_{thJC}$ | –      | 13   | –    | K/W  | –  | P_4.3.6  |
| Junction to ambient | $R_{thJA}$ | –      | 60   | –    | K/W  | <sup>2)</sup> 2s2p board   | P_4.3.7  |
| Junction to ambient | $R_{thJA}$ | –      | 184  | –    | K/W  | <sup>3)</sup> 1s0p board, footprint only                           | P_4.3.8  |
| Junction to ambient | $R_{thJA}$ | –      | 75   | –    | K/W  | <sup>3)</sup> 1s0p board, 300 mm <sup>2</sup> heatsink area on PCB | P_4.3.9  |
| Junction to ambient | $R_{thJA}$ | –      | 64   | –    | K/W  | <sup>3)</sup> 1s0p board, 600 mm <sup>2</sup> heatsink area on PCB | P_4.3.10 |

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 1 copper layer (1 × 70 μm Cu).

## 4 Block description and electrical characteristics

### 4.1 Voltage regulation

The output voltage  $V_Q$  is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

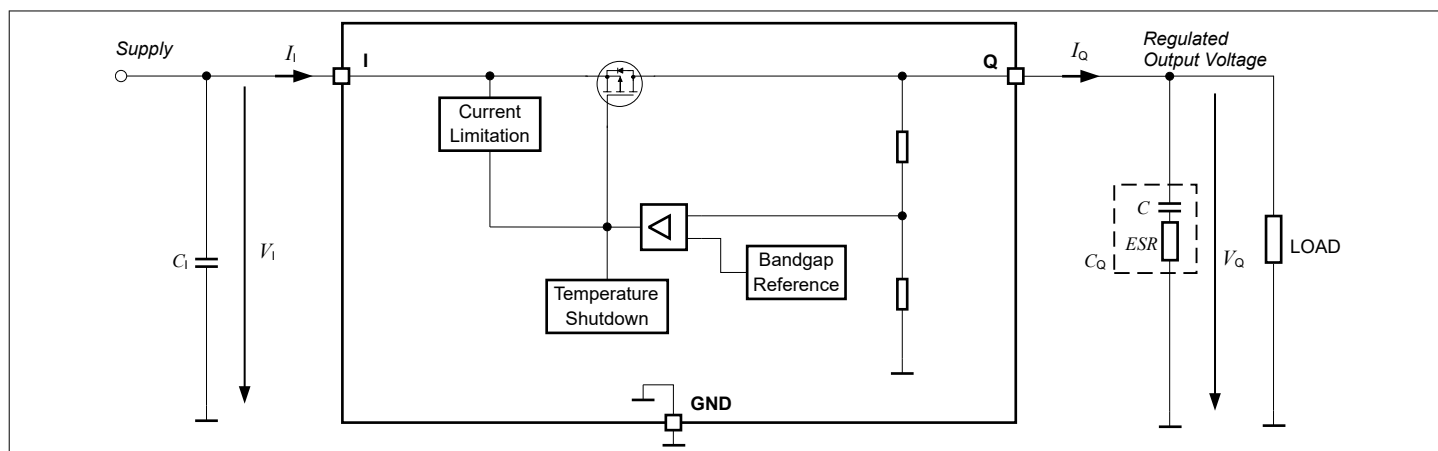
The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the internal circuit structure. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistance ESR requirements given in [Functional range](#) have to be maintained. For details see the typical performance graph [Output capacitor equivalent series resistance ESR \( \$C\_Q\$ \) versus output current  \$I\_Q\$](#) . Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor  $C_I$  is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used, in case the input is connected directly to the battery line. Connect the capacitors close to the regulator terminals.

In order to prevent overshoots during start-up, a smooth ramping up function is implemented. This ensures almost no overshoots during start-up, mostly independent from load and output capacitance.

Whenever the load current exceeds the specified limit, for example in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (for example output continuously short-circuit) by switching off the power stage. After the chip has cooled down, the regulator restarts. This oscillatory thermal behavior causes the junction temperature to exceed the maximum rating of 150°C and can significantly reduce the IC's lifetime.



**Figure 4** Block diagram voltage regulation

**Table 7 Electrical characteristics**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified).

Typical values are given at  $T_j = 25^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ .

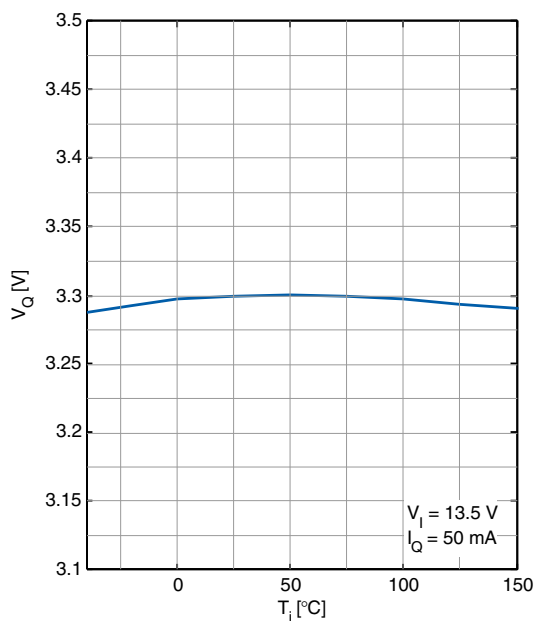
| Parameter                                     | Symbol                     | Values |      |      | Unit             | Note or Test Condition   | Number  |
|---|----------------------------|--------|------|------|------------------|--|---------|
|   |                            | Min.   | Typ. | Max. |                  |  |         |
| Output voltage precision                      | $V_Q$                      | 3.23   | 3.30 | 3.37 | V                | $50\text{ }\mu\text{A} \leq I_Q \leq 100\text{ mA}$ ,<br>$4\text{ V} \leq V_I \leq 28\text{ V}$                                  | P_5.1.1 |
| Output voltage precision                      | $V_Q$                      | 3.23   | 3.30 | 3.37 | V                | $50\text{ }\mu\text{A} \leq I_Q \leq 50\text{ mA}$ ,<br>$4\text{ V} \leq V_I \leq 42\text{ V}$                                   | P_5.1.2 |
| Output current limitation                     | $I_{Q,\text{lim}}$         | 110    | 190  | 260  | mA               | $0\text{ V} \leq V_Q \leq V_{Q,\text{nom}} - 0.1\text{ V}$   | P_5.1.3 |
| Line regulation steady-state                  | $\Delta V_{Q,\text{line}}$ | –      | 1    | 20   | mV               | $I_Q = 1\text{ mA}$ , $6\text{ V} \leq V_I \leq 32\text{ V}$   | P_5.1.4 |
| Load regulation steady-state                  | $\Delta V_{Q,\text{load}}$ | -20    | -1   | –    | mV               | $V_I = 6\text{ V}$ ,<br>$50\text{ }\mu\text{A} \leq I_Q \leq 100\text{ mA}$  | P_5.1.5 |
| Dropout voltage $V_{\text{dr}} = V_I - V_Q$   | $V_{\text{dr}}$            | –      | 250  | 650  | mV               | <sup>1)</sup> $I_Q = 100\text{ mA}$  | P_5.1.6 |
| Ripple rejection                              | $PSRR$                     | –      | 60   | –    | dB               | <sup>2)</sup> $I_Q = 50\text{ mA}$ ,<br>$f_{\text{ripple}} = 100\text{ Hz}$ ,<br>$V_{\text{ripple}} = 0.5\text{ V}_{\text{p-p}}$ | P_5.1.7 |
| Overtemperature shutdown threshold            | $T_{j,\text{sd}}$          | 151    | 175  | –    | $^\circ\text{C}$ | <sup>2)</sup> $T_j$ increasing   | P_5.1.8 |
| Overtemperature shutdown threshold hysteresis | $T_{j,\text{sdh}}$         | –      | 10   | –    | K                | <sup>2)</sup> $T_j$ decreasing   | P_5.1.9 |

1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{ V}$ .

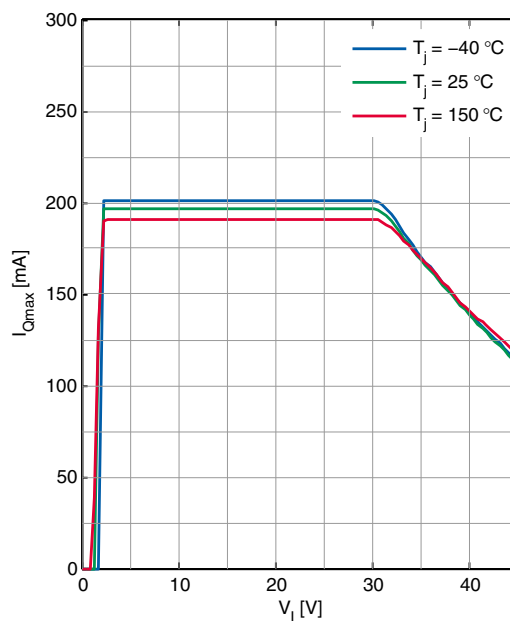
2) Not subject to production test, specified by design.

## 4.2 Typical performance characteristics voltage regulation

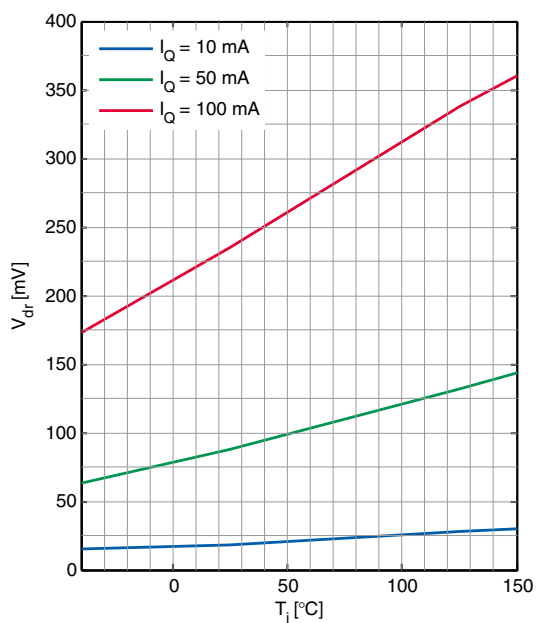
Output voltage  $V_Q$  versus  
junction temperature  $T_j$



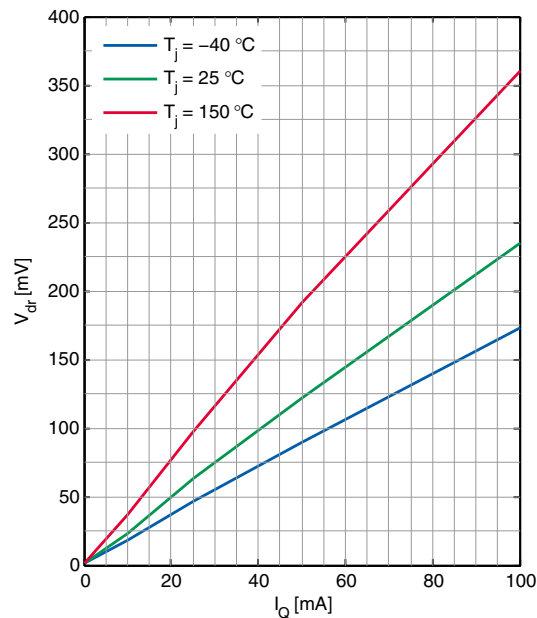
Output current  $I_Q$  versus  
input voltage  $V_I$



Dropout voltage  $V_{dr}$  versus  
junction temperature  $T_j$

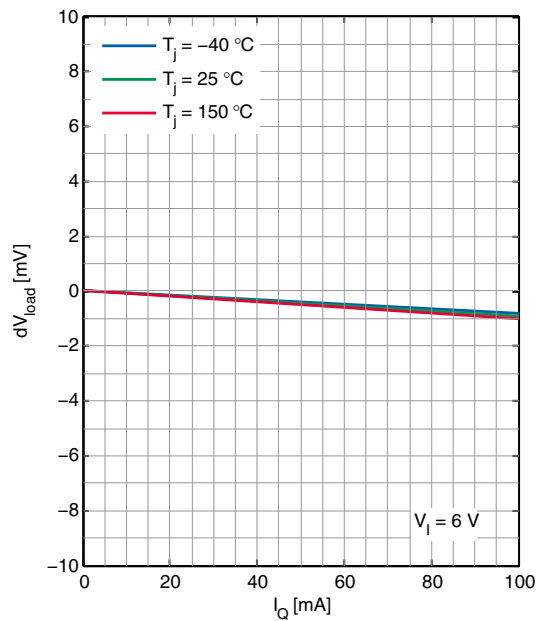


Dropout voltage  $V_{dr}$  versus  
output current  $I_Q$

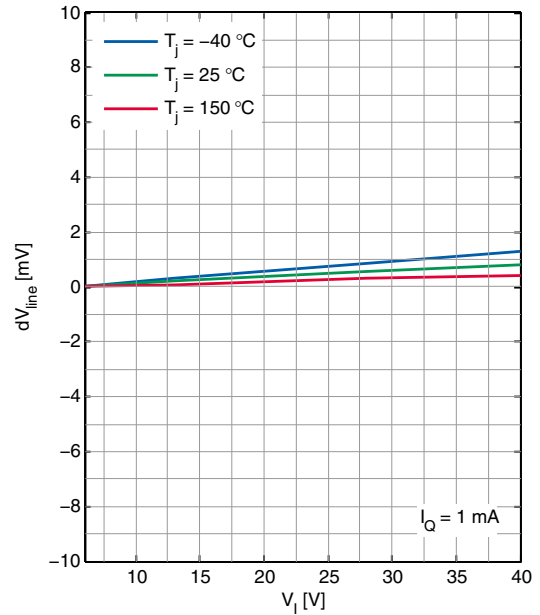


**4 Block description and electrical characteristics**

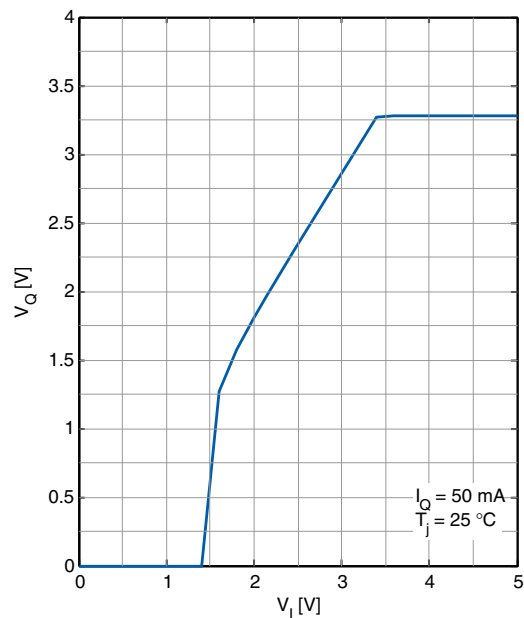
Load regulation  $\Delta V_{Q,load}$  versus  
output current  $I_Q$



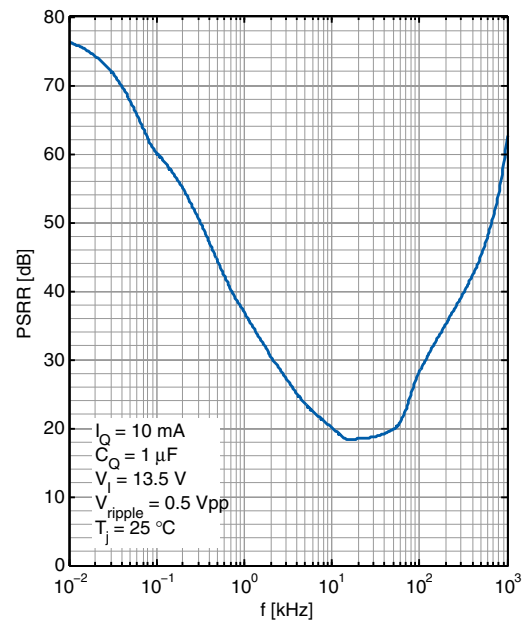
Line regulation  $\Delta V_{Q,line}$  versus  
input voltage  $V_I$



Output voltage  $V_Q$  versus  
input voltage  $V_I$

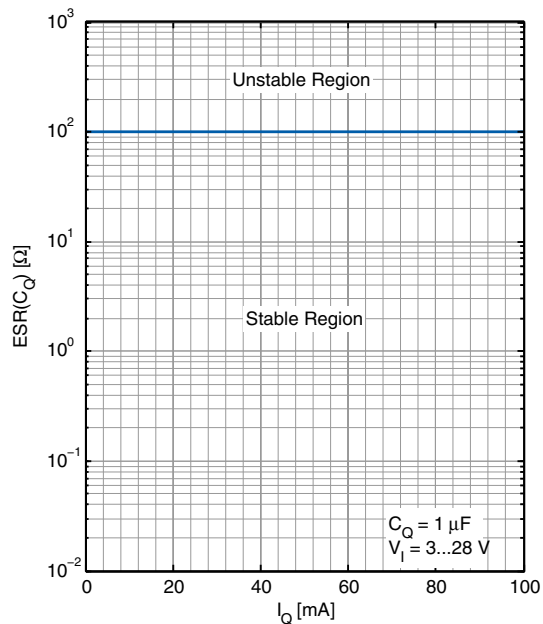


Power supply ripple rejection  $PSRR$  versus  
ripple frequency  $f_r$



**4 Block description and electrical characteristics**

Output capacitor equivalent series resistance  $ESR(C_Q)$   
versus  
output current  $I_Q$



### 4.3 Current consumption

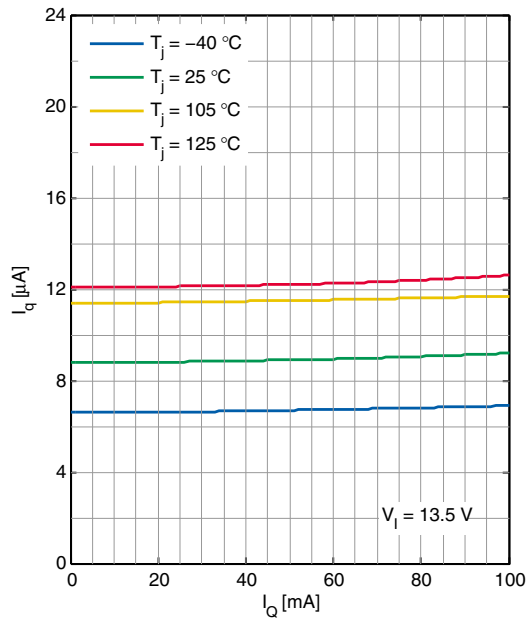
**Table 8** Electrical characteristics current consumption

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$  (unless otherwise specified).

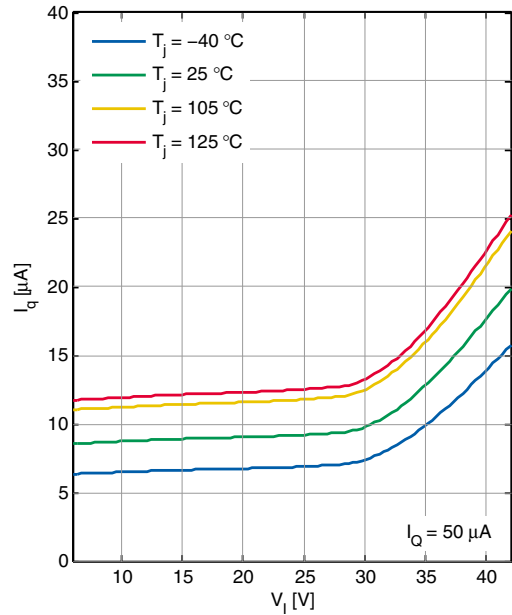
| Parameter                                | Symbol      | Values |      |      | Unit          | Note or Test Condition                                    | Number  |
|--|-------------|--------|------|------|---------------|---|---------|
|  |             | Min.   | Typ. | Max. |               |   |         |
| Current consumption<br>$I_q = I_I$       | $I_{q,off}$ | –      | –    | 1    | $\mu\text{A}$ | $V_{EN} \leq 0.4\text{ V}$ , $T_j < 105^\circ\text{C}$    | P_5.3.1 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$       | –      | 9    | 11.5 | $\mu\text{A}$ | $I_Q = 50\text{ }\mu\text{A}$ , $T_j = 25^\circ\text{C}$  | P_5.3.2 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$       | –      | 11.5 | 14.5 | $\mu\text{A}$ | $I_Q = 50\text{ }\mu\text{A}$ , $T_j < 105^\circ\text{C}$ | P_5.3.3 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$       | –      | 12   | 16   | $\mu\text{A}$ | $I_Q = 50\text{ }\mu\text{A}$ , $T_j < 125^\circ\text{C}$ | P_5.3.4 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$       | –      | 12   | 16   | $\mu\text{A}$ | $I_Q = 100\text{ mA}$ , $T_j < 125^\circ\text{C}$         | P_5.3.5 |

## 4.4 Typical performance characteristics current consumption

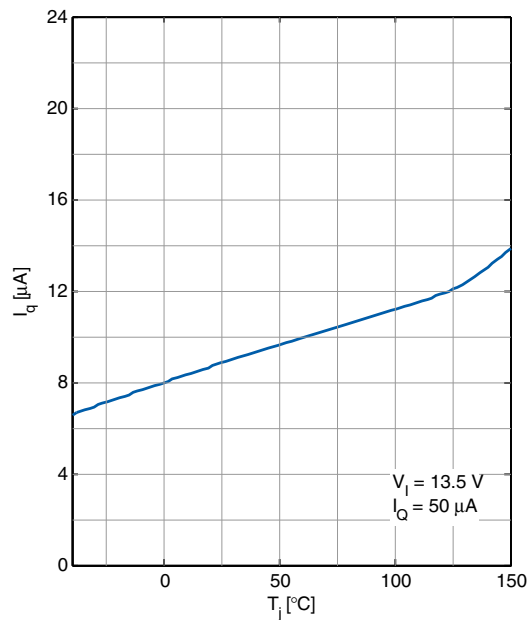
Current consumption  $I_q$  versus  
output current  $I_Q$



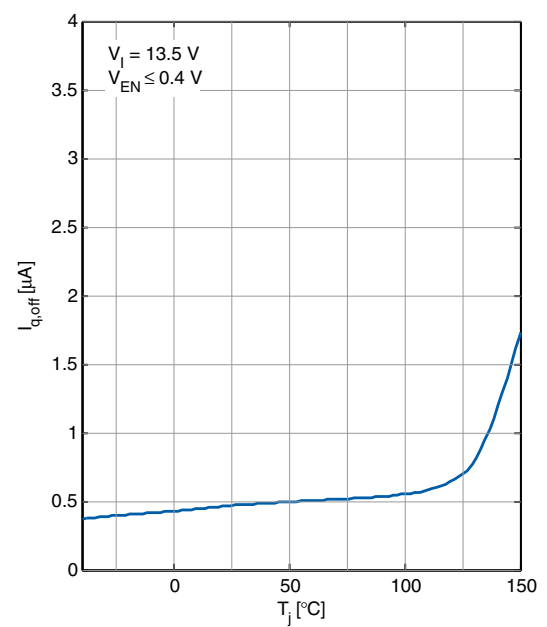
Current consumption  $I_q$  versus  
input voltage  $V_I$



Current consumption  $I_q$  versus  
junction temperature  $T_j$



Current consumption in OFF mode  $I_{q,off}$  versus  
junction temperature  $T_j$



## 4.5 Enable

The device can be switched on and off by the Enable feature. Connect a HIGH level as specified below (for example the battery voltage) to pin EN to enable the device; connect a LOW level as specified below (for example GND) to switch it off. The Enable function has a build-in hysteresis to avoid toggling between ON/OFF state, if signals with slow slopes are applied to the EN input.

**Table 9 Electrical characteristics enable**

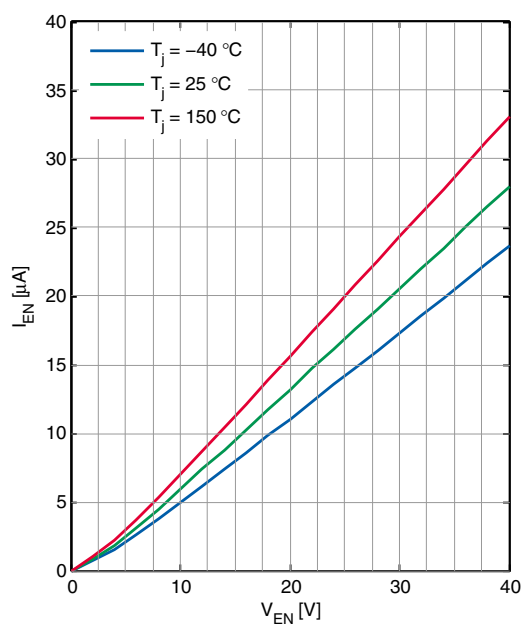
$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified).

Typical values are given at  $T_j = 25^{\circ}\text{C}$ ,  $V_I = 13.5\text{ V}$ .

| Parameter                          | Symbol            | Values |      |      | Unit             | Note or Test Condition       | Number  |
|------------------------------------|-------------------|--------|------|------|------------------|------------------------------|---------|
|                                    |                   | Min.   | Typ. | Max. |                  |                              |         |
| Enable high level input voltage    | $V_{\text{EN,H}}$ | 2      | –    | –    | V                | $V_Q$ settled                | P_5.5.1 |
| Enable low level input voltage     | $V_{\text{EN,L}}$ | –      | –    | 0.8  | V                | $V_Q \leq 0.1\text{ V}$      | P_5.5.2 |
| Enable high level input current    | $I_{\text{EN,H}}$ | –      | –    | 4    | $\mu\text{A}$    | $V_{\text{EN}} = 5\text{ V}$ | P_5.5.3 |
| Enable internal pull-down resistor | $R_{\text{EN}}$   | 1.25   | 2    | 3.5  | $\text{M}\Omega$ | –                            | P_5.5.4 |

## 4.6 Typical performance characteristics enable

Enable input current  $I_{EN}$  versus  
enable input voltage  $V_{EN}$



## 4.7 Reset function

The reset function provides several features:

### Output undervoltage reset

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal may be used to reset a microcontroller during low supply voltage.

### Power-on reset delay time

The power-on reset delay time  $t_{rd}$  allows microcontroller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold  $V_{RT}$  until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time  $t_{rd}$  is defined by an external delay capacitor  $C_D$  connected to pin D charged by the delay capacitor charge current  $I_{D,ch}$  starting from  $V_D = 0$  V.

If the application needs a power-on reset delay time  $t_{rd}$  different from the value given in [Table 10](#), the delay capacitor's value can be derived from the specified value and the desired power-on delay time:

$$C_D = \frac{t_{rd,new}}{t_{rd}} \cdot 100 \text{ nF} \quad (1)$$

with

- $C_D$ : capacitance of the delay capacitor to be chosen
- $t_{rd,new}$ : desired power-on reset delay time
- $t_{rd}$ : power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor's tolerance into consideration.

### Reset reaction time

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction time  $t_{rr}$  considers the internal reaction time  $t_{rr,int}$  and the discharge time  $t_{rr,d}$  defined by the external delay capacitor  $C_D$  (see typical performance graph for details). Hence, the total reset reaction time becomes:

$$t_{rr} = t_{rr,int} + t_{rr,d} \quad (2)$$

with

- $t_{rr}$ : reset reaction time
- $t_{rr,int}$ : internal reset reaction time
- $t_{rr,d}$ : reset discharge

### Optional reset output pull-up resistor $R_{RO,ext}$

The Reset Output RO is an open collector output with an integrated pull-up resistor. If needed, an external pull-up resistor to the output Q can be added. In [Table 10](#) a minimum value for the external resistor  $R_{RO,ext}$  is given.

4 Block description and electrical characteristics

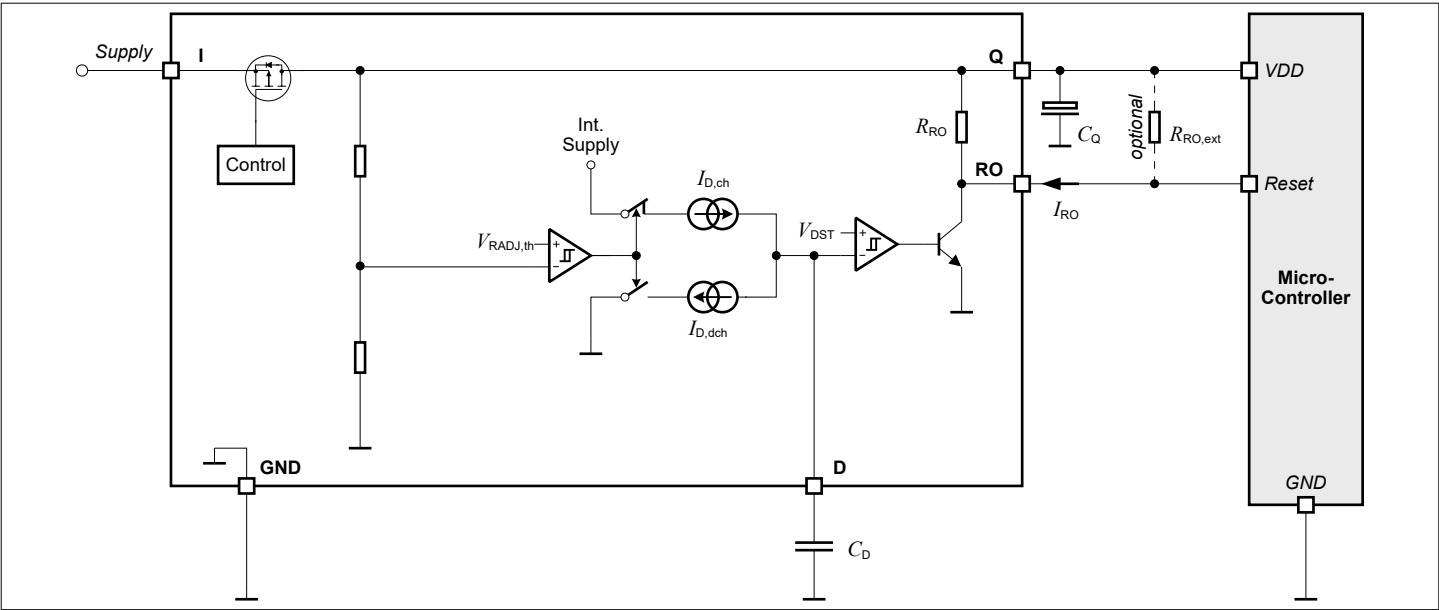


Figure 5 Block diagram reset function

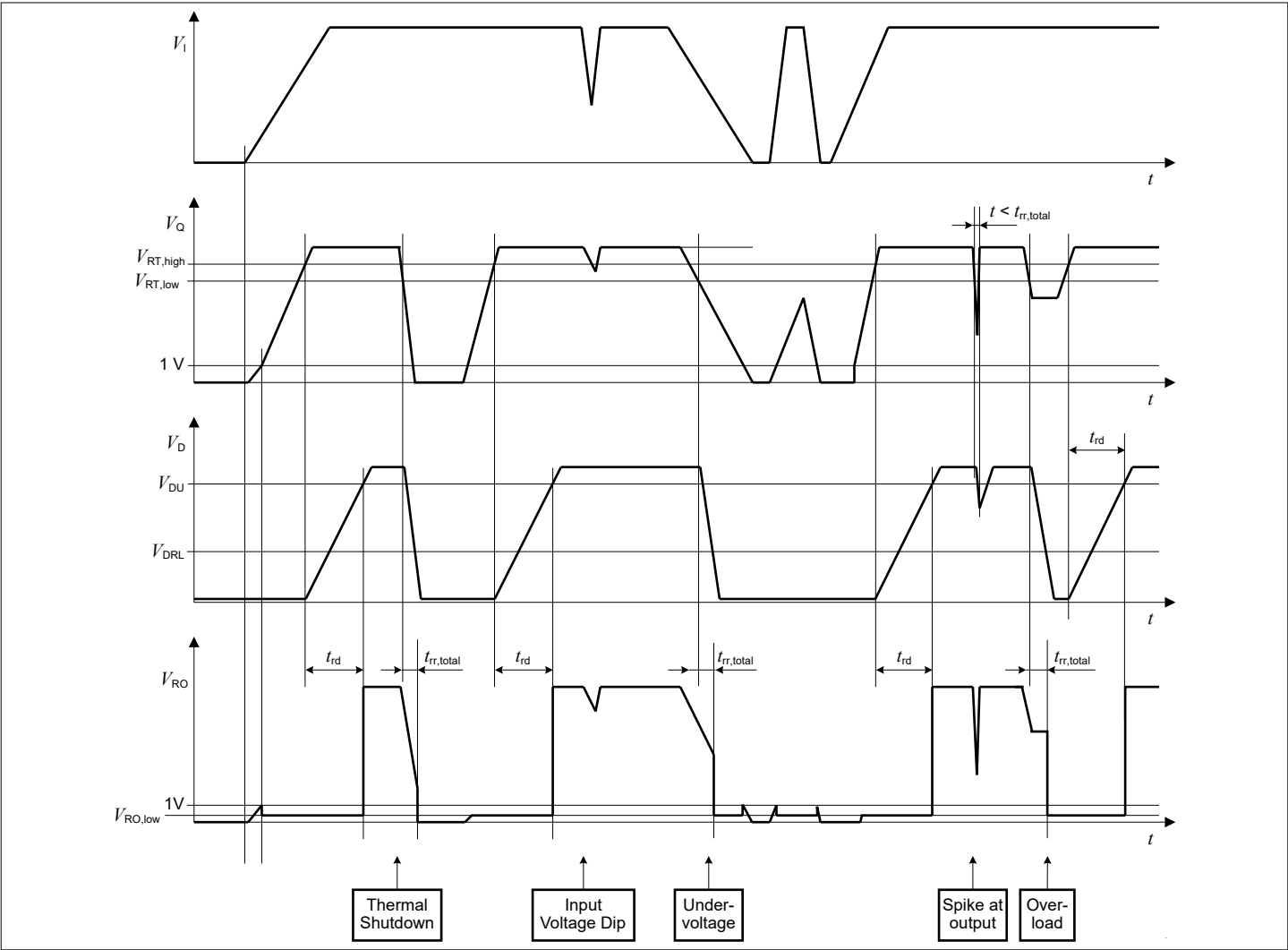


Figure 6 Timing diagram reset

**Table 10 Electrical characteristics reset**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified).

Typical values are given at  $T_j = 25^{\circ}\text{C}$ ,  $V_I = 13.5\text{ V}$ .

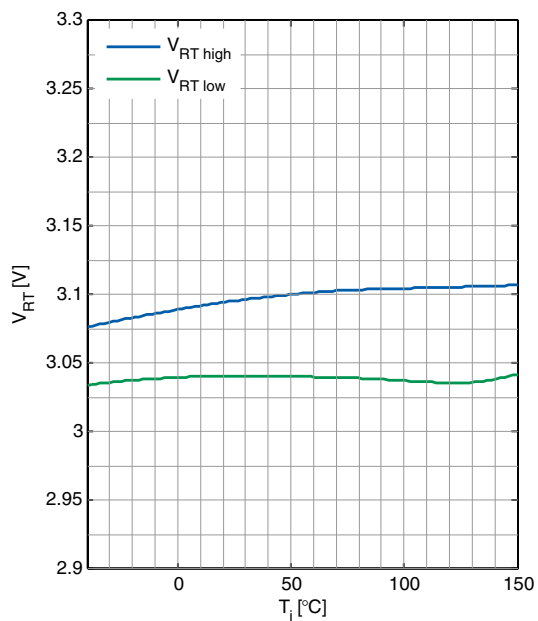
| Parameter   | Symbol         | Values |      |      | Unit          | Note or Test Condition   | Number   |
|---|----------------|--------|------|------|---------------|--|----------|
|   |                | Min.   | Typ. | Max. |               |  |          |
| Output undervoltage reset                                 |                |        |      |      |               |  |          |
| Output undervoltage reset upper switching threshold       | $V_{RT,high}$  | 3.03   | 3.10 | 3.17 | V             | $V_Q$ increasing,<br>$V_{EN} \geq 2.0\text{ V}$                      | P_5.7.1  |
| Output undervoltage reset lower switching threshold       | $V_{RT,low}$   | 2.97   | 3.03 | 3.10 | V             | $V_Q$ decreasing,<br>$V_{EN} \geq 2.0\text{ V}$                      | P_5.7.2  |
| Reset output RO   |                |        |      |      |               |  |          |
| Reset output low voltage                                  | $V_{RO,low}$   | 0      | 0.2  | 0.4  | V             | $1\text{ V} \leq V_Q \leq V_{RT}$ ,<br>$R_{RO} > 4.7\text{ k}\Omega$ | P_5.7.3  |
| Reset output internal pull-up resistor                    | $R_{RO,int}$   | 13     | 20   | 36   | k $\Omega$    | Internally connected to Q  | P_5.7.4  |
| Reset output external pull-up resistor to $V_Q$           | $R_{RO,ext}$   | 4.7    | –    | –    | k $\Omega$    | $1\text{ V} \leq V_Q \leq V_{RT}$ ,<br>$V_{RO} \leq 0.4\text{ V}$    | P_5.7.5  |
| Reset delay timing  |                |        |      |      |               |  |          |
| Power on reset delay time                                 | $t_{rd}$       | 17     | 25   | 37   | ms            | $C_D = 100\text{ nF}$<br>Calculated value                            | P_5.7.6  |
| Upper delay switching threshold                           | $V_{DU}$       | –      | 0.9  | –    | V             | –  | P_5.7.7  |
| Lower output undervoltage reset upper switching threshold | $V_{DL}$       | –      | 0.6  | –    | V             | –  | P_5.7.8  |
| Delay capacitor charge current                            | $I_{D,ch}$     | –      | 3.6  | –    | $\mu\text{A}$ | $V_D = 1\text{ V}$   | P_5.7.9  |
| Delay capacitor discharge current                         | $I_{D,dch}$    | –      | 250  | –    | mA            | $V_D = 1\text{ V}$   | P_5.7.10 |
| Delay capacitor discharge time                            | $t_{rr,d}$     | –      | 2    | 4    | $\mu\text{s}$ | $C_D = 100\text{ nF}$<br>Calculated value                            | P_5.7.11 |
| Internal reset reaction time                              | $t_{rr,int}$   | –      | 8    | 14   | $\mu\text{s}$ | <sup>1)</sup> $C_D = 0\text{ nF}$                                    | P_5.7.12 |
| Reset reaction time                                       | $t_{rr,total}$ | –      | 10   | 18   | $\mu\text{s}$ | $C_D = 100\text{ nF}$<br>Calculated value                            | P_5.7.13 |

1) Parameter not subject to production test; specified by design.

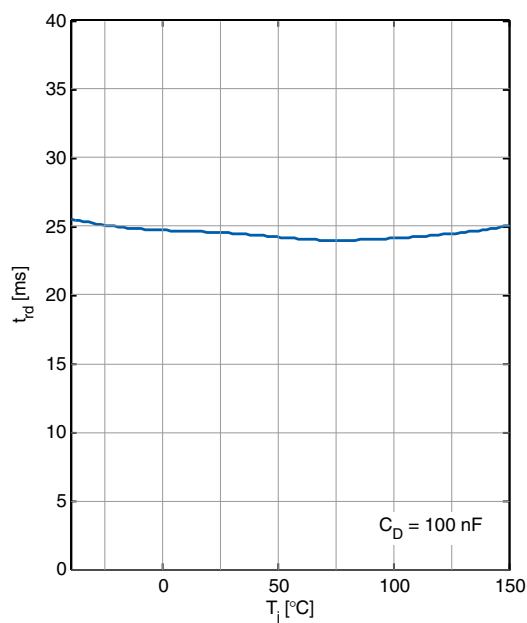
## 4.8 Typical performance characteristics Reset

### Typical performance characteristics

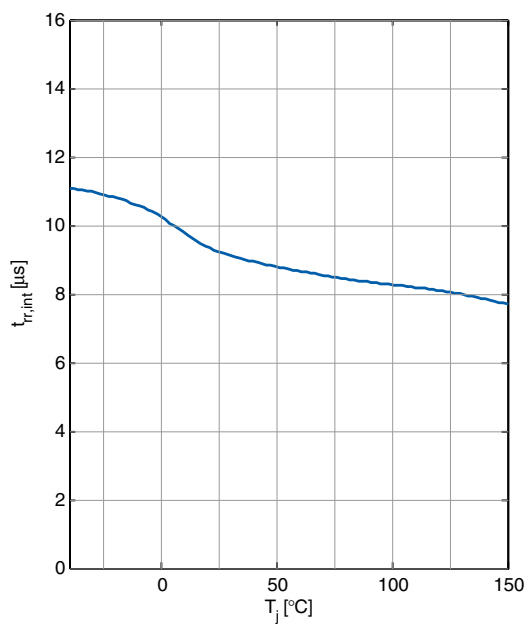
Undervoltage reset threshold  $V_{RT}$  versus  
 Junction temperature  $T_j$



Power On reset delay time  $t_{rd}$  versus  
 Junction temperature  $T_j$



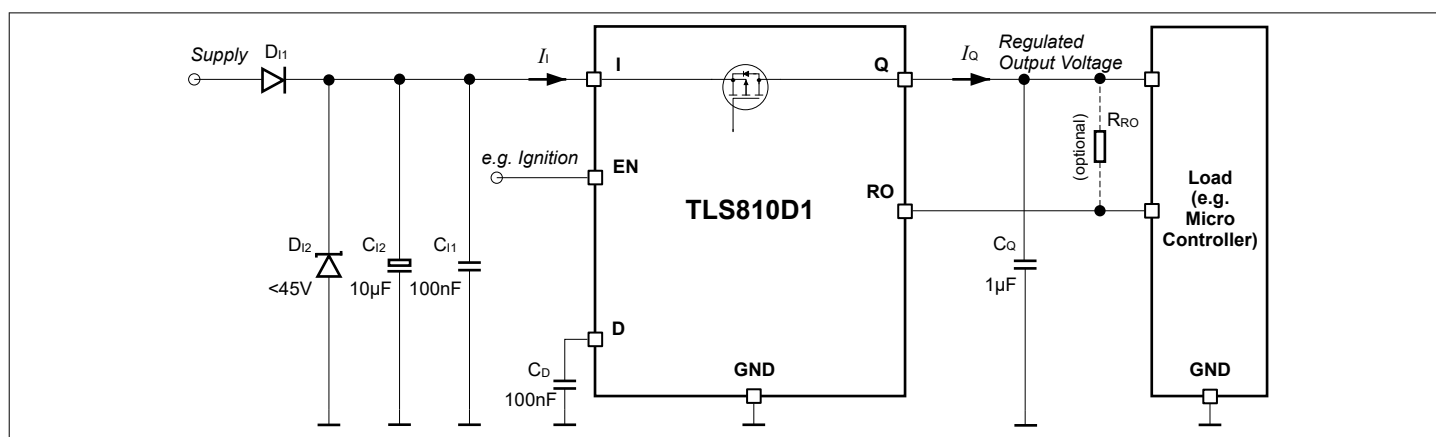
Internal reset reaction time  $t_{rr,int}$  versus  
 Junction temperature  $T_j$



## 5 Application information

**Note:** The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

### 5.1 Application diagram



**Figure 7** Application diagram

## 5.2 Selection of external components

### 5.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to overvoltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

### 5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in [Functional range](#). The graph, [Output capacitor equivalent series resistance ESR\( \$C\_Q\$ \) versus output current  \$I\_Q\$](#)  shows the stable operation range of the device.

TLS810D1 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (3)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA, \max} = \frac{T_{j, \max} - T_a}{P_D} \quad (4)$$

with

- $T_{j, \max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [Thermal resistance](#).

#### Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 3.3 \text{ V}$$

$$I_Q = 70 \text{ mA}$$

$$T_a = 105^\circ\text{C}$$

Calculation of  $R_{thJA, \max}$ :

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$

$$= (13.5 \text{ V} - 3.3 \text{ V}) \times 70 \text{ mA} + 13.5 \text{ V} \times 0.012 \text{ mA}$$

$$= 0.714 \text{ W}$$

$$R_{thJA, \max} = (T_{j, \max} - T_a) / P_D$$

$$= (150^\circ\text{C} - 105^\circ\text{C}) / 0.714 \text{ W}$$

$$= 63.03 \text{ K/W}$$

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 63.03 K/W. According to [Thermal resistance](#), the 2s2p board can be used. Using the FR4 1s0p board with PG-DSO-8 EP, at least 600 mm<sup>2</sup> heatsink area is required.

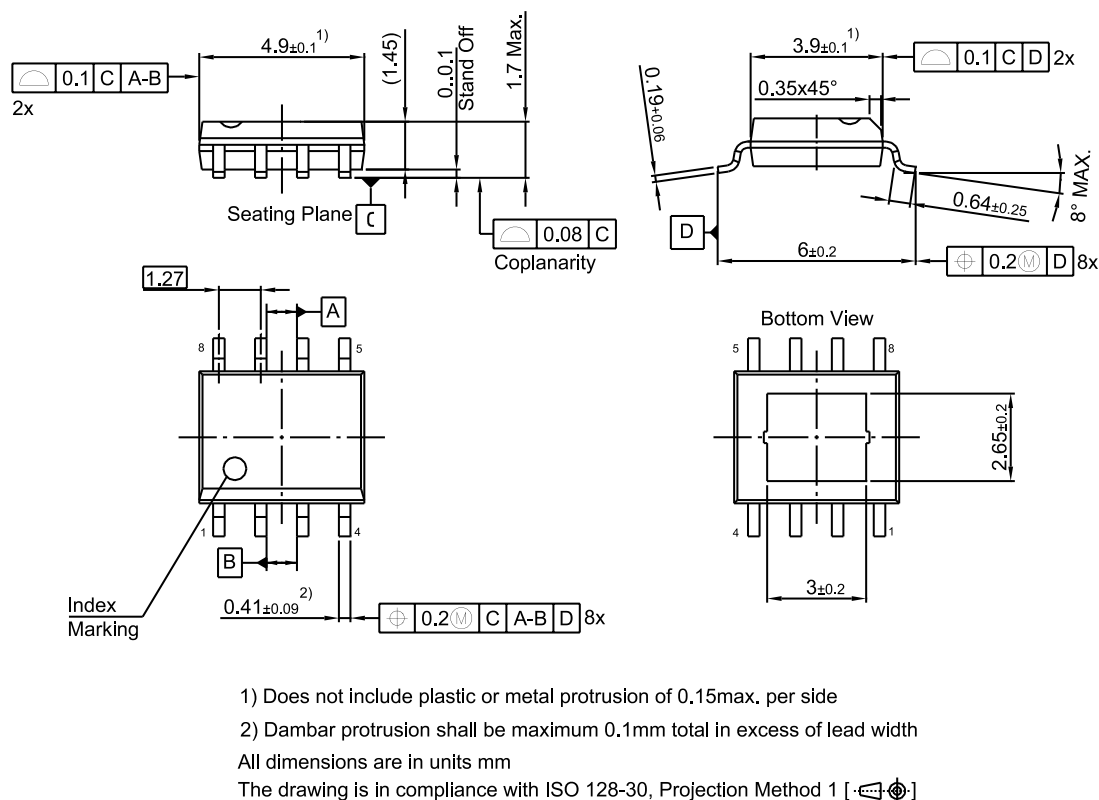
## **5.4 Reverse polarity protection**

TLS810D1 is not self protected against reverse polarity faults. To protect the device against negative supply voltage, an external reverse polarity diode is needed, as shown in [Figure 7](#). The absolute maximum ratings of the device as specified in [Chapter 3.1](#) must be respected.

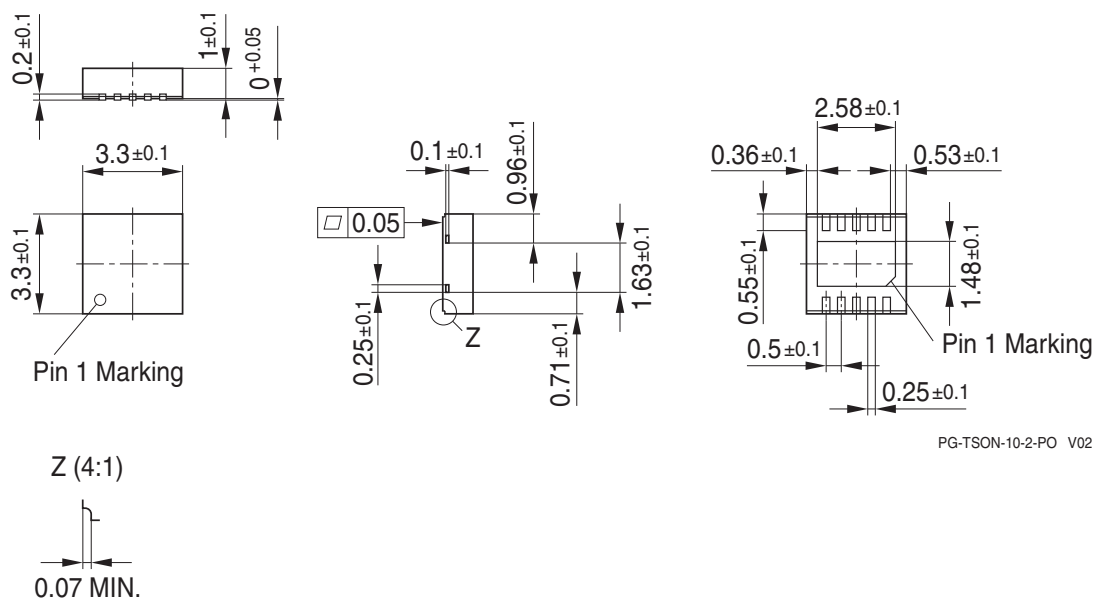
## **5.5 Further application information**

For further information you may contact <http://www.infineon.com>

## 6 Package outlines



**Figure 8 PG-DSO-8 EP**



**Figure 9 PG-TSON-10<sup>1)</sup>**

<sup>1)</sup> Dimensions in mm

**Green product (RoHS-compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website: [www.infineon.com/packages](http://www.infineon.com/packages)

## 7 Revision History

| Revision | Date       | Changes                               |
|----------|------------|---------------------------------------|
| 1.11     | 2025-02-07 | Editorial changes and template update |
| 1.10     | 2016-12-20 | Template updated                      |
| 1.00     | 2016-10-19 | Datasheet - Initial version           |

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