

## DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Check for Samples: [SN74LVC2G126-EP](#)

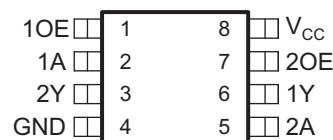
### FEATURES

- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.8 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military ( $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DCU PACKAGE  
(TOP VIEW)



### DESCRIPTION

This dual bus buffer gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G126 is a dual bus driver/line driver with 3-state outputs. The outputs are disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

$T_J$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
$-55^\circ\text{C}$ to $125^\circ\text{C}$	VSSOP - DCU	Tape of 250	CLVC2G126MDCUTEP	CEPR	V62/14604-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Function Table  
(Each Buffer)

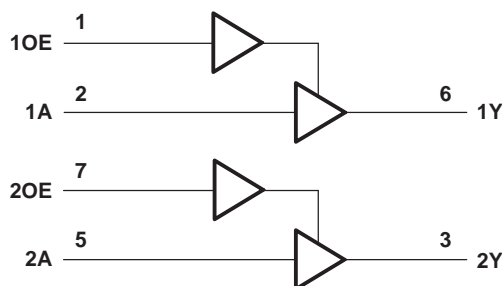
INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z



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**Logic Diagram (Positive Logic)****ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage range	-0.5	6.5	V
$V_I$ Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$ Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$ Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$ Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$ Output clamp current	$V_O < 0$		-50 mA
$I_O$ Continuous output current			±50 mA
Continuous current through $V_{CC}$ or GND			±100 mA
$T_J$ Absolute maximum junction temperature range	-55	150	°C
$T_{stg}$ Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		SN74LVC2G126-EP	UNITS
		DCU	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	204.3	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	78	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	83	
$\Psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	7.6	
$\Psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	82.6	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\Psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\Psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–4	mA
		V <sub>CC</sub> = 2.3 V		–8	
		V <sub>CC</sub> = 3 V		–16	
		V <sub>CC</sub> = 4.5 V		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
		V <sub>CC</sub> = 4.5 V		24	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>J</sub>	Operating virtual junction temperature		–55	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

These specifications apply for  $-55^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$		$I_{OH} = -100\ \mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$			V
		$I_{OH} = -4\ \text{mA}$	1.65 V	1.2			
		$I_{OH} = -8\ \text{mA}$	2.3 V	1.9			
		$I_{OH} = -16\ \text{mA}$	3 V	2.4			
		$I_{OH} = -24\ \text{mA}$		2.3			
		$I_{OH} = -32\ \text{mA}$	4.5 V	3.8			
$V_{OL}$		$I_{OL} = 100\ \mu\text{A}$	1.65 V to 5.5 V			0.1	V
		$I_{OL} = 4\ \text{mA}$	1.65 V			0.45	
		$I_{OL} = 8\ \text{mA}$	2.3 V			0.3	
		$I_{OL} = 16\ \text{mA}$	3 V			0.4	
		$I_{OL} = 24\ \text{mA}$				0.55	
		$I_{OL} = 32\ \text{mA}$	4.5 V			0.55	
$I_I$	A or OE inputs	$V_I = 5.5\ \text{V}$ or GND	0 to 5.5 V			$\pm 5$	$\mu\text{A}$
$I_{off}$		$V_I$ or $V_O = 5.5\ \text{V}$	0			$\pm 10$	$\mu\text{A}$
$I_{OZ}$		$V_O = 0$ to 5.5 V	3.6 V			10	$\mu\text{A}$
$I_{CC}$		$V_I = 5.5\ \text{V}$ or GND, $I_O = 0$	1.65 V to 5.5 V			10	$\mu\text{A}$
$\Delta I_{CC}$		One input at $V_{CC} - 0.6\ \text{V}$ , Other inputs at $V_{CC}$ or GND	3 V to 5.5 V			500	$\mu\text{A}$
$C_I$	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		3.5		pF
	Control inputs				4		
$C_O$		$V_O = V_{CC}$ or GND	3.3 V		6.5		pF

(1) All typical values are at  $V_{CC} = 3.3\ \text{V}$ ,  $T_J = 25^{\circ}\text{C}$ .

## SWITCHING CHARACTERISTICS

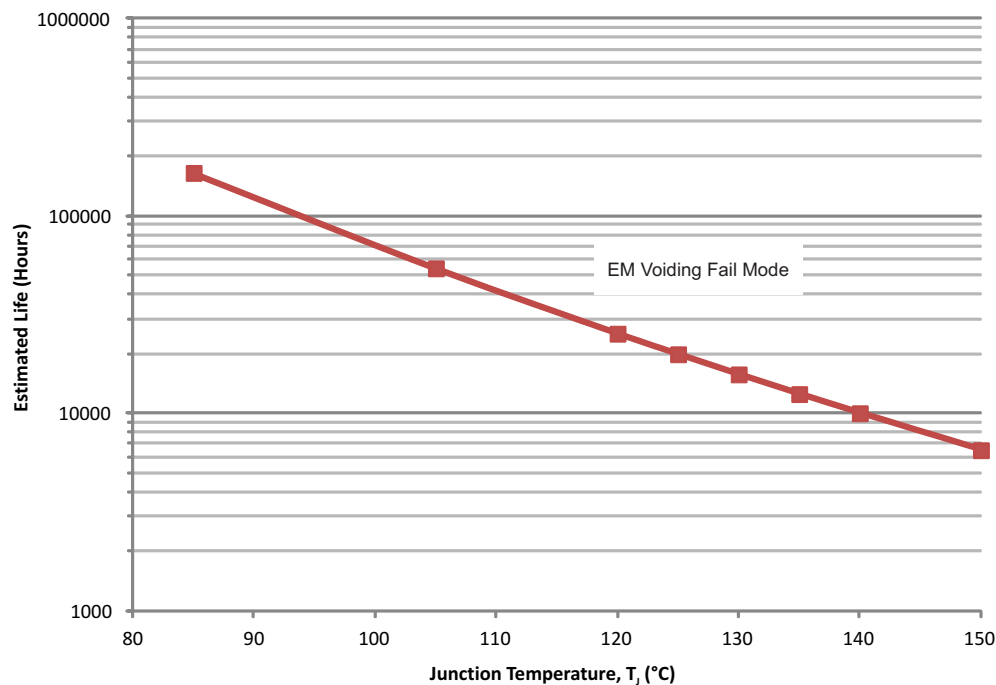
These specifications apply for  $-55^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\ \text{V} \pm 0.15\ \text{V}$		$V_{CC} = 2.5\ \text{V} \pm 0.2\ \text{V}$		$V_{CC} = 3.3\ \text{V} \pm 0.3\ \text{V}$		$V_{CC} = 5\ \text{V} \pm 0.5\ \text{V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	3.5	15.2	1.7	8.6	1.4	6.8	1	5.5	ns
$t_{en}$	OE	Y	3.5	15.2	1.7	8.6	1.5	6.8	1	5.5	ns
$t_{dis}$	OE	Y	1.7	12.6	1	5.7	1	4.5	0.1	3.3	ns

## OPERATING CHARACTERISTICS

$T_J = 25^{\circ}$

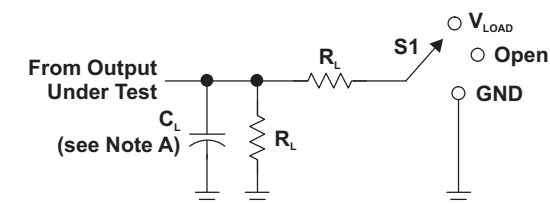
PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\ \text{V}$	$V_{CC} = 2.5\ \text{V}$	$V_{CC} = 3.3\ \text{V}$	$V_{CC} = 5\ \text{V}$	UNIT
				TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$f = 10\ \text{MHz}$	19	19	20	22	pF
		Outputs disabled		2	2	2	3	



- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

**Figure 1. SN74LVC2G126-EP Operating Life Derating Chart**

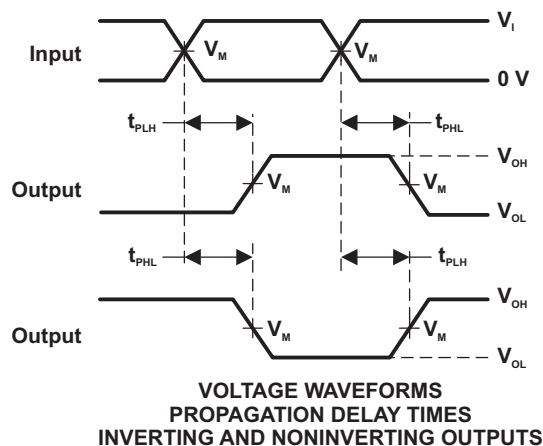
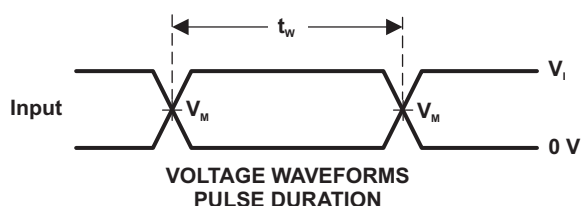
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_f/t_r$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC2G126MDCUTEP	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CEPR	<a href="#">Samples</a>
V62/14604-01XE	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CEPR	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC2G126-EP :**

- Catalog: [SN74LVC2G126](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

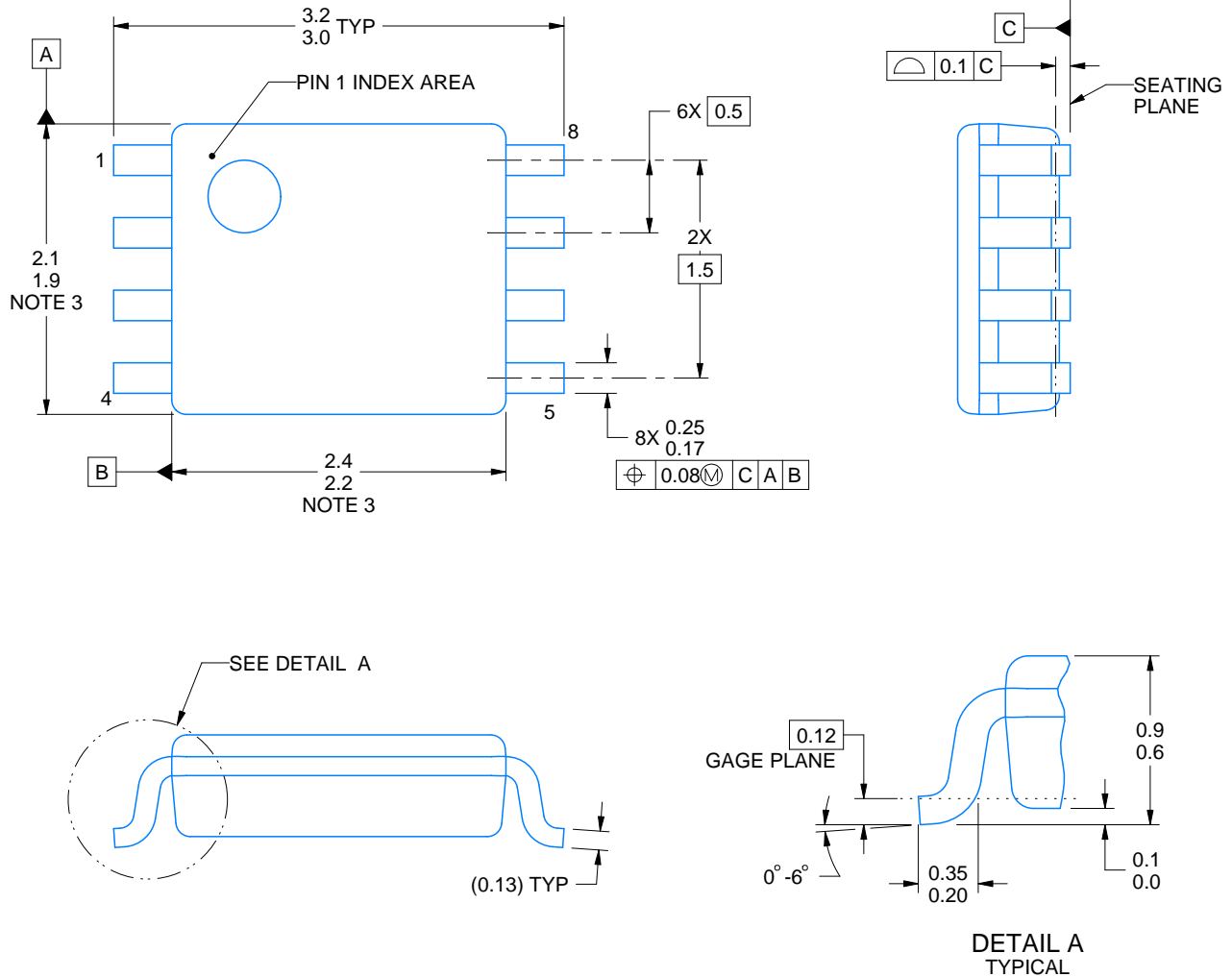
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC2G126MDCUTEP	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC2G126MDCUTEP	VSSOP	DCU	8	250	202.0	201.0	28.0



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## NOTES:

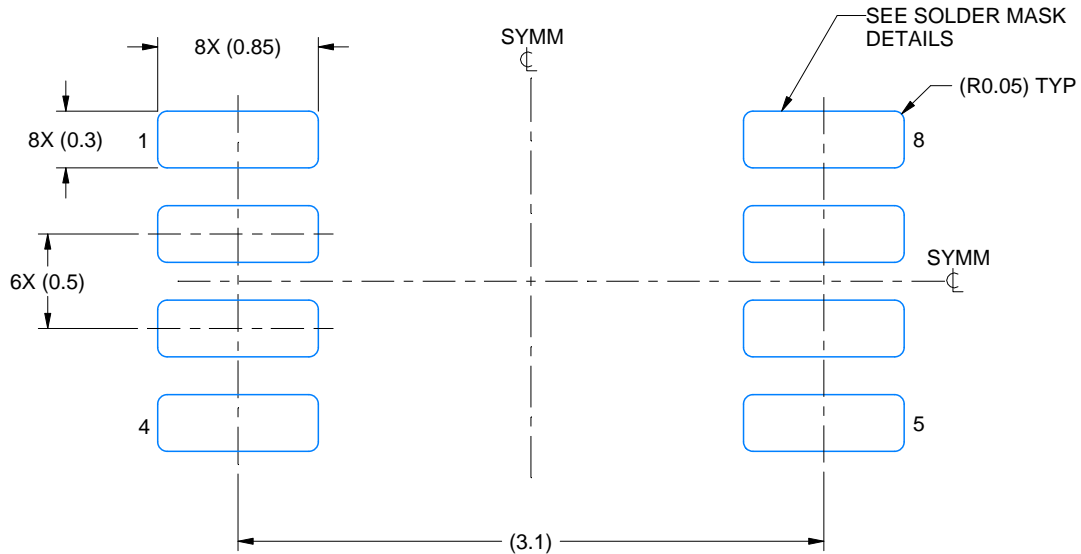
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

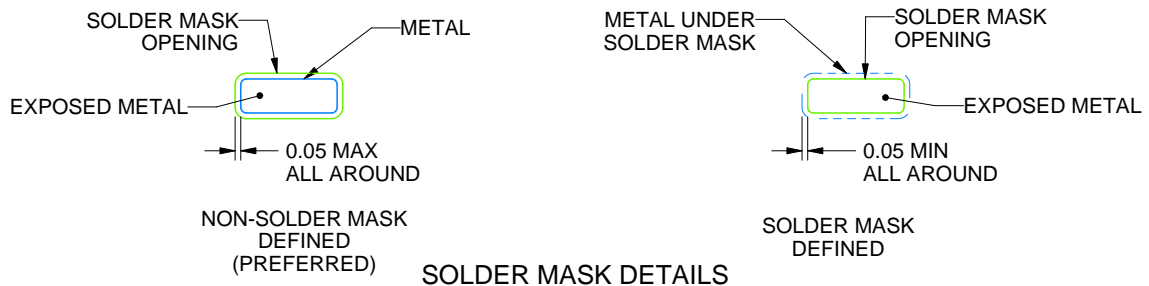
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

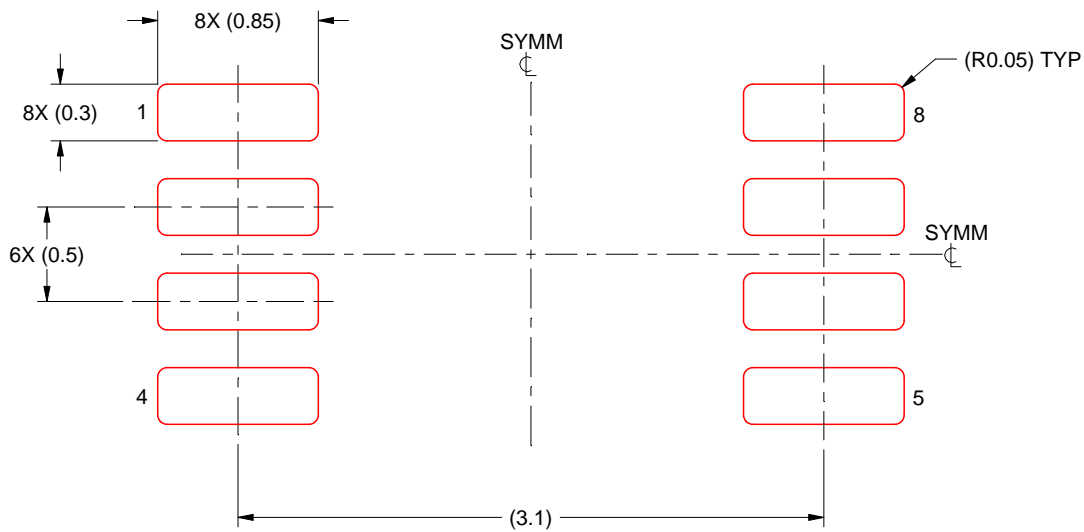
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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