**ADVANCED**

# GT24C02

# 2-Wire

# 2Kb Serial EEPROM

# Table of Content

# 1 FEATURES

- Two-Wire Serial Interface, $I^2C^{TM}$ Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - Vcc = 1.8V to 5.5V
- Speed: 400 KHz (1.8V) and 1 MHz (2.5V~5.5V)
- Standby current: 1 μA (max.), 1.8V
- Operating current: 3 mA (max.), 5.5V
- Hardware Data Protection
  - Write Protect Pin
- Sequential & Random Read Features
- Memory organization: 2Kb (256 x 8)
- Page Size: 16 bytes
- Page write mode
  - Partial page writes allowed
- Self timed write cycle: 5 ms (max.)
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- Industrial grade
- Packages: PDIP, SOIC/SOP, TSSOP, MSOP and UDFN
- Lead-free, RoHS, Halogen free, Green

# 2 DESCRIPTION

The GT24C02 is an industrial standard electrically erasable programmable read only memory (EEPROM) device that utilizes the industrial standard 2-wire interface for communications. The GT24C02 contains a memory array of 2K bits (256x8), which is organized in 16-byte per page.

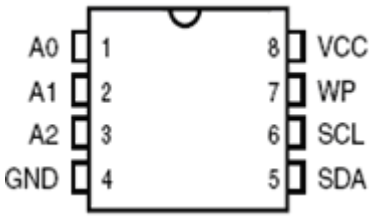
The EEPROM operates in a wide voltage range from 1.8V to 5.5V, which fits most application. The product provides low-power operations and low standby current. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin PDIP, SOIC/SOP, TSSOP, MSOP and UDFN.

The GT24C02 is compatible to the standard 2-wire bus protocol. The simple bus consists of Serial Clock (SCL) and Serial Data (SDA) signals. Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this GT24C02. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The GT24C02 also has a Write Protect function via WP pin to cease from overwriting the data stored inside the memory array.

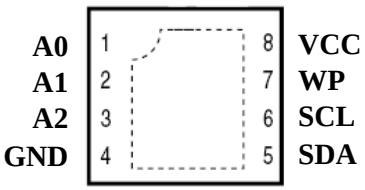
In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage ($V_{CC}$) has reached an acceptable stable level above the reset threshold voltage. Once $V_{CC}$ passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once $V_{CC}$ drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is not recommended to send an command until the Vcc reaches its operating level.

# 3 PIN CONFIGURATION

**8-Pin PDIP, SOIC/SOP, MSOP and TSSOP**




**8-Lead UDFN**




## Pin Definitions

| Name | Definition |
|---|---|
| **A0** | Address Input |
| **A1** | Address Input |
| **A2** | Address Input |
| **SDA** | Serial Address/Data I/O |
| **SCL** | Serial Clock Input |
| **WP** | Write Protect Input |
| **$V_{CC}$** | Power Supply |
| **GND** | Ground |

# 4 PIN DESCRIPTIONS

**SCL**

This input clock pin is used to synchronize the data transfer to and from the device.

**SDA**

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

**A0, A1, A2**

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

**WP**

WP is the Write Protect pin. While the WP pin is connected to the power supply of GT24C02, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

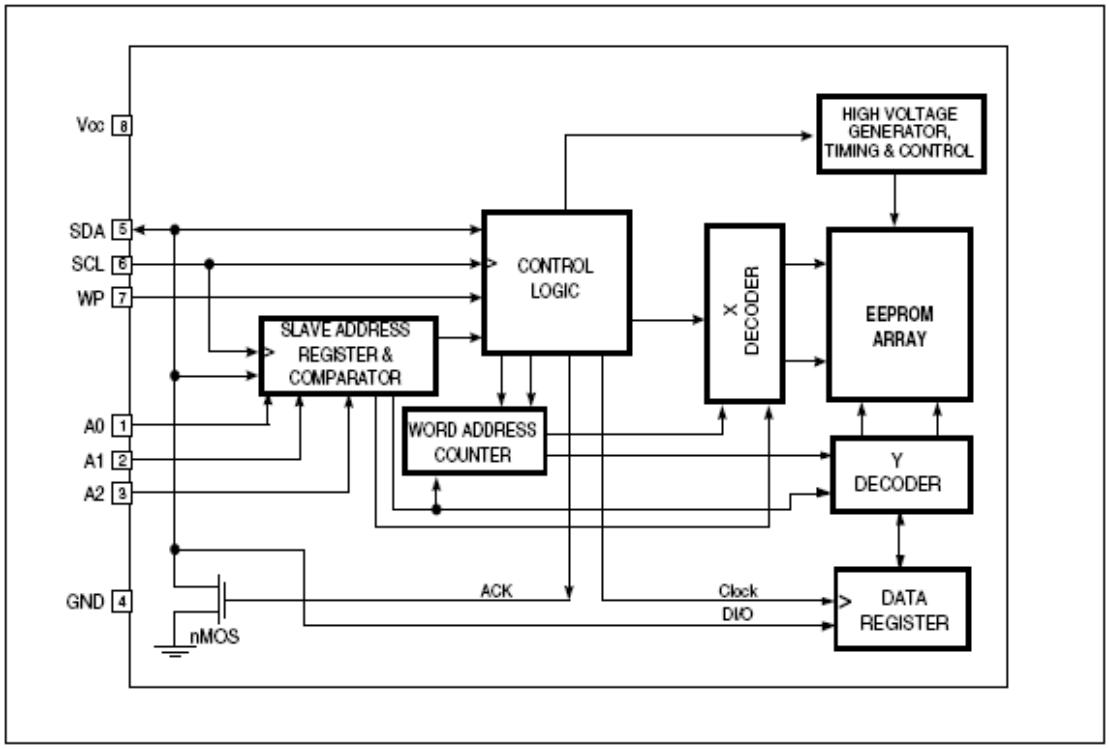
**Vcc**

Supply voltage

**GND**

Ground of supply voltage

# 5 BLOCK DIAGRAM



# 6 DEVICE OPERATION

The GT24C02 serial interface supports communications using industrial standard 2-wire bus protocol, such as $I^2C$.

## 2-WIRE BUS

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The GT24C02 is the Slave device.

### The Bus Protocol:

Data transfer may be initiated only when the bus is not busy.

During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

### Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

### Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

### Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

### Reset

The GT24C02 contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

### Standby Mode

While in standby mode, the power consumption is minimal. The GT24C02 enters into standby mode during one of the following conditions: a) After Power-up, while no Opcode is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

## DEVICE ADDRESSING

The Master begins a transmission on by sending a Start condition, and then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Fig. 5.

The four most significant bits of the Slave address are fixed (1010) for GT24C02.

The next three bits, A0, A1 and A2, of the Slave address are specifically related to EEPROM. Up to eight GT24C02 units can be connected to the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, GT24C02, will respond with ACK on the SDA line. Then GT24C02 will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The GT24C02 then prepares for a Read or Write operation by monitoring the bus.

## WRITE OPERATION

### Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT24C02. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT24C02 acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

### Page Write

The GT24C02 is capable of 16-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 15 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the four lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 16 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 16 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT24C02 in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

### Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT24C02 initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT24C02 has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

## READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

### Current Address Read

The GT24C02 contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to

the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the GT24C02 discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

## Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT24C02 acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

## Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT24C02 sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT24C02. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

# 7 TIMING DIAGRAMS

**Fig. 1: Typical System Bus Configuration**

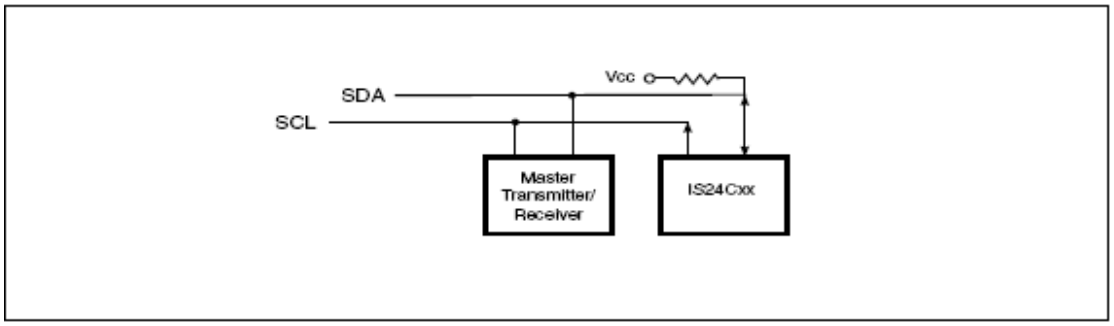



**Fig. 2: output Acknowledge**

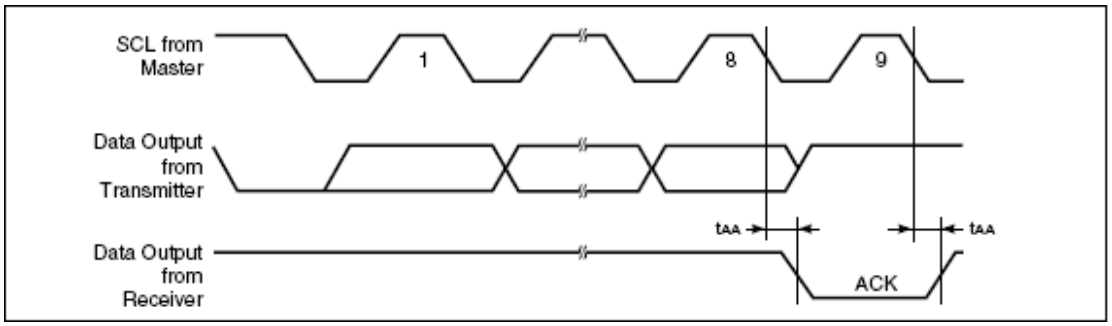



**Fig. 3: Start and Stop Conditions**

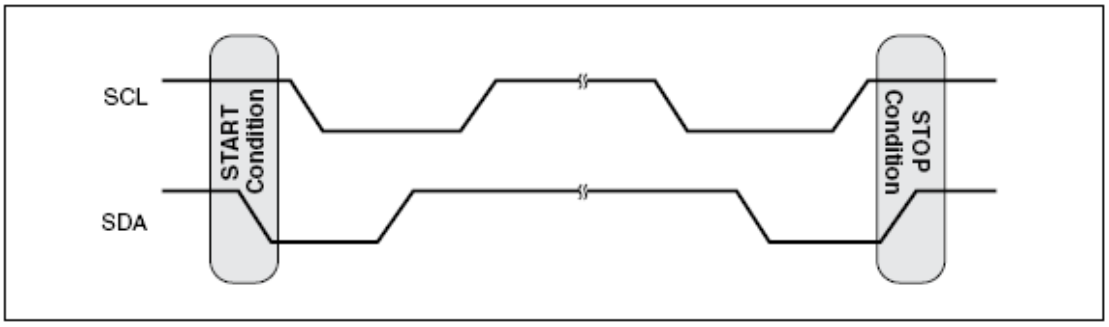


**Fig. 4: Data Validity Protocol**

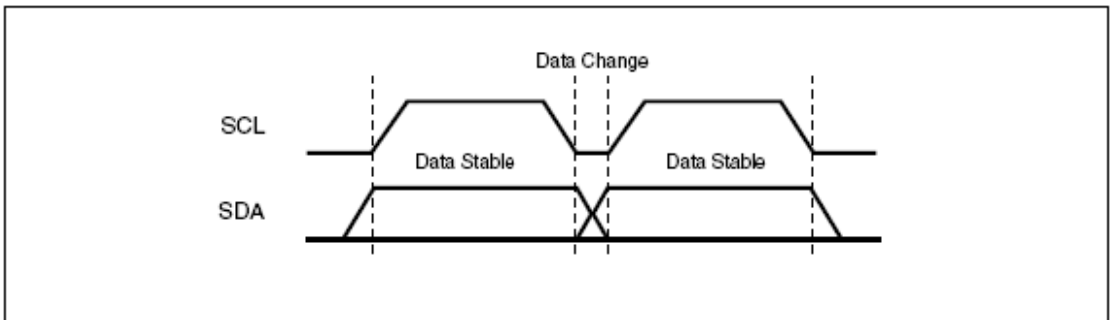



**Fig. 5: Slave Address**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R / $\overline{W}$ |

**Fig. 6: Byte Write**

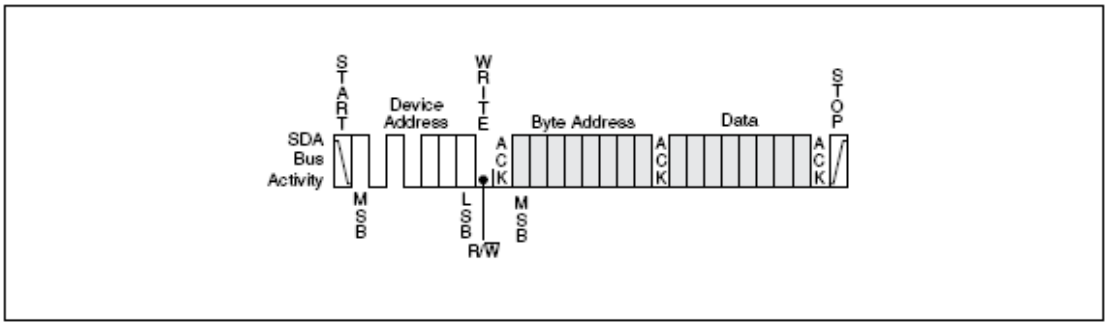



**Fig. 7: Page Write**

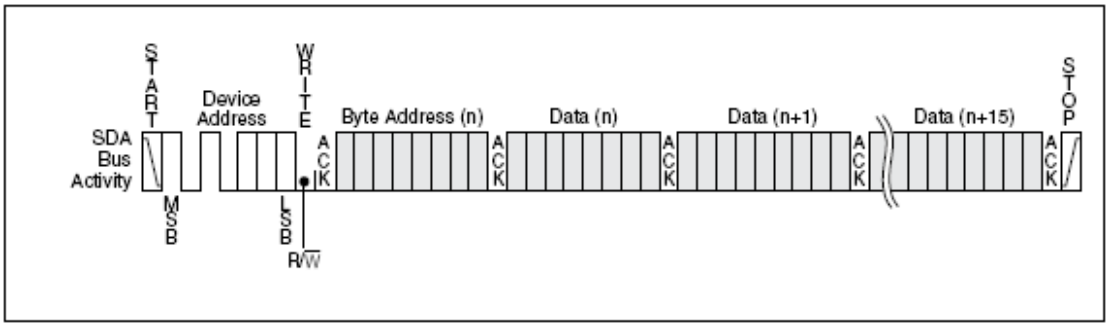


**Fig. 8: Current Address Read**

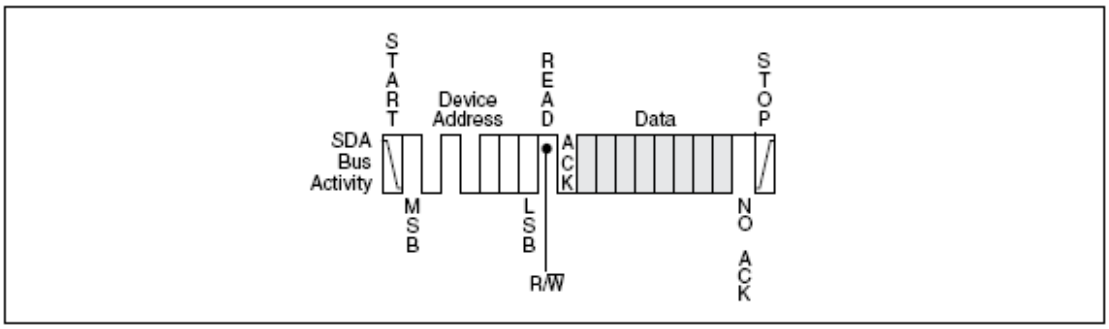



**Fig. 9: Random Address Read**

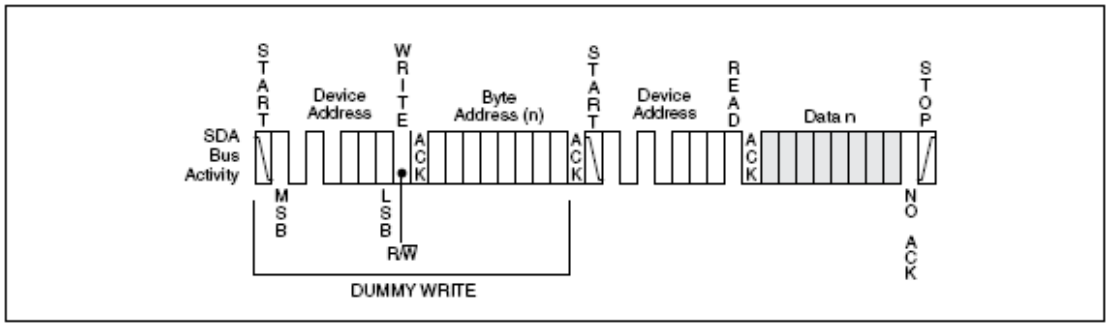
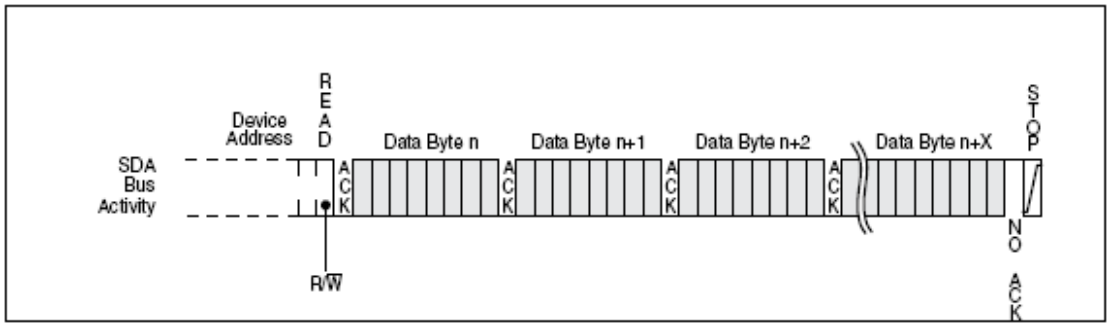



**Fig. 10: Sequential Read**



## AC Timing

**Fig. 11: Bus Timing**

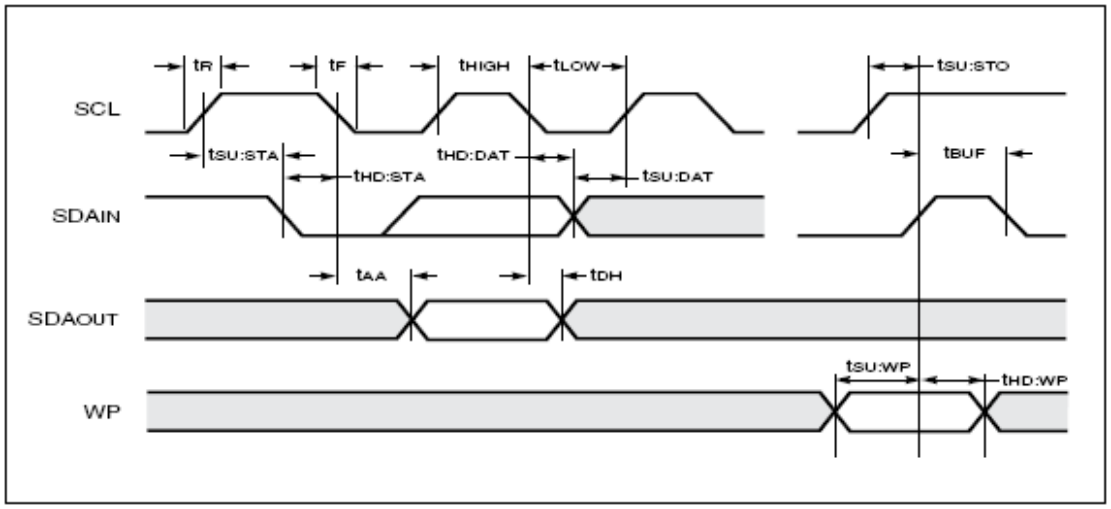
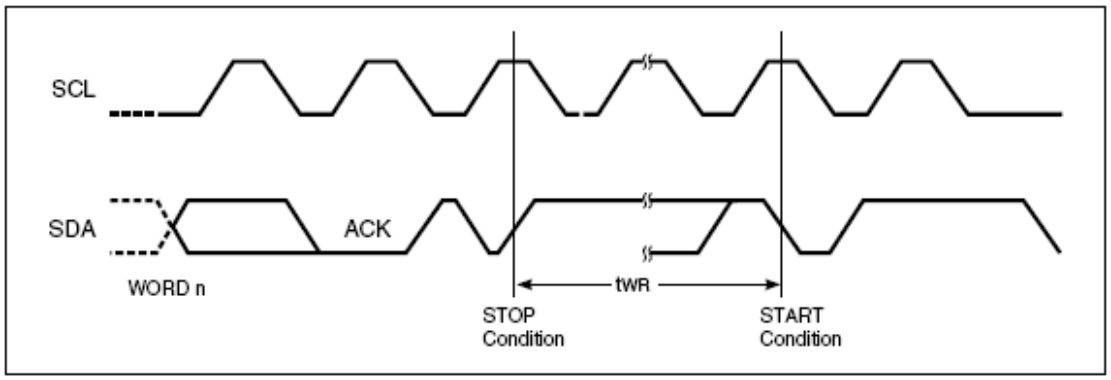



**Fig. 12: Write Cycle Timing**



# 8 ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_S$ | Supply Voltage | -0.5 to + 6.5 | V |
| $V_P$ | Voltage on Any Pin | –0.5 to Vcc + 0.5 | V |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | Output Current | 5 | mA |

**Notes:**
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# OPERATING RANGE

| Range | Ambient Temperature ($T_A$) | $V_{CC}$ |
|---|---|---|
| **Industrial** | –40°C to +85°C | 1.8V to 5.5V |

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

## CAPACITANCE (1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{I/O}$ | Input /Output Capacitance | $V_{I/O}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, Vcc = 5.0V.

# 9 DC ELECTRICAL CHARACTERISTICS

**Industrial**: $T_A$ = –40°C to +85°C, Vcc = 1.8V ~ 5.5V

| Symbol | Parameter [1] | Vcc | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | | 1.8 | 5.5 | V |
| $V_{IH}$ | Input High Voltage (SDA, SCL, WP) | | | 0.7*$V_{CC}$ | $V_{CC}$+1 | V |
| $V_{IL}$ | Input Low Voltage (SDA, SCL, WP) | | | -1 | 0.3* $V_{CC}$ | V |
| $I_{LI}$ | Input Leakage Current (SDA, SCL, WP, A0, A1 & A2) | 5V | $V_{IN}$ = 0V ~ $V_{CC}$, standby mode | -- | 2 | µA |
| $I_{LO}$ | Output Leakage Current | 5V | $V_{OUT}$ = 0V~$V_{CC}$, SDA in Hi-Z | -- | 2 | µA |
| $V_{OL1}$ | Output Low Voltage | 1.8V | $I_{OL}$ = 0.15 mA | — | 0.2 | V |
| $V_{OL2}$ | Output Low Voltage | 3V | $I_{OL}$ = 2.1 mA | — | 0.4 | V |
| $I_{SB1}$ | Standby Current | 1.8V | $V_{IN}$ = Vcc or GND | — | 1 | µA |
| | | 2.5V | $V_{IN}$ = Vcc or GND | — | 1 | µA |
| | | 5.5V | $V_{IN}$ = Vcc or GND | — | 3 | µA |
| $I_{CC1}$ | Read Current | 1.8V | Read at 400 KHz | — | 0.8 | mA |
| | | 4.5V | Read at 1 MHz | — | 2 | mA |
| | | 5.5V | Read at 1 MHz | — | 2 | mA |
| $I_{CC2}$ | Write Current | 1.8V | Write at 400 KHz | — | 1 | mA |
| | | 4.5V | Write at 1 MHz | — | 3 | mA |
| | | 5.5V | Write at 1 MHz | — | 3 | mA |

**Notes:** [1] The parameters are characterized but not 100% tested.

# 10 AC ELECTRICAL CHARACTERISTICS

## AC Characteristics - Industrial

$T_A$ = –40°C to +85°C, Supply voltage = 1.8V to 5.5V

| Symbol | Parameter [1] [2] | 1.8V ≤ Vcc < 2.5V | | 2.5V ≤ Vcc < 4.5V | | 4.5V ≤ Vcc ≤ 5.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $F_{SCL}$ | SCK Clock Frequency | | 400 | | 1000 | | 1000 | KHz |
| $T_{LOW}$ | Clock Low Period | 1200 | — | 400 | — | 400 | — | ns |
| $T_{HIGH}$ | Clock High Period | 600 | — | 400 | — | 400 | — | ns |
| $T_R$ | Rise Time (SCL and SDA) | — | 300 | — | 300 | — | 300 | ns |
| $T_F$ | Fall Time (SCL and SDA) | — | 300 | — | 100 | — | 100 | ns |
| $T_{SU:STA}$ | Start Condition Setup Time | 500 | — | 200 | — | 200 | — | ns |
| $T_{SU:STO}$ | Stop Condition Setup Time | 500 | — | 200 | — | 200 | — | ns |
| $T_{HD:STA}$ | Start Condition Hold Time | 500 | — | 200 | — | 200 | — | ns |
| $T_{SU:DAT}$ | Data In Setup Time | 100 | — | 40 | — | 40 | — | ns |
| $T_{HD:DAT}$ | Data In Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $T_{AA}$ | Clock to Output Access time (SCL Low to SDA Data Out Valid) | 100 | 900 | 50 | 400 | 50 | 400 | ns |
| $T_{DH}$ | Data Out Hold Time (SCL Low to SDA Data Out Change) | 100 | — | 50 | — | 50 | — | ns |
| $T_{WR}$ | Write Cycle Time | — | 5 | — | 5 | — | 5 | ms |
| $T_{BUF}$ | Bus Free Time Before New Transmission | 1000 | — | 400 | — | 400 | — | ns |
| $T_{SU:WP}$ | WP pin Setup Time | 1000 | — | 400 | — | 400 | | ns |
| $T_{HD:WP}$ | WP pin Hold Time | 1000 | — | 400 | — | 400 | — | ns |
| T | Noise Suppression Time | — | 100 | — | 50 | — | 50 | ns |

**Notes:** [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

$R_L$ (connects to Vcc): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.8V)

$C_L$ = 100 pF

Input pulse voltages: 0.3*Vcc to 0.7*Vcc

Input rise and fall times: ≤ 50 ns

Timing reference voltages: half Vcc level

# 11 ORDERING INFORMATION

**Industrial Grade: -40°C to +85°C, Lead-free**

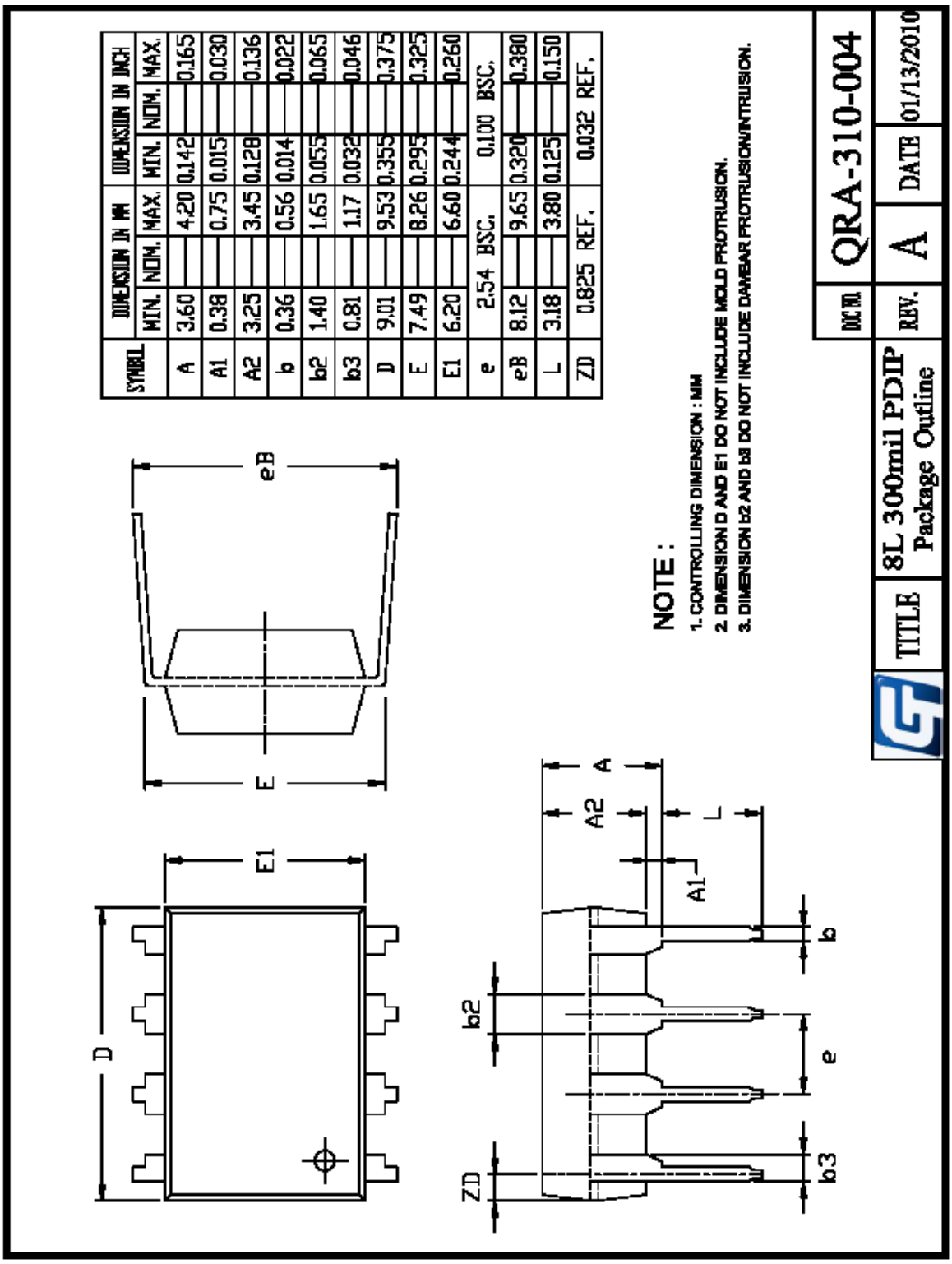
| Voltage Range | Part Number* | Package (8-pin)* |
|---|---|---|
| 1.8V to 5.5V | GT24C02-2GLI-TR | 150-mil SOIC/SOP (JEDEC) |
| | GT24C02-2PLI | 300-mil PDIP |
| | GT24C02-2ZLI-TR | 3 x 4.4 mm TSSOP |
| | GT24C02-2SLI-TR | 3 x 3 mm MSOP |
| | GT24C02-2UDLI-TR | 2 x 3 x 0.55 mm UDFN |

*

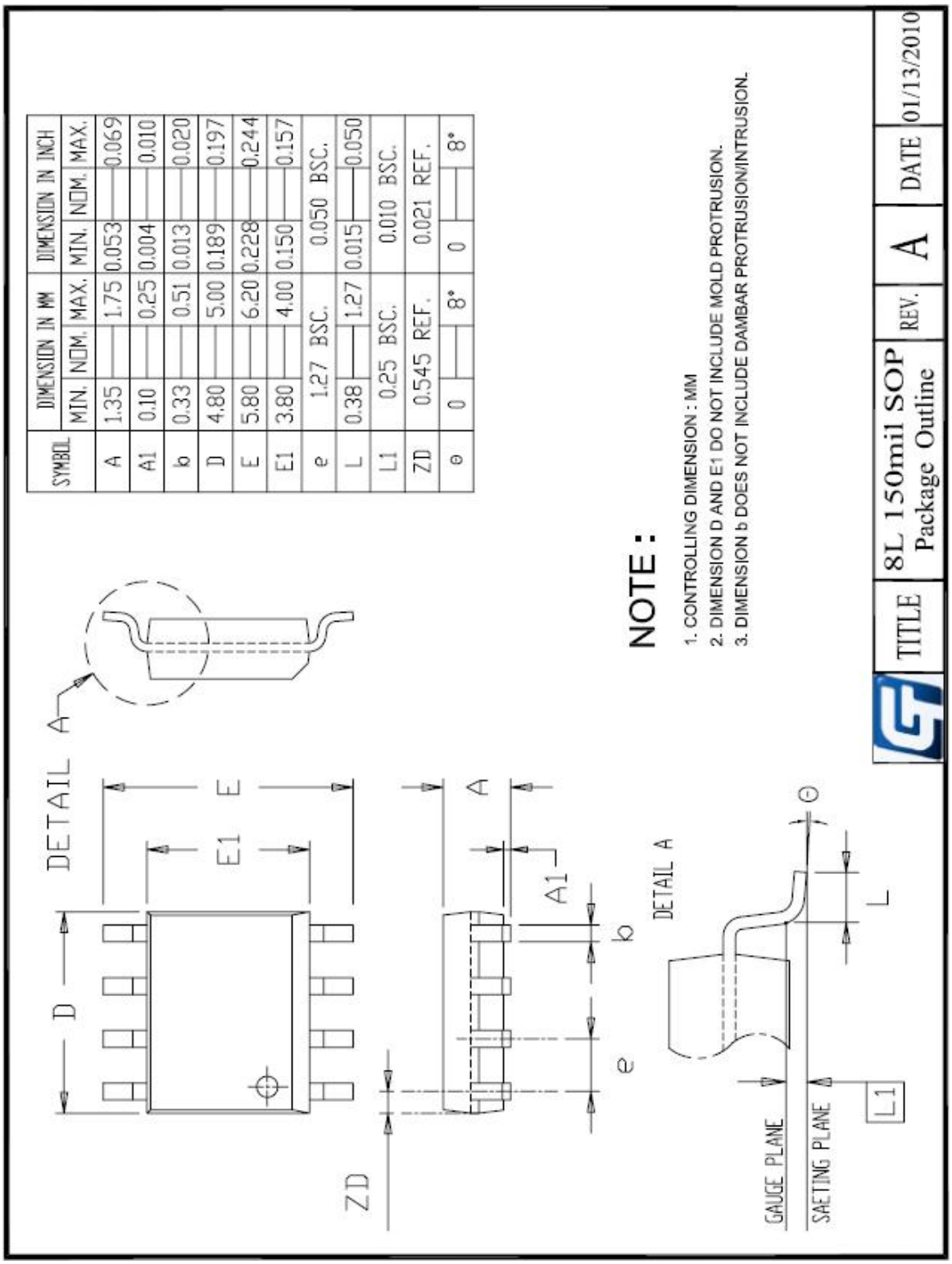
1. Contact Giantec Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel "-TR" (4K per reel). UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

# 12 PACKAGE INFORMATION

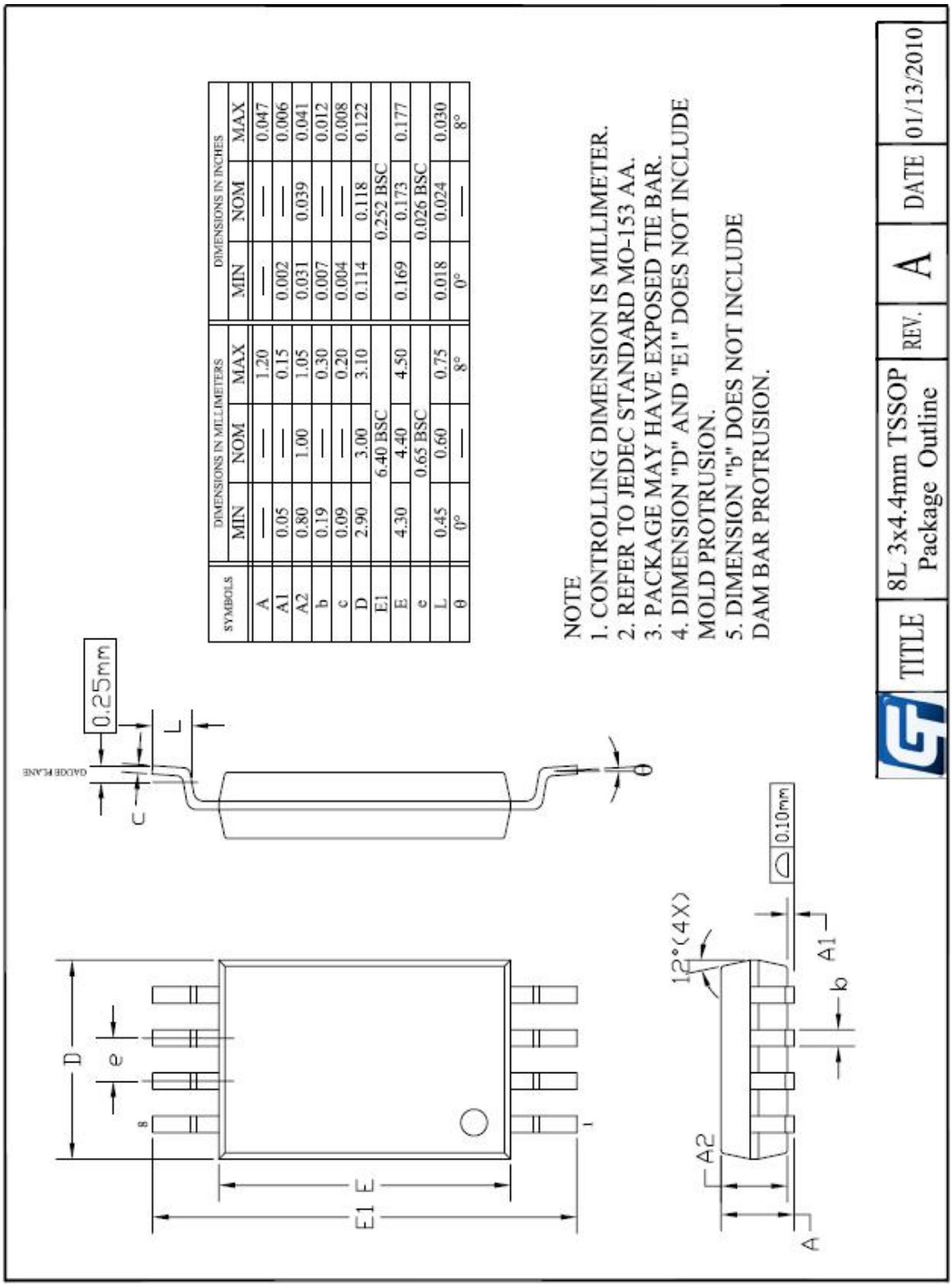
## PDIP



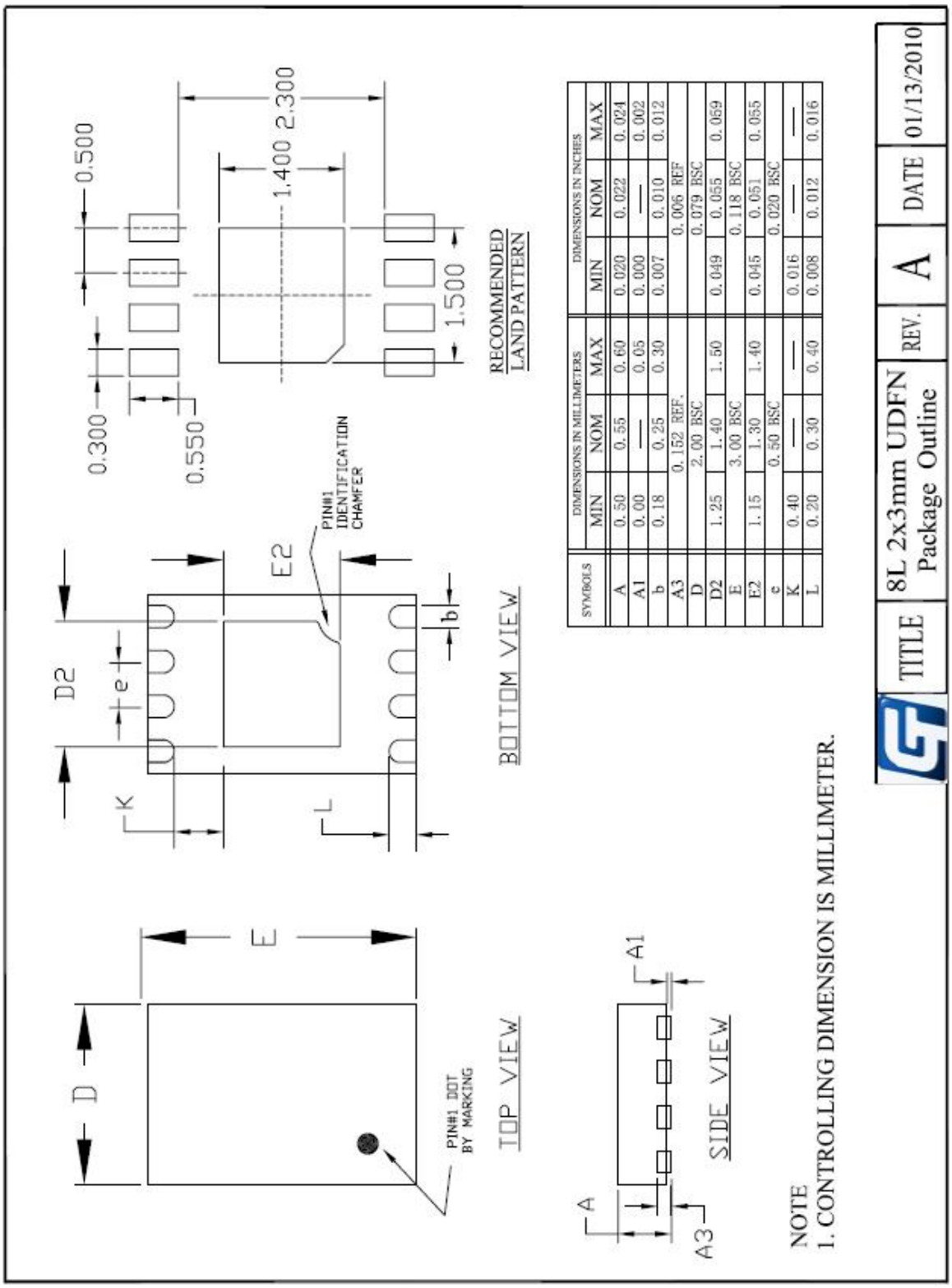
## SOIC/SOP (JEDEC)



## TSSOP

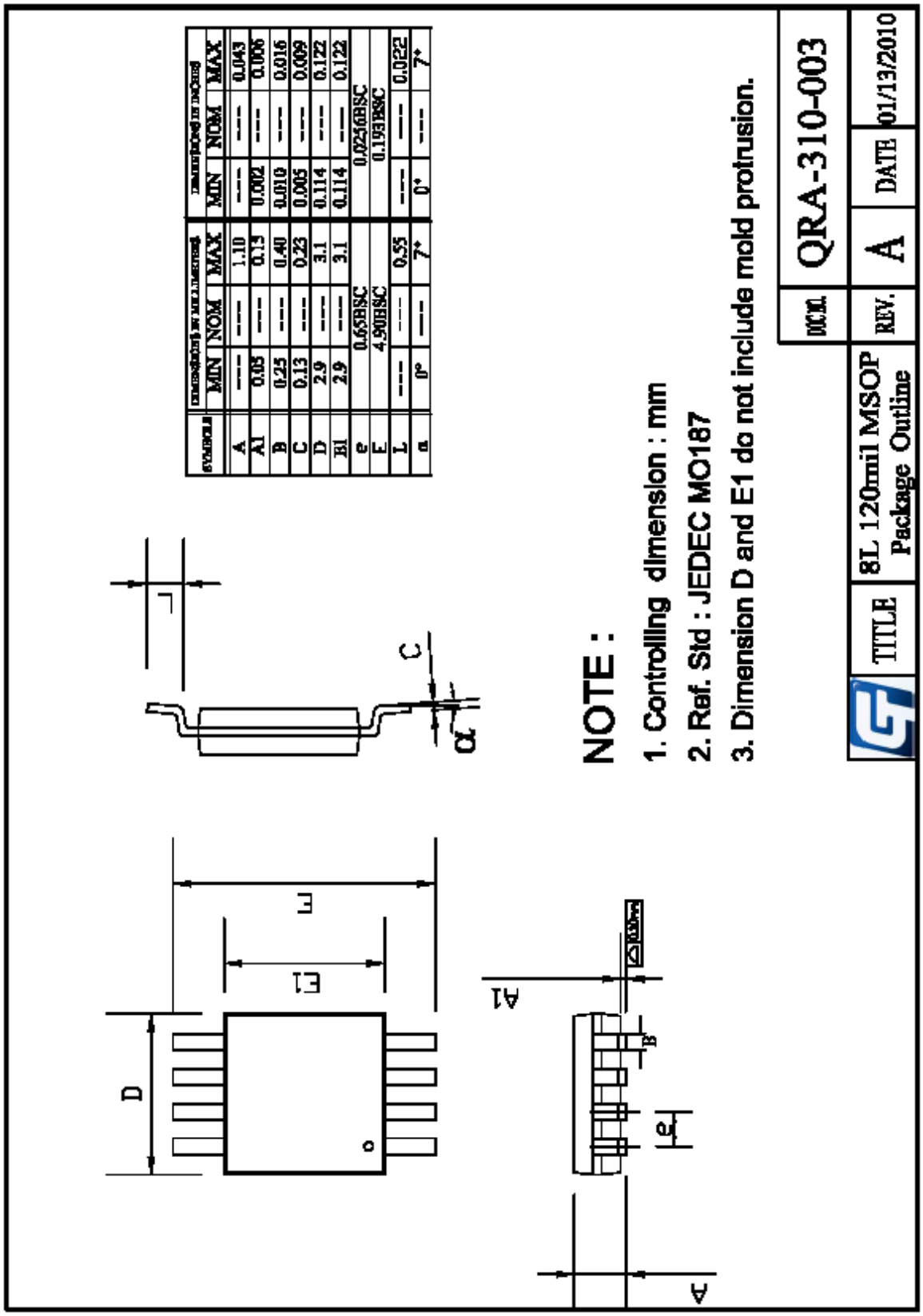


## UDFN: Ultra-thin DFN




| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.00 | — | 0.05 | 0.000 | — | 0.002 |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| A3 | | 0.152 REF. | | | 0.006 REF | |
| D | | 2.00 BSC | | | 0.079 BSC | |
| D2 | 1.25 | 1.40 | 1.50 | 0.049 | 0.055 | 0.059 |
| E | | 3.00 BSC | | | 0.118 BSC | |
| E2 | 1.15 | 1.30 | 1.40 | 0.045 | 0.051 | 0.055 |
| e | | 0.50 BSC | | | 0.020 BSC | |
| K | 0.40 | — | — | 0.016 | — | — |
| L | 0.20 | 0.30 | 0.40 | 0.008 | 0.012 | 0.016 |

**MSOP**



# 13 REVISION HISTORY

| Revision | Date | Descriptions |
|---|---|---|
| a0 | Jan 2010 | Initial draft |