IOR HiRel
An Infineon Technologies Company

RIC74424

Radiation hardened non-inverting dual output gate driver

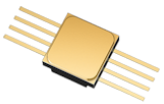
Features

- Dual independent gate drivers with common return
- Wide supply voltage operating range
- High drive current
- Low propagation delay
- Low quiescent current
- Schmitt trigger inputs with internal pull-down resistor
- Total ionizing dose (TID) hardness
  - Low dose rate (ELDRS) (<10 mrad(Si)/s) of 50 krad(Si)
  - High dose rate (50-300 rad(Si)/s) of 100 krad(Si)
- Single event effect (SEE) hardness
  - SEB, SEGR and SEL free up to 81.9 MeV·cm^2/mg
  - SET characterized up to 81.9 MeV·cm^2/mg
- ESD Rating: Class 3B per MIL-STD-883, Method 3015
- Electrical characteristics specified over full military temperature range

Product summary

- V_S = 5 V to 20 V
- $I_{OUTA/B}$ source/sink (typ) = 3 A / -3 A
- t_{on} (typ) = 110 ns
- t_{off} (typ) = 90 ns
- T_J = -55°C to 125°C

Package



Flatpack

Potential applications

- Satellite Bus and Payload
- Power Conditioning Unit
- Power Distribution Unit
- DC-DC Converter
- Motor Drive

Ordering information

Table 1 Ordering information

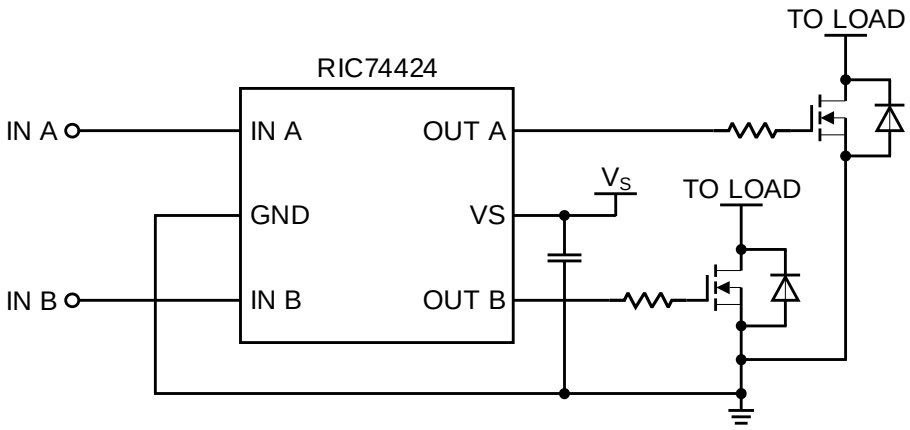
Orderable part number	Package type	Device class	Total ionizing dose level	Temperature range (°C)
RIC74424HSCS	Flatpack	Level S[1]	100 krad(Si)	-55 to 125
RIC74424HSCB	Flatpack	Level B[1]	100 krad(Si)	-55 to 125
RIC74424H	Flatpack	COTS	100 krad(Si)	-55 to 125
RIC74424EVAL1	Evaluation Board			

[1] Per MIL-PRF-38535

Description

RIC74424 is a high speed, dual channel low side gate driver intended for harsh radiation environments. It is specifically designed for high performance in demanding space environments, with electrical characteristics specified pre and post-irradiation over the entire military specification ambient temperature range of -55°C to 125°C and single event effects (SEE) characterized up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg.

RIC74424 enables high performance from key parameters. The 3 A source/sink gate drive and low propagation delay of 110 ns/90 ns results in lower power loss by reducing turn on and off time. The wide bias voltage range of 5 V to 20 V and input logic compatible with most analog and digital controllers allow for direct operation in a variety of systems. Additionally, Schmitt trigger inputs with internal pull-down resistor allow for support of input signals with lower risetimes. The dual independent channels provide flexibility to support multiple topologies, such as push-pull or active clamp forward, along with driving synchronous rectifier such as a current doubler and motors with two windings.



This diagram shows electrical connections only. Please refer to PCB layout recommendations section in this datasheet for proper circuit board layout.

Figure 1 Typical application block diagram

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1 Block diagram

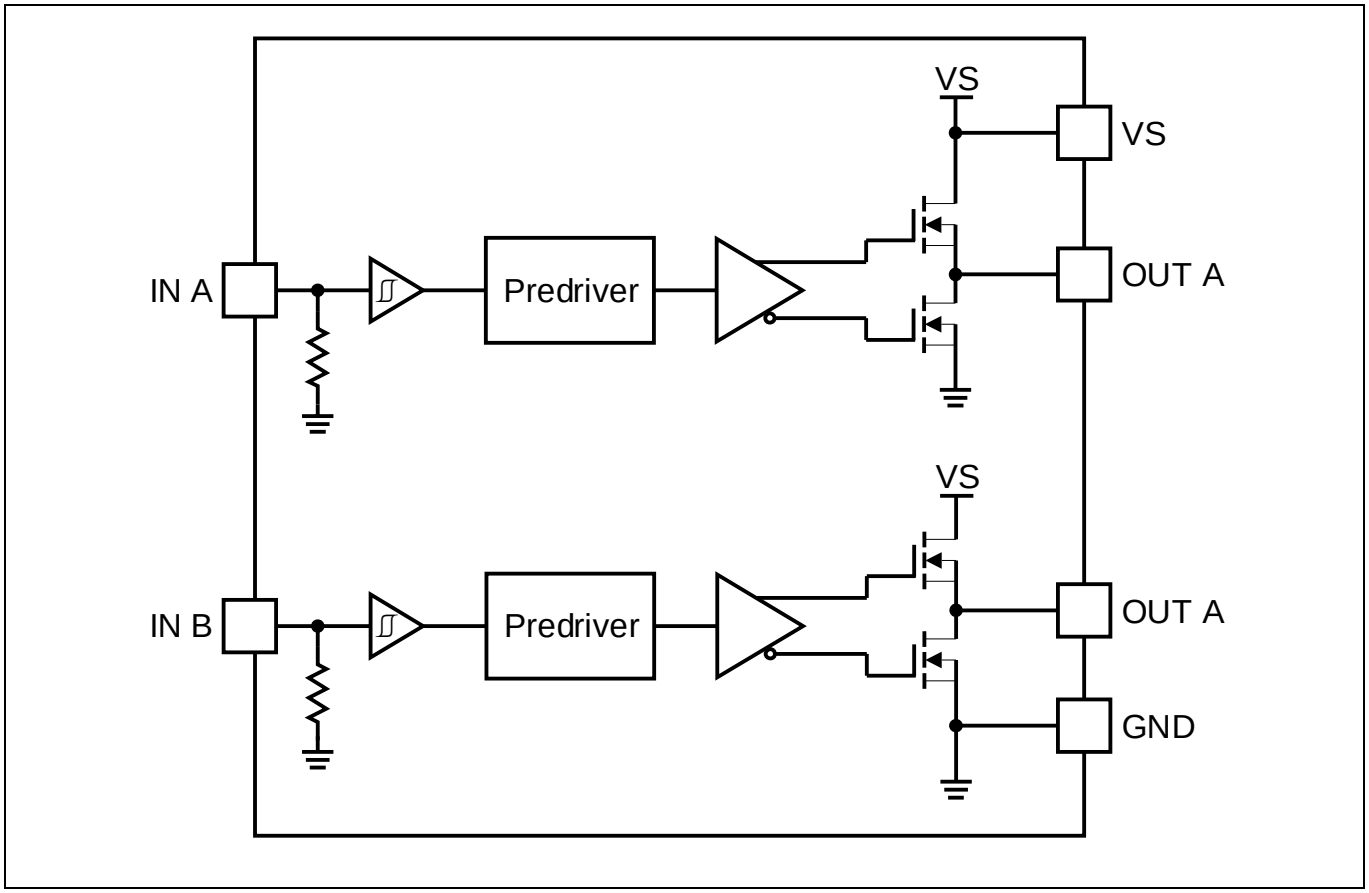
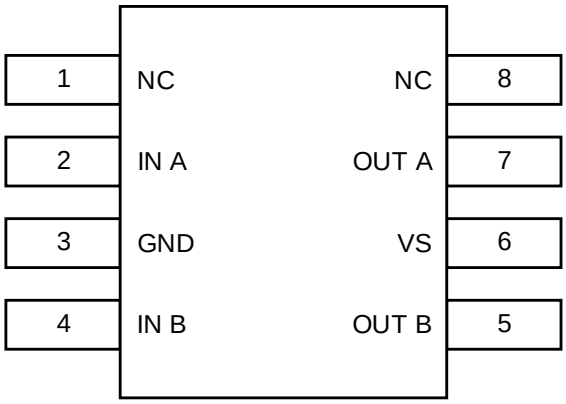


Figure 2 Block diagram

2 Pin configuration and functionality

2.1 Pin configuration



8 Lead Flatpack Package

RIC74424H

Figure 3 RIC74424 pin assignments (top view)

2.2 Pin functionality

Table 2 Pin functionality

Pin RIC74424H	Symbol	Description
1, 8	NC	No Connection. This may be connected to GND or left floating
2	IN A	Logic input for gate driver A
3	GND	Ground return
4	IN B	Logic input for gate driver B
5	OUT B	Output for driver B
6	VS	Supply voltage
7	OUT A	Output for driver A
Lid		No Connection. This may be connected to GND or left floating

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table.

Table 3 Absolute maximum ratings

Symbol	Definition	Min	Max	Units
V_S	Supply voltage	-0.3	20	V
V_{IN}	Input voltage	-0.3	V_S + 0.3	V
T_J	Operating junction temperature	-55	150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temp (soldering, 10s, 0.063in (1.6mm) from case)		300	°C

3.2 ESD ratings

Table 4 ESD ratings

Symbol	Definition	Value	Units
V_{ESD}	ESD Human Body Model (HBM), Class 3B per MIL-STD-883, Method 3015	8.75	kV

3.3 Thermal characteristics

All ratings are measured under board mounted and still air conditions.

Table 5 Thermal Characteristics

Symbol	Definition	Min	Max	Units
$R_{\Theta JL}$	Thermal resistance, junction to lead, with 1 driver on		400	°C/W
$R_{\Theta JL}$	Thermal resistance, junction to lead, with 2 drivers on		800	°C/W
$R_{\Theta JC}$	Thermal resistance, junction to case, with 1 driver on		11.7	°C/W
$R_{\Theta JC}$	Thermal resistance junction to case, with 2 drivers on		17.1	°C/W

3.4 Recommended operating conditions

For proper operation the device should be used within the recommended operating conditions. All voltage parameters are absolute voltages referenced to GND unless otherwise stated.

Table 6 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_S	Supply voltage	5	20	V
V_{IN}	Input voltage	0	V_S	V
T_J	Junction temperature	-55	125	°C

3.5 Static electrical characteristics

V_S = 5 V to 20 V and $T_A = T_J$ = -55 to 125°C unless otherwise specified. All voltage parameters are absolute voltages referenced to GND and all parameter ratings are per single driver unless otherwise stated. **Parameter ratings that are stated post-irradiation apply over a total ionizing dose (TID) of 100 krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s.**

Table 7 Static electrical characteristics

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
Bias Power							
V_{STH}	VS enable threshold	1	3		5	V	T_J=25°C, **Post-irradiation**
		2, 3	3		5	V	
V_{SHY}	VS enable hysteresis	1, 2, 3		150		mV	
I_{QS}	VS quiescent current	1			400	µA	V_S=5 V, V_{IN}=0 V or 5 V, T_J=25°C, **Post-irradiation**
		2, 3			400	µA	V_S=5 V, V_{IN}=0 V or 5 V
		1			900	µA	V_S=15 V, V_{IN}=0 V or 15 V, T_J=25°C, **Post-irradiation**
		2, 3			900	µA	V_S=15 V, V_{IN}=0 V or 15 V
		1, 2, 3			900	µA	V_S=20 V, V_{IN}=0 V or 20 V
Input							
V_{IH}	Logic “1” input voltage	1	3.0			V	V_S=15 V, T_J=25°C, **Post-irradiation**
		1	3.0			V	V_S=15 V or 20 V, T_J=25°C
		2	3.5			V	V_S=15 V or 20 V, T_A=125°C
		3	2.9			V	V_S=15 V or 20 V, T_A=-55°C
V_{IL}	Logic “0” input voltage	1			0.4	V	V_S=15 V, T_J=25°C, **Post-irradiation**
		1			0.4	V	V_S=15 V or 20 V, T_J=25°C
		2, 3			0.4	V	V_S=15 V or 20 V
I_{INH}	Logic “1” input current	1			10	µA	V_S= 5 V or 15 V, V_{IN}=5 V, T_J=25°C, **Post-irradiation**
		2, 3			11	µA	V_S=5 V, 15 V or 20 V, V_{IN}=5V
I_{INL}	Logic “0” input current	1			5	µA	V_S=5 V or 15 V, V_{IN}=0 V, T_J=25°C, **Post-irradiation**

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
I_{INL}	Logic “0” input current	2, 3			5	µA	V_S=5 V, 15 V or 20 V, V_{IN}=0 V
Output							
V_{OH}	Logic “1” output voltage (V_{VS}-$V_{OUT\ A/B}$)	1			1.3	V	V_S=15 V, V_{IN}=5 V, $I_{OUT\ A/B}$=0 mA, T_J=25°C, **Post-irradiation**
		1, 2, 3			1.3	V	V_S=15 V, V_{IN}=5 V, $I_{OUT\ A/B}$=0 mA
					2.175	V	V_S=15 V, V_{IN}=5 V, $I_{OUT\ A/B}$=2 mA
					2.975	V	V_S=15 V, V_{IN}=5 V, $I_{OUT\ A/B}$=20 mA
V_{OL}	Logic “0” output voltage ($V_{OUT\ A/B}$)	1			0.1	V	V_S=15 V, V_{IN}=0 V, $I_{OUT\ A/B}$=0 mA, T_J=25°C, **Post-irradiation**
		1, 2, 3			0.1	V	V_S=15 V, V_{IN}=0 V, $I_{OUT\ A/B}$=0 mA
					0.1	V	V_S=15 V, V_{IN}=0 V, $I_{OUT\ A/B}$=2 mA
					0.14	V	V_S=15 V, V_{IN}=0 V, $I_{OUT\ A/B}$=20 mA
I_{O+}	Output high short circuit pulsed current[2]	1, 2, 3		2.0		A	V_S=10 V, PW ≤ 10 µs
		1, 2, 3		3.5		A	V_S=15 V, PW ≤ 10 µs
		1, 2, 3		4.5		A	V_S=18 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current[2]	1, 2, 3		2.0		A	V_S=10 V, PW ≤ 10 µs
		1, 2, 3		3.5		A	V_S=15 V, PW ≤ 10 µs
		1, 2, 3		4.5		A	V_S=18 V, PW ≤ 10 µs

[1] Per MIL-STD-883 Method 5005

[2] Parameter not subject to production test. Parameter guaranteed by design and characterization.

3.6 Dynamic electrical characteristics

V_S = 5 V to 20 V, T_A = T_J = -55 to 125°C and C_L = 1 nF unless otherwise stated. Refer to Figure 4 for switching time definition and Figure 5 for test schematic. **Parameter ratings that are stated post-irradiation apply over a total ionizing dose (TID) of 100 krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s.**

Table 8 Dynamic electrical characteristics

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
t_r	Rise time	9, 11		50	60	ns	V_S=5 V, T_A=-55 to 25°C
		10			125	ns	V_S=5 V, T_A=125°C
		9, 10, 11		25	40	ns	V_S=12 V
		9, 10, 11		20	40	ns	V_S=15 V

Electrical parameters

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
t_f	Fall time	9, 10, 11		25	40	ns	V_S=5 V
		9, 10, 11		15	30	ns	V_S=12 V
		9, 10, 11		15	25	ns	V_S=15 V
t_{on}	Turn-on propagation delay	9, 11		230	320	ns	V_S=5 V, T_A=-55 to 25°C
		10			410	ns	V_S=5 V, T_A=125°C
		9, 11		110	170	ns	V_S=12 V, T_A=-55 to 25°C
		10			210	ns	V_S=12 V, T_A=125°C
		9, 11		100	160	ns	V_S=15 V, T_A=-55 to 25°C
		10			190		V_S=15 V, T_A=125°C
t_{off}	Turn-off propagation delay	9, 11		170	290	ns	V_S=5 V, T_A=-55 to 25°C
		10			420	ns	V_S=5 V, T_A=125°C
		9, 10, 11		90	180	ns	V_S=12 V
		9, 11		85	160	ns	V_S=15 V, T_A=-55 to 25°C
		10			170		V_S=15 V, T_A=125°C

[1] Per MIL-STD-883 Method 5005

4 Timing diagrams

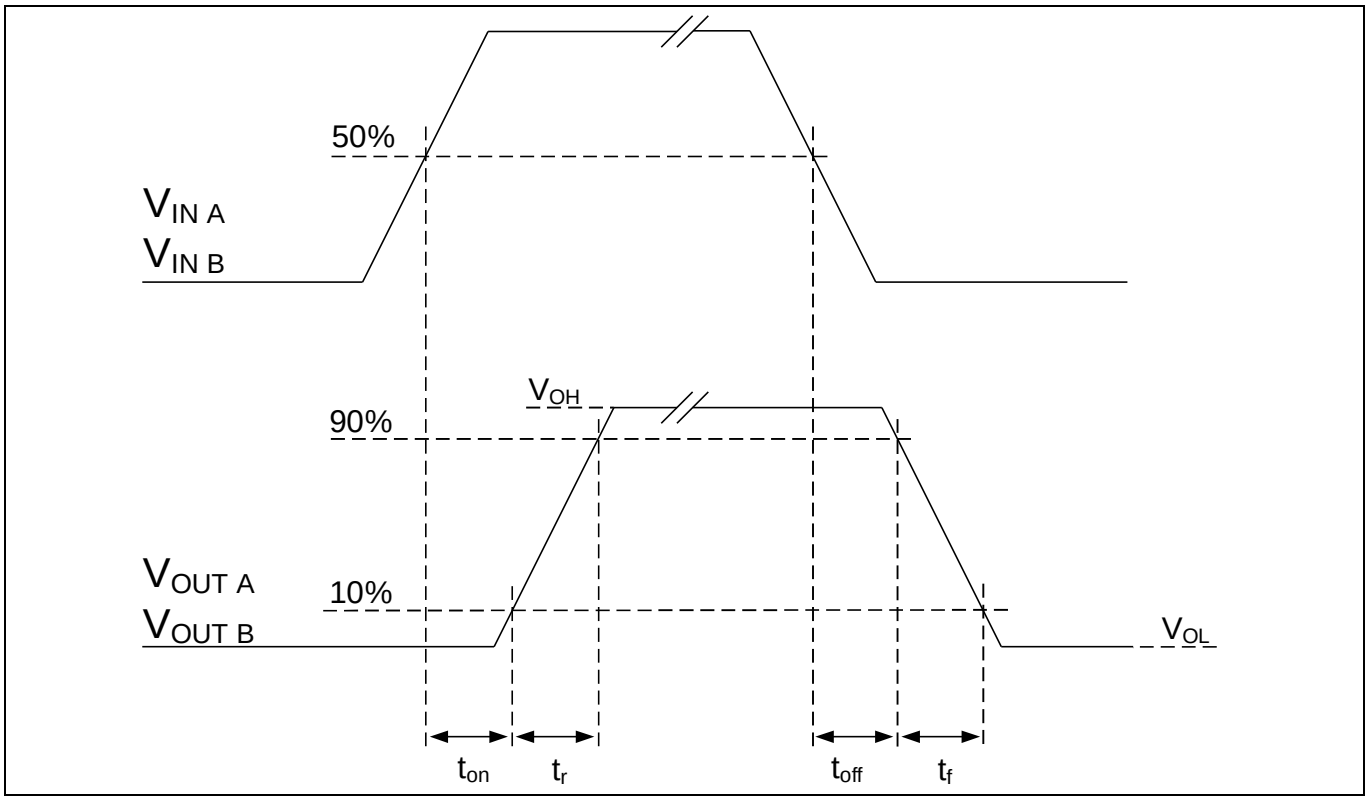


Figure 4 Propagation delay, rise and fall time definition

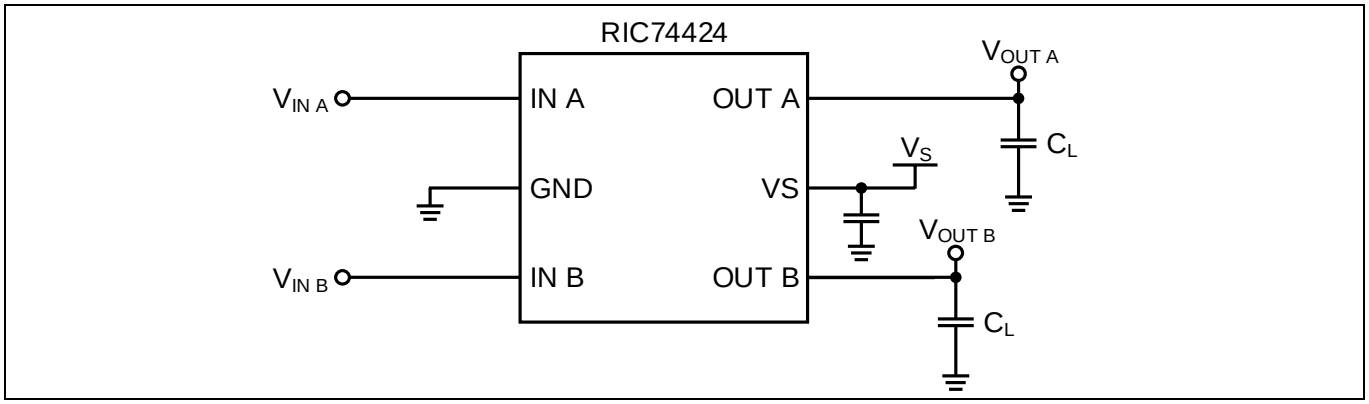


Figure 5 Dynamic electrical characteristics circuit

5 Typical characteristics

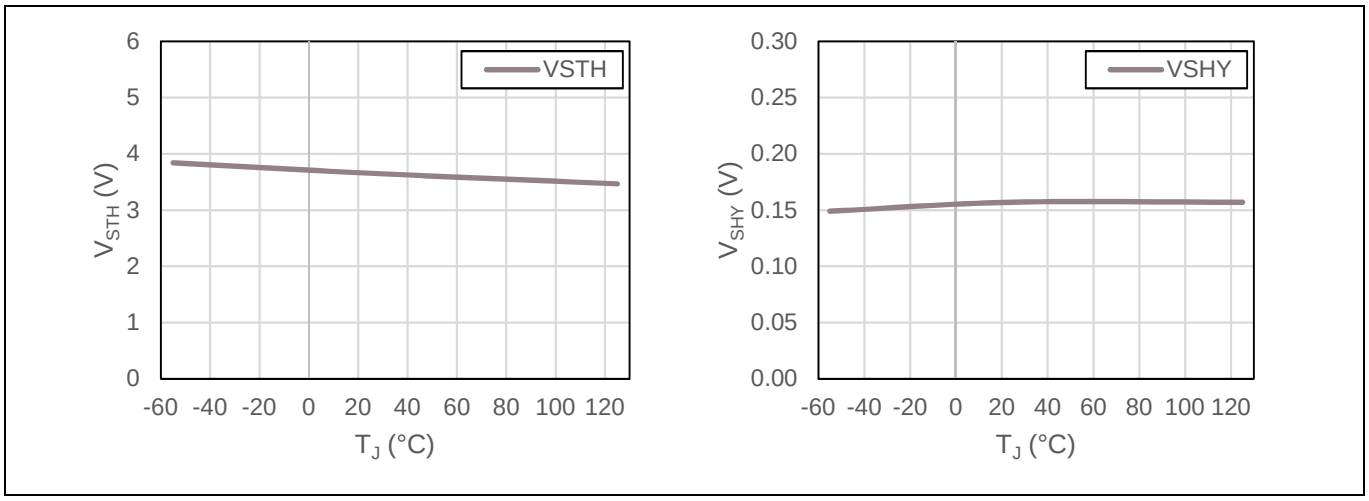


Figure 6 V_{STH} and V_{SHY} over temperature

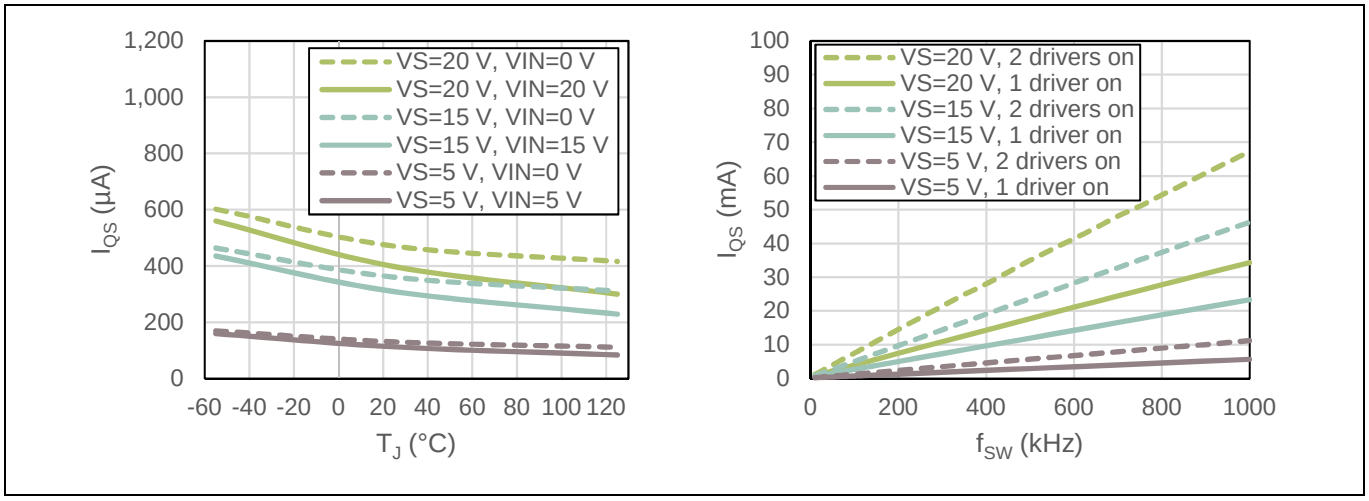


Figure 7 I_{QS} over temperature and frequency

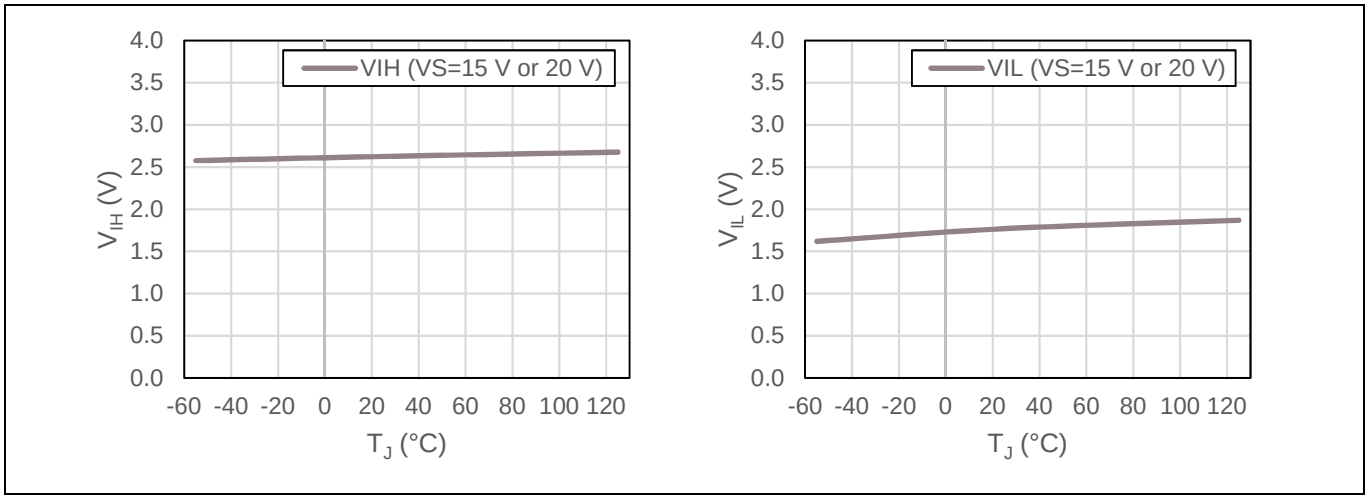


Figure 8 V_{IH} and V_{IL} over temperature

Typical characteristics

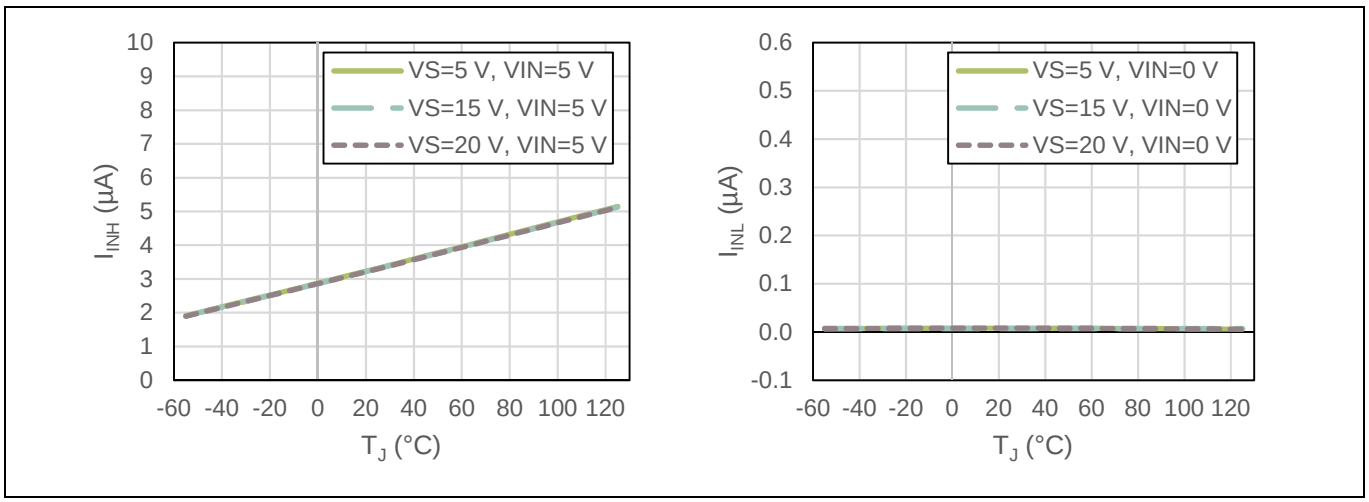


Figure 9 I_{INH} and I_{INL} over temperature

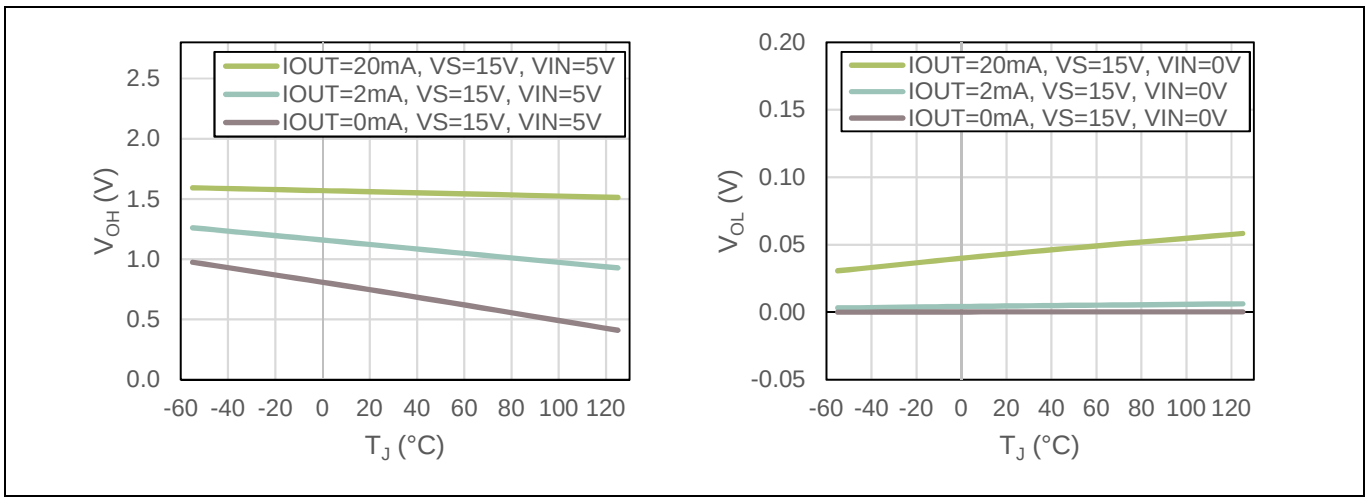


Figure 10 V_{OH} and V_{OL} over temperature

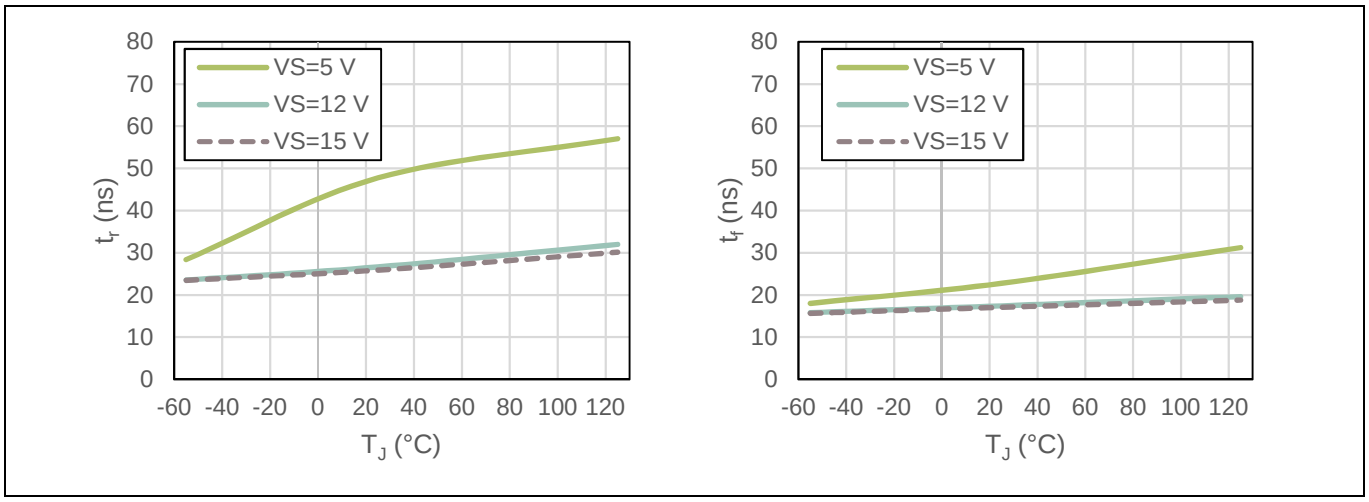


Figure 11 t_r and t_f over temperature

Typical characteristics

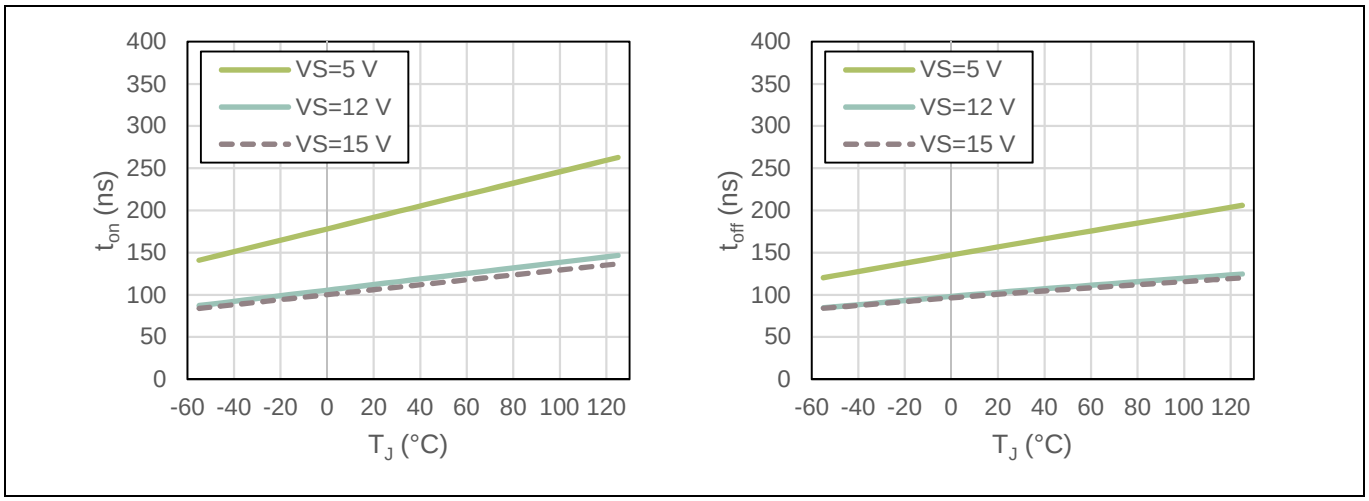


Figure 12 t_{on} **and** t_{off} **over temperature**

6 Application information and additional details

RIC74424 is an independent two channel low side gate driver. The independent logic allows for use in single ended topologies, such as boost or flyback, or dual ended low side referenced topologies such as a push-pull and active clamp forward. It may also be used to drive synchronous rectifiers, such as a current doubler. The high speed and large drive strength facilitates high efficient driving of power FET, such as the R9 MOSFET and rad hard powerMOS. Performance is shown with the evaluation board RIC74424EVAL1.

6.1 Radiation performance

RIC74424 is designed to work in space and other applications where there is significant ionizing radiation and energetic particles in the environment that can affect microcircuit performance. RIC74424 is characterized for operation up to a total ionizing dose (TID) of 100 krad, with electrical parameters including limits post-irradiation. It is also characterized for single event effects (SEE) up to 81.9 MeV·cm^2/mg.

The packaged version of RIC74424 has several NC pins and metal lid. All of these metal points are isolated from one another and are electrically floating. Typically, in space and other irradiation environments, it is desired for all conductors to be connected to known potentials, since floating metal can build up charge and lead to undesired effects. To satisfy this requirement all the NC pins and metal lid can be connected to GND. It is recommended to ensure that any connection made does not violate any creepage or clearance spacing requirement.

6.1.1 Total ionizing dose (TID)

RIC74424 is tested over TID to verify robustness to ionizing protons and electrons radiation environments, such as space. The radiation hardness assurance (RHA) program at IR HiRel uses a Cobalt-60 (60 Co) source. Every wafer is tested per MIL-STD-883, Method 1019, test condition A “Ionizing Radiation (Total Dose) Test Procedure.” Both pre- and post-irradiation performance are tested to the limits specified in the electrical characteristics. For details on TID hardness refer to the RIC74424 TID test report.

6.1.2 Single event effects (SEE)

RIC74424 has been characterized in heavy ion environment for SEE. RIC74424 is single event burnout (SEB), single event gate rupture (SEGR) and single event latchup (SEL) free over the entire recommended VS operating range of 5 V to 20 V up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg. Single event transients (SET) from heavy ions are characterized up to an LET of 81.9 MeV·cm^2/mg. For details on SEE performance refer to the RIC74424 SEE test report.

6.2 Bias power

RIC74424 features undervoltage lock out to prevent operation when the bias voltage is too low. To start operation, the bias voltage V_S must exceed the enable threshold V_{STH}. It includes hysteresis, so once on RIC74424 will operate until the bias voltage drops by V_{SHY} from V_{STH}. For proper operation it is recommended to maintain V_S within the recommended range of 5 V to 20 V. RIC74424 also features low quiescent current I_{QS}, which helps improve system efficiency.

6.2.1 VS bypass capacitance

An external bypass capacitor from VS to GND is highly recommended. For typical designs this capacitor acts to decouple any inductance in series with the power supply source for VS. Without it there could be voltage fluctuations on V_S which can interfere or interrupt operation.

A surface mount ceramic capacitor is recommended due to the low equivalent series resistance (ESR). To help minimize parasitic inductance from PCB trace and layout, it's recommended to place the capacitor as close to VS and GND pin as possible.

6.3 Input

RIC74424 has two independent inputs which control their corresponding outputs, where IN A drives OUT A and IN B drives OUT B. Both inputs support 5 V and higher CMOS logic and have low current consumption, which allows support for many common analog and digital controllers.

Both inputs feature Schmitt triggers on the input, which provides hysteresis to enhance noise immunity. This helps insure that an input signal with low rise time and noise will result in a clean, desired output. They also have internal pull-down resistors, which help insure that the output voltage is low during initial startup or any instance where the input signal is high impedance.

While not required, in high electrical noise environments it may be desired to have a low pass RC filter as close to the input pins IN A and IN B to insure proper operation. If a filter is used, it is recommended the cutoff frequency is sufficiently high enough to prevent significant phase delay from impacting overall performance. It is also recommended to keep the filter as close as possible to the IN A and IN B pins as possible.

6.4 Output

Each output of RIC74424 is a high speed driver. The output drive in RIC74424 are two n-channel MOSFETs in a totem pole configuration. This reduces the turn on delay, which in turn lowers switching losses of the power MOSFET that it is driving.

6.4.1 Drive voltage

The drive voltage level is dependent on the supply voltage V_S, where the drive voltage $V_{OUT\ A/B}$ is V_S minus the voltage drop in the internal high side NMOS transistor V_{OH}. Please note that V_{OH} varies over output drive current, details of which are specified in the electrical parameters.

$$V_{OUT\ A/B} = V_S - V_{OH}$$

6.4.2 External gate drive resistor

While not always required, an external gate drive resistor is often times used to reduce generated EMI, reduce voltage ringing on the power FET gate and lower temperature rise in RIC74424. This resistance has an undesired side effect of increasing switching loss in the power FET, so it's important to determine the best value for this resistance to optimize tradeoffs.

6.4.2.1 EMI

An external resistor slows down the time it takes to turn on and off the power FET, which in turn reduces the high voltage slew rate seen on the drain of the power FET. This reduction in slew rate lowers the voltage overshoot and ringing often times seen in switched mode power supplies, which is a major source of EMI. The exact resistance depends on the specifics of the design, since EMI filtering is a system level challenge that can be resolved thru a combination of many different techniques. For more information on EMI filter design please refer to the application note EMC and System-ESD Design Guidelines for Board Layout.

6.4.2.2 Gate voltage ringing

Parasitic inductance from PCB trace and package leads, among others, create a LC resonant tank with the capacitance at the gate of the power FET. This resonant tank causes voltage overshoot and ringing during normal PWM operation. To prevent this ringing from reducing performance or damaging components, a gate

drive resistor is often times used to dampen the LC resonant tank. For some designs the internal resistance in RIC74424 is sufficient, but for others an additional external resistor is needed for proper dampening. For more information on how to select a gate drive resistor for dampening refer to the application note CoolMOS™ gate drive and switching dynamics.

6.4.2.3 Power loss

During normal operation, the power FET's repeated charging and discharging of the total gate charge causes losses in RIC74424. If no external resistor is used, these losses are all in RIC74424 and the corresponding temperature rise can limit the operating range. An external resistor dissipates some of these losses, which in turn reduces the temperature rise in RIC74424 and extends the effective ambient temperature range. The total loss in RIC74424 can be calculated with the equations below.

$$P_{on\_int} = \frac{1}{2} \times Q_g \times V_{OUT\ A/B} \times f_{SW} \times \frac{R_{on\_int}}{R_{on\_int} + R_{on\_ext}}$$

$$P_{off\_int} = \frac{1}{2} \times Q_g \times V_{OUT\ A/B} \times f_{SW} \times \frac{R_{off\_int}}{R_{off\_int} + R_{off\_ext}}$$

Where

- Q_g is the total gate charge, which is specified in the FET datasheet
- $V_{OUT\ A/B}$ is the output drive voltage, which can be calculated using the equation in section 6.4.1
- f_{sw} is the switching frequency, which is selected during the design process
- R_{on_int} is the internal source resistance of RIC74424, which is typically 3.5 Ω when V_S=5 V, 2.1 Ω when V_S=15 V and 2 Ω when V_S=20 V
- R_{on_ext} is the external turn on resistance, which is selected during the design process
- R_{off_int} is the internal turn off resistance of RIC74424, which is typically 3.5 Ω when V_S=5 V, 2.1 Ω when V_S=15 V and 2 Ω when V_S=20 V
- R_{off_ext} is the external turn off resistance, which is selected during the design process

Likewise, the power loss for each external resistor can be calculated by modifying these equations slightly, as shown below.

$$P_{on\_ext} = \frac{1}{2} \times Q_{gtot} \times V_{OUT\ A/B} \times f_p \times \frac{R_{on\_ext}}{R_{on\_int} + R_{on\_ext}}$$

$$P_{off\_ext} = \frac{1}{2} \times Q_{gtot} \times V_{OUT\ A/B} \times f_p \times \frac{R_{off\_ext}}{R_{off\_int} + R_{off\_ext}}$$

6.4.2.4 Separate turn on and off resistance

Often times it is determined and desired to have a separate external resistor for turn on and turn off. This can be achieved by using a fast diode in series with a resistor in parallel with another resistor, as shown in Figure 13.

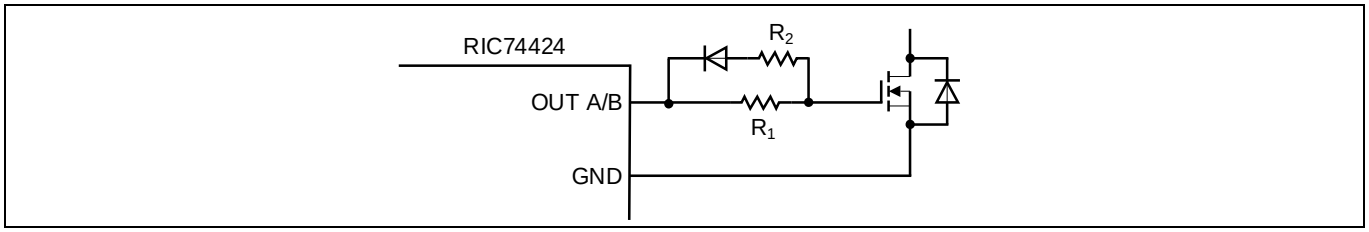


Figure 13 External gate drive resistor with separate turn on and off speed

The corresponding external turn on R_{on_ext} and turn off R_{off_ext} resistance can be calculated with the following equations

$$R_{on\_ext} = R_1$$

$$R_{off\_ext} = R_1||R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

For the diode selection, it is recommended to select a blocking voltage that is high enough to support $V_{OUT\ A/B}$ plus any voltage overshoot. For high frequency operation a Schottky diode is recommended to reduce losses.

6.4.3 Parallel output

For higher current output to drive larger power transistors, the two channels of RIC74424 can be combined to create a single channel low side driver with twice the drive strength. This is done by connecting IN A and IN B, as well as OUT A and OUT B together, as shown in Figure 14. It is recommended to keep the PCB connection between IN A and IN B, along with OUT A and OUT B as short as possible to minimize undesired effects from PCB parasitic components.

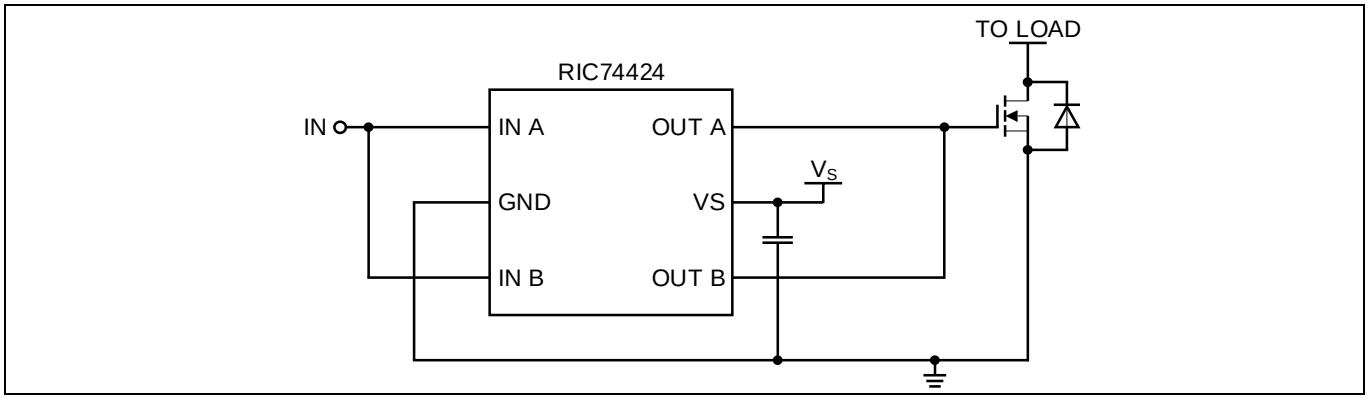


Figure 14 Parallel output

6.5 PCB layout recommendations

To achieve high performance a good PCB layout is required. A poor layout can introduce parasitic inductance and capacitance, which couple electrical noise that interferes with operation. Below are some recommendations to reduce these undesired impacts, and Figure 15 shows a recommended layout.

- Input RC filter: place as close to IN A/B and GND as possible
- VS bypass capacitor: place as close to RIC74424 as possible with short trace length for both VS and GND
- Power FET source kelvin connection: have an independent trace from GND to the source pin (or as close to the source pin as possible)
- Isolate ground loops: keep separate ground for logic and power, with single connection point close to GND

Isolate noise: keep sensitive logic signals (such as IN A/B) far away from the drain voltage of the FET and other high electrical noise sources

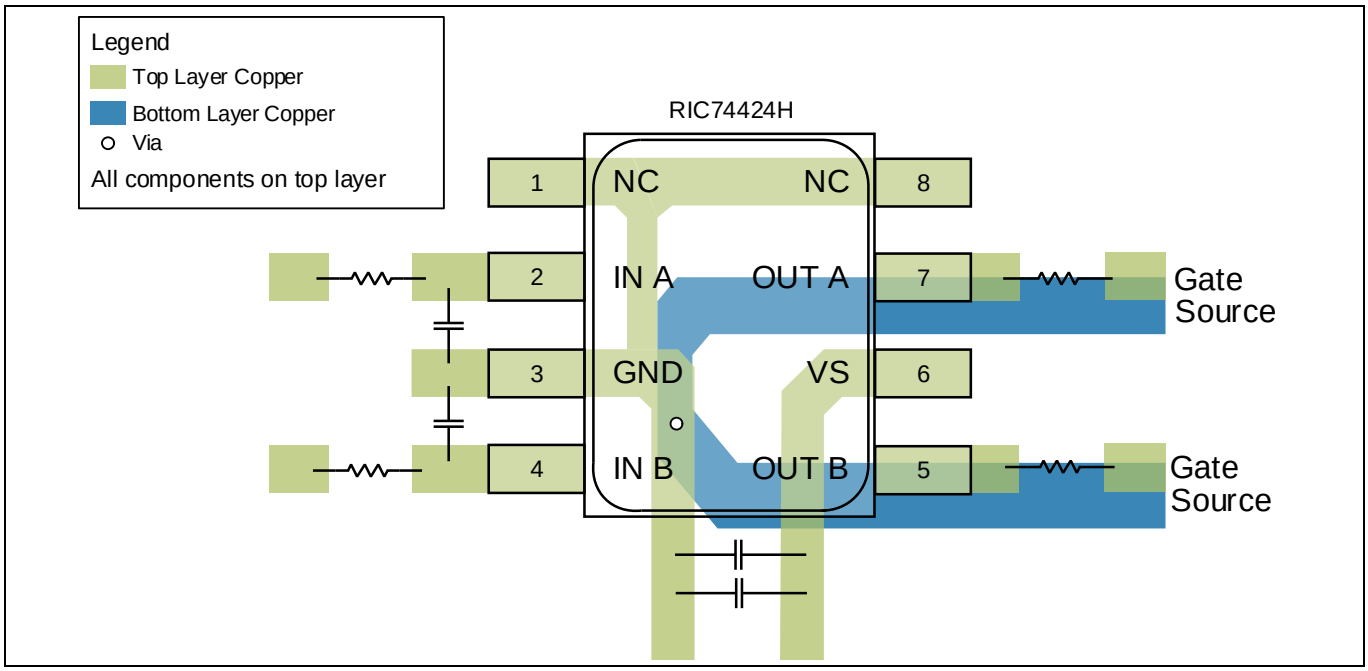


Figure 15 Recommended PCB layout

7 Package details

7.1 Flatpack

For latest package outline drawing please refer to 8-Lead Flatpack package outline.

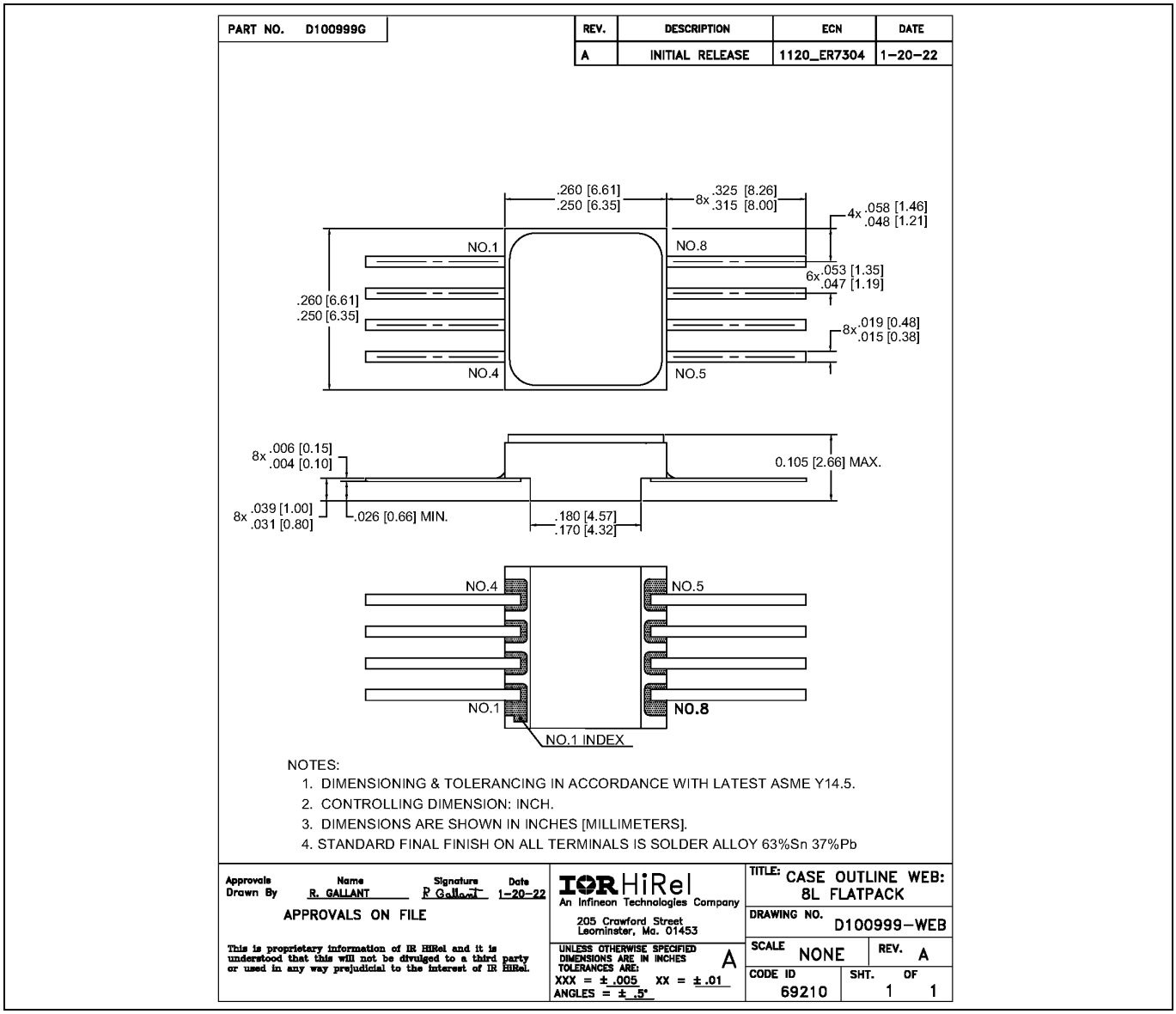


Figure 16 8-Lead Flatpack package outline

Revision history

Document revision	Date	Description of changes
	12/20/2018	Datasheet (PD-97901)
Rev A	09/22/2022	Updated based on ECN-1120_09211

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