

Product Summary

BV_{DSS}	$R_{DS(ON)} \text{ Max}$	$I_D \text{ Max}$ $T_A = +25^\circ\text{C} (t < 10\text{s})$
-30V	7.0m Ω @ $V_{GS} = -10\text{V}$	-17A
	10.0m Ω @ $V_{GS} = -4.5\text{V}$	-13A

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

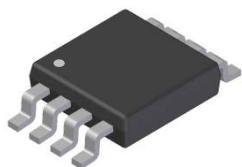
- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

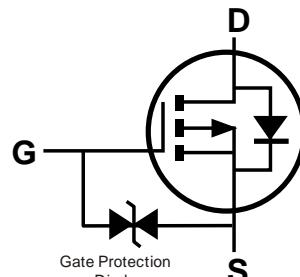
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

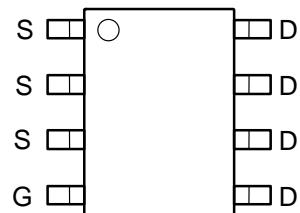
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections Indicator: See Diagram Below
- Terminals: Finish—Matte Tin Annealed Over Copper Leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.074 grams (Approximate)



Top View



Internal Schematic


 Top View
Pin Configuration

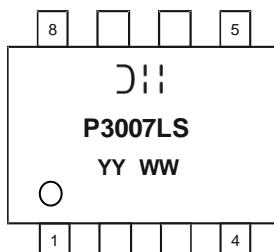
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3007LSS-13	SO-8	2,500/Tape & Reel

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



DII = Manufacturer's Marking
P3007LS = Product Type Marking Code
YYWW = Date Code Marking
YY or **YY** = Year (ex: 18 = 2018)
WW = Week (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit		
Drain-Source Voltage			V_{DSS}	-30	V		
Gate-Source Voltage			V_{GSS}	± 25	V		
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 6)	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-14 -11.5	A		
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$		-17 -12.5	A		
	Maximum Continuous Body Diode Forward Current (Note 6)		I_S	-16.5	A		
	Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)		I_{DM}	-120	A		
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)			I_{SM}	-120	A		
Avalanche Current, $L=1\text{mH}$ (Note 7)			I_{AS}	-13	A		
Avalanche Energy, $L=1\text{mH}$ (Note 7)			E_{AS}	87	mJ		

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$ Steady State $t < 10\text{s}$	P_D	1.4	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	91	°C/W
Total Power Dissipation (Note 6)		P_D	2.1	W
Thermal Resistance, Junction to Ambient (Note 6)	$T_A = +25^\circ\text{C}$ Steady State $t < 10\text{s}$	$R_{\theta JA}$	59	°C/W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	48	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}		-55 to +150	°C

Electrical Characteristics ($T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-2.8	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	4.1	7	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -17\text{A}$
		—	5.9	10		$V_{GS} = -4.5\text{V}, I_D = -15\text{A}$
		—	6.4	12		$V_{GS} = -4.0\text{V}, I_D = -13\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	$V_{GS} = 0\text{V}, I_S = -1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	2826	—	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	606	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	305	—	pF	
Gate Resistance	R_g	—	22.8	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_g	—	31.2	—	nC	$V_{DS} = -15\text{V}, I_D = -11.5\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_g	—	64.2	—	nC	
Gate-Source Charge	Q_{gs}	—	10.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	11.6	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.8	—	ns	
Turn-On Rise Time	t_r	—	4.3	—	ns	$V_{DD} = -15\text{V}, V_{GS} = -10\text{V}, R_g = 6\Omega, I_D = -11.5\text{A}$
Turn-Off Delay Time	$t_{D(OFF)}$	—	306	—	ns	
Turn-Off Fall Time	t_f	—	125	—	ns	
Reverse Recovery Time	t_{RR}	—	19	—	ns	$I_S = -11.5\text{A}, dI/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	9.8	—	nC	

Notes:

5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

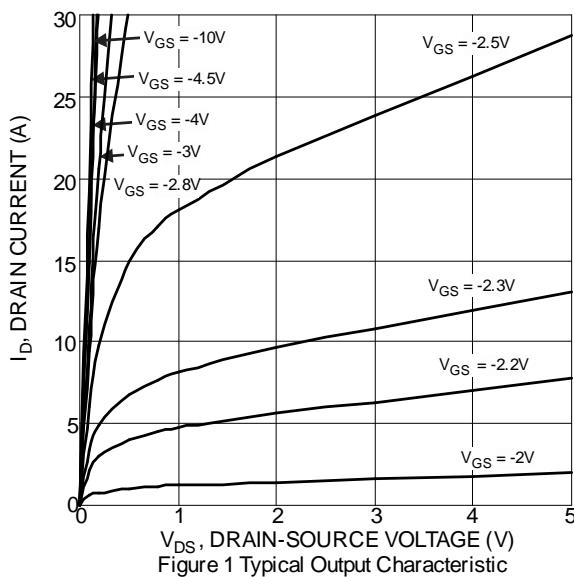


Figure 1 Typical Output Characteristic

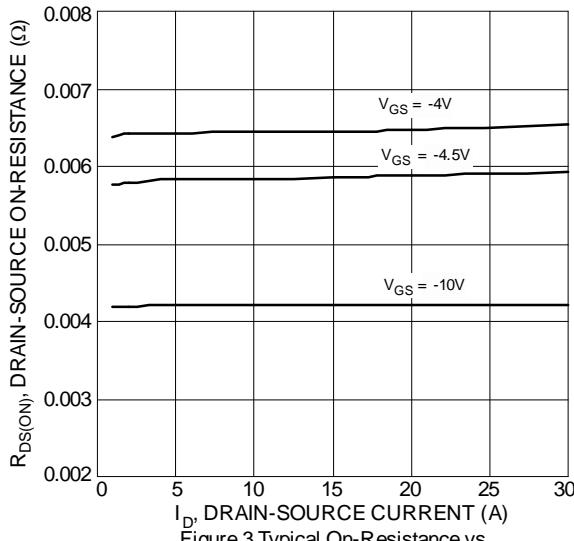


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

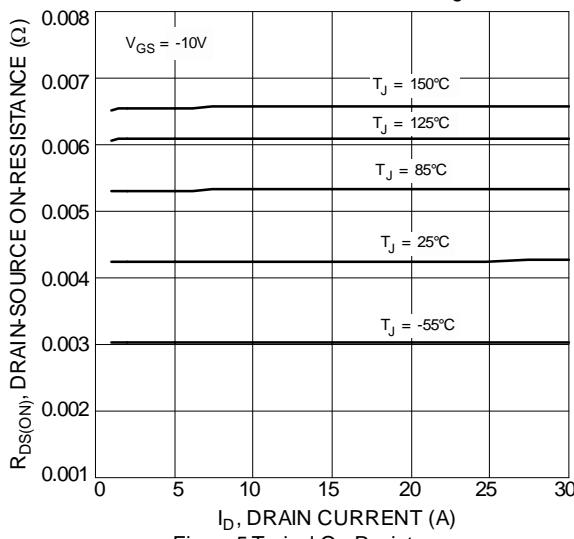


Figure 5 Typical On-Resistance vs.
Drain Current and Temperature

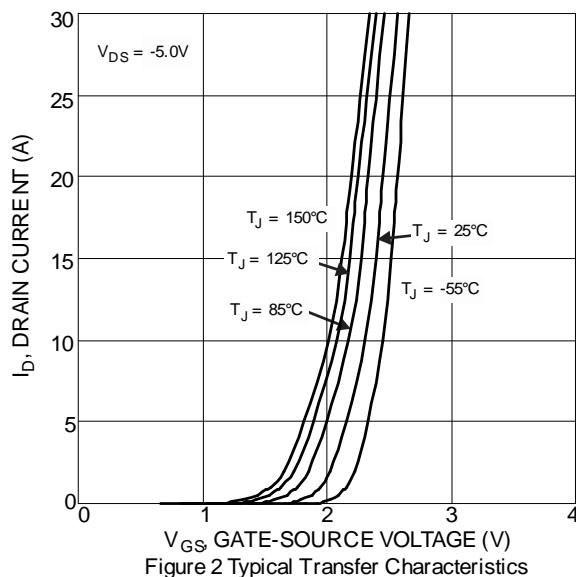


Figure 2 Typical Transfer Characteristics

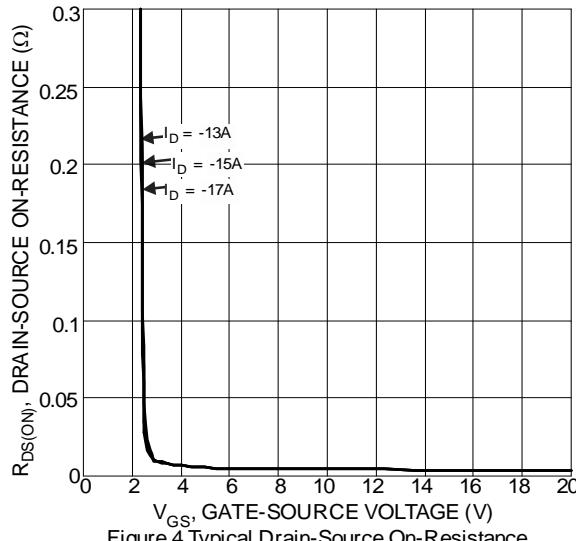


Figure 4 Typical Drain-Source On-Resistance
vs. Gate-Source Voltage

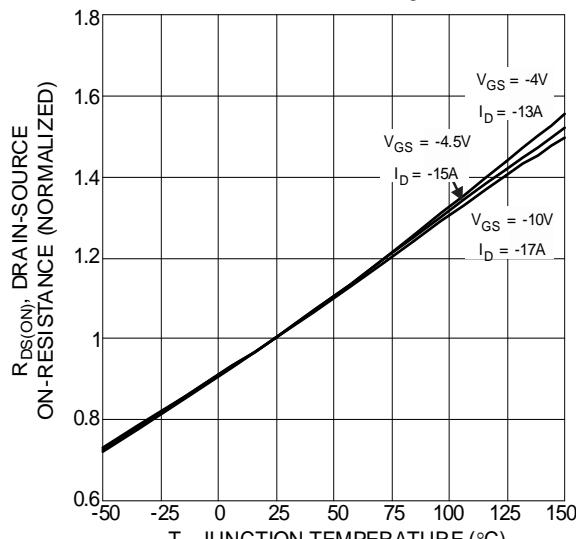


Figure 6 On-Resistance Variation with Temperature

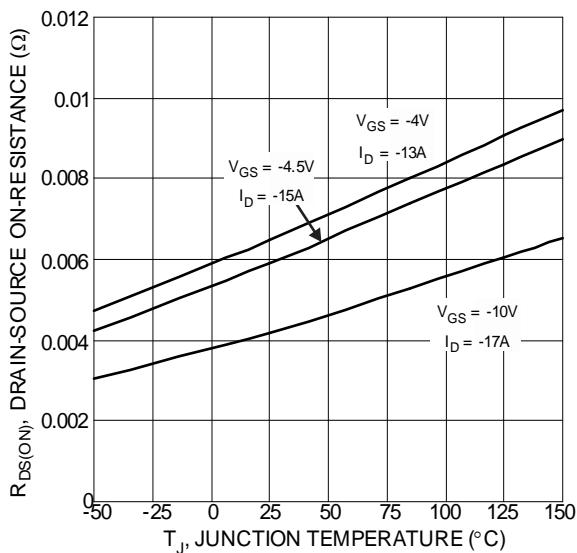


Figure 7 On-Resistance Variation with Temperature

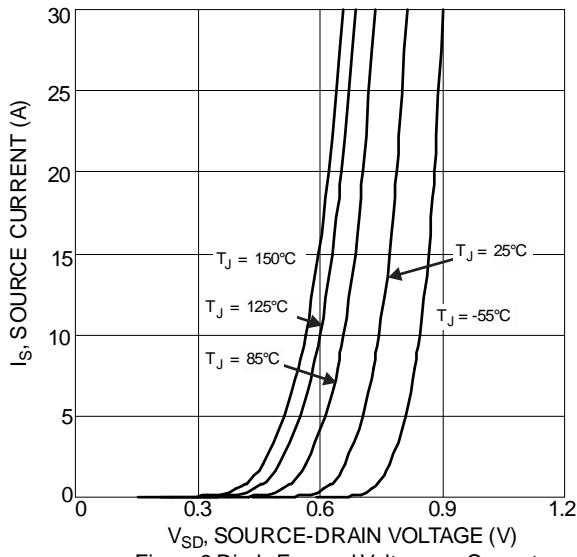


Figure 9 Diode Forward Voltage vs. Current

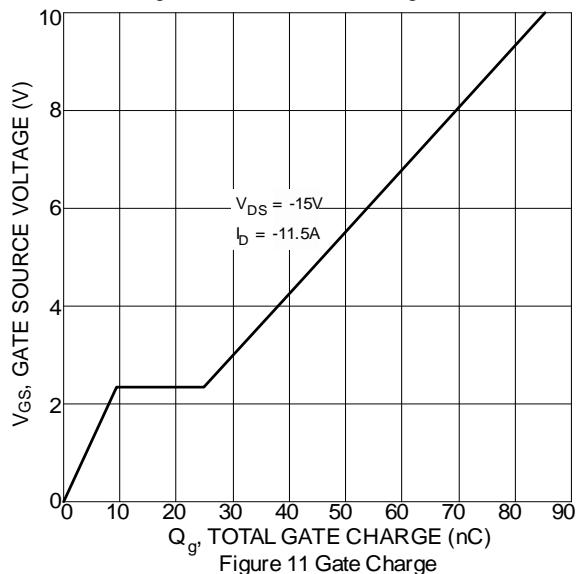


Figure 11 Gate Charge

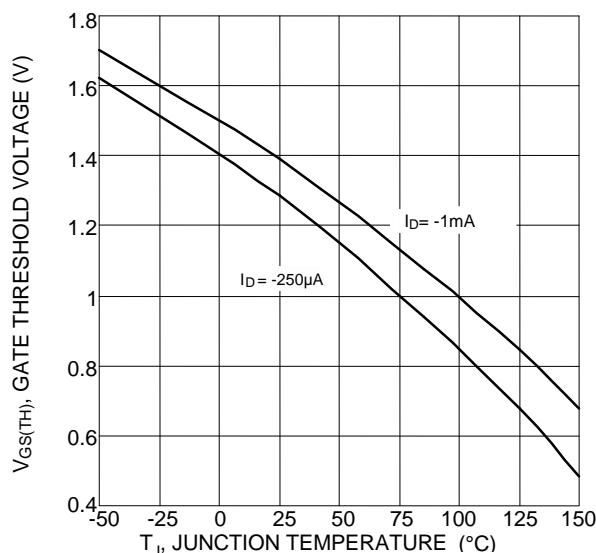


Figure 8 Gate Threshold Variation vs. Junction Temperature

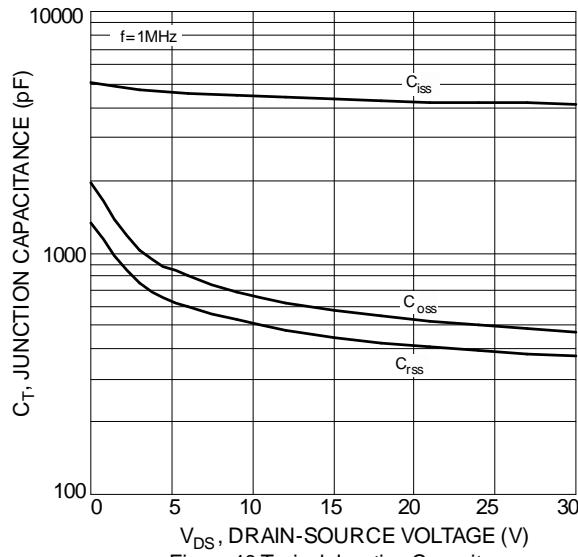


Figure 10 Typical Junction Capacitance

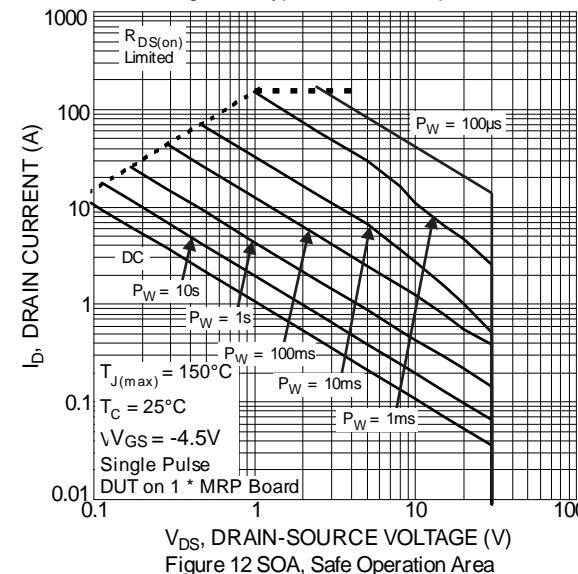


Figure 12 SOA, Safe Operation Area

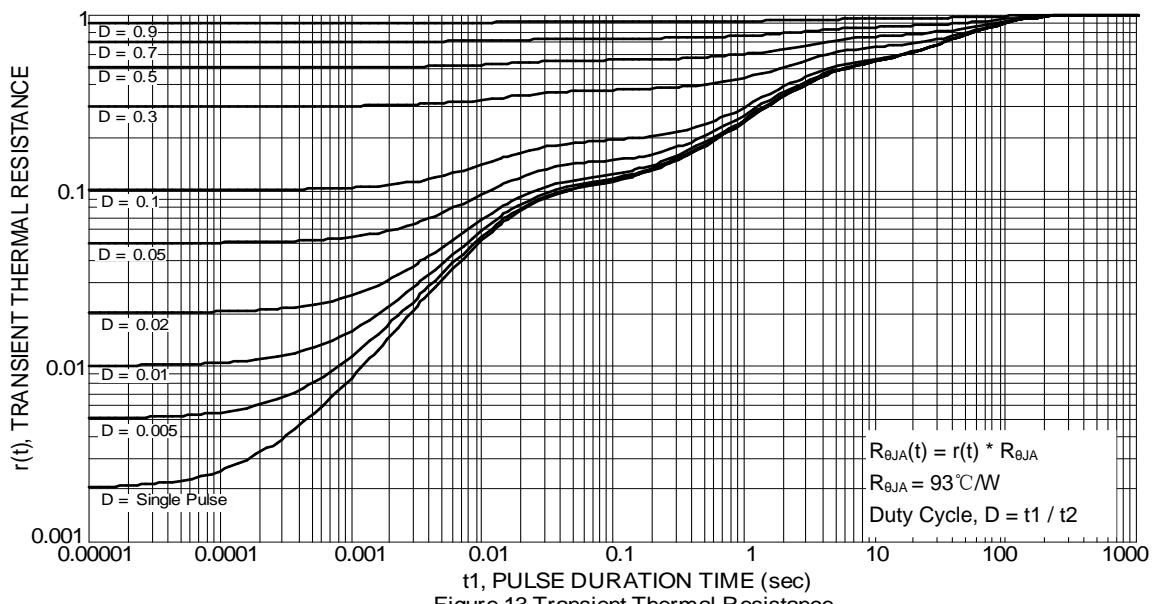
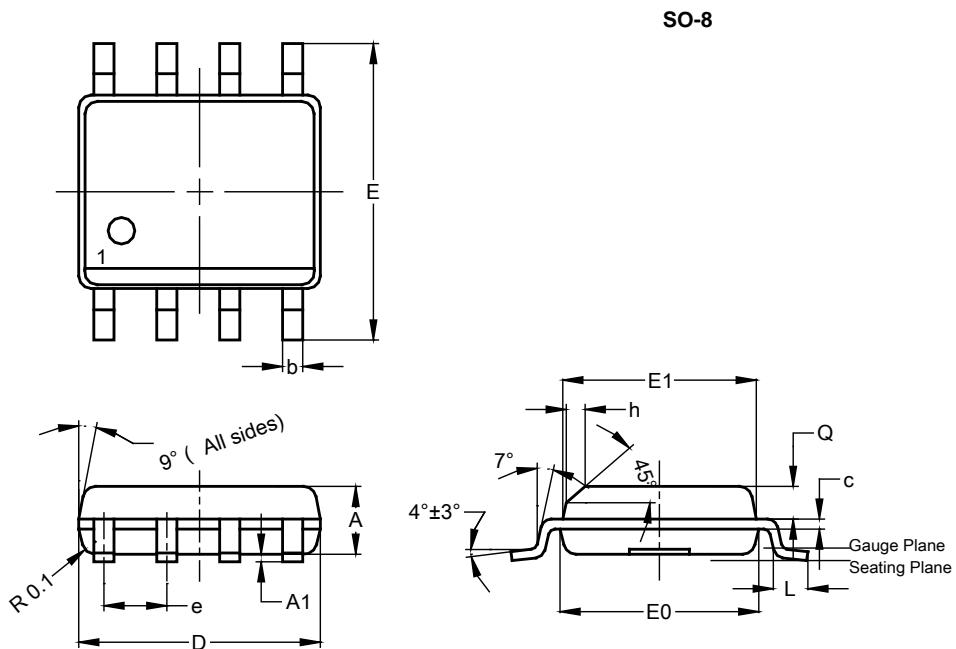


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

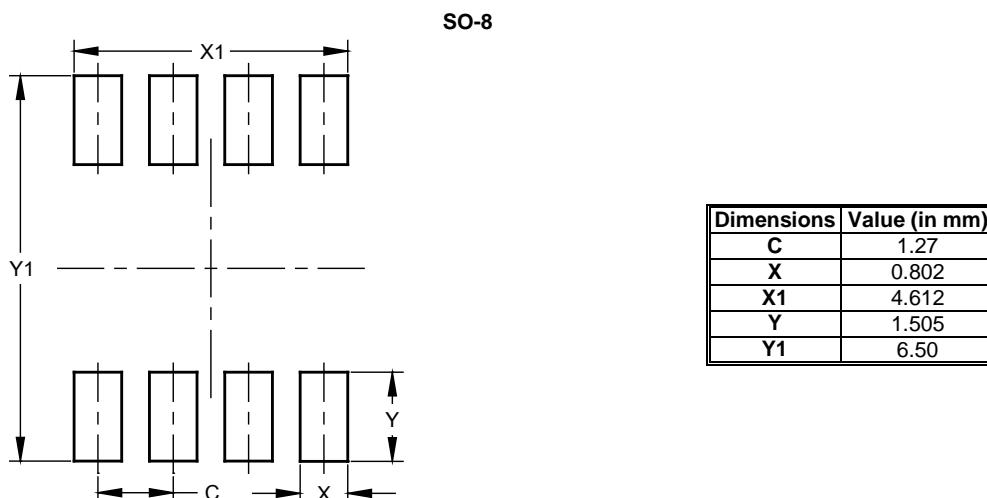


SO-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	—	—	1.27
h	—	—	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



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