MP9928

4V-60V Input, Current Mode, Synchronous Step-Down Controller

The Future of Analog IC Technology

DESCRIPTION

The MP9928 is a high-voltage, synchronous step-down switching regulator controller that can directly step down voltages from up to 60V. The MP9928 uses PWM current control architecture with accurate cycle-by-cycle current limiting. It is capable of driving dual N-channel MOSFET switches.

AAM Mode (Advanced asynchronous mode) enables non-synchronous operation and PFM mode to optimize light load efficiency.

The operating frequency of MP9928 can be programmed by an external resistor or synchronized to an external clock for noise-sensitive applications. Fault protections are available including a precision output over voltage protection (OVP), output over current protection (OCP), and thermal shutdown.

The MP9928 is available in TSSOP20-EP package and QFN-20 (3mmx4mm) package.

FEATURES

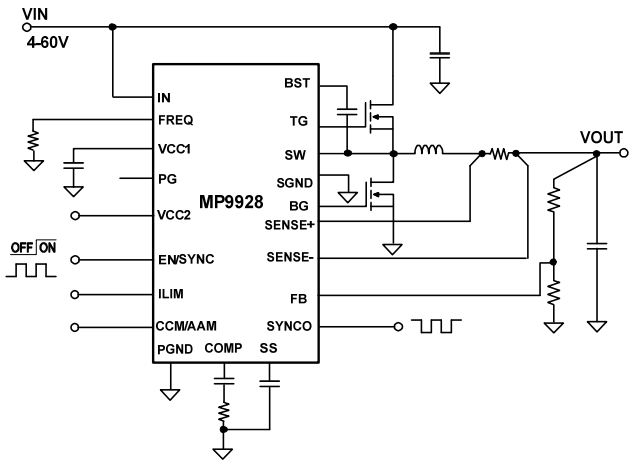
- Wide 4V to 60V Operating Input Range
- Dual N-Channel MOSFET Driver
- Low Dropout Operation: Maximum Duty Cycle at 99.5%
- Programmable Frequency Range: 100kHz - 1000kHz
- 180° Out-of-Phase SYNCO
- External Soft-Start and PG Pin
- Selectable Cycle-by-Cycle Current Limit
- Output Over Voltage Protection
- Internal LDO with Externally Power Supply Option
- Programmable CCM and AAM Pulse-Skipping Mode
- Accuracy Over Temperature Protection
- TSSOP20-EP package and QFN-20 (3mmx4mm) Package

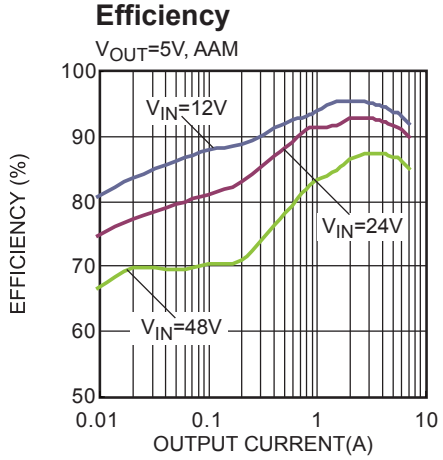
APPLICATIONS

- PD Power Supply in PoE System
- USB Dedicated Charging Port (DCP)
- Industrial Control Systems
- Power Supply for Linear Chargers

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Package	Top Marking
MP9928GF*	TSSOP-20 EP	*See Below*
MP9928GL**	QFN-20 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP9928GF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP9928GL–Z)

TOP MARKING (MP9928GF)

MPSYYWW

MP9928

LLLLLLLLL

MP9928: product code of MP9928GF;
MPS: MPS prefix;
YY: year code;
WW: week code:
LLLLLLLLL: lot number;

TOP MARKING (MP9928GL)

MPYW

9928

LLL

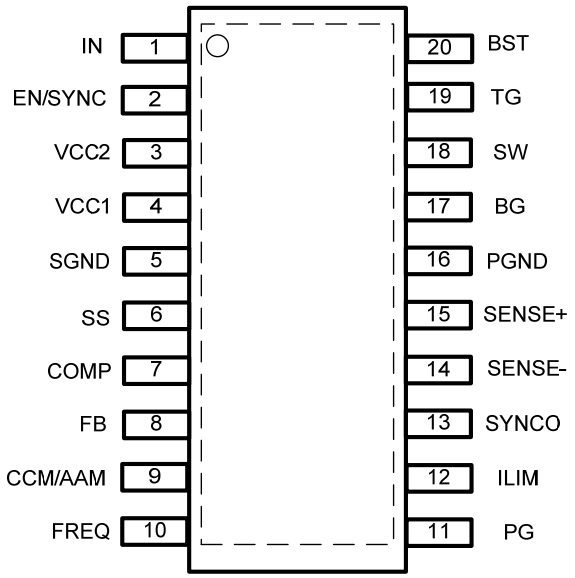
9928: product code of MP9928GL;
MP: MPS prefix;
Y: year code;
W: week code:
LLL: lot number;

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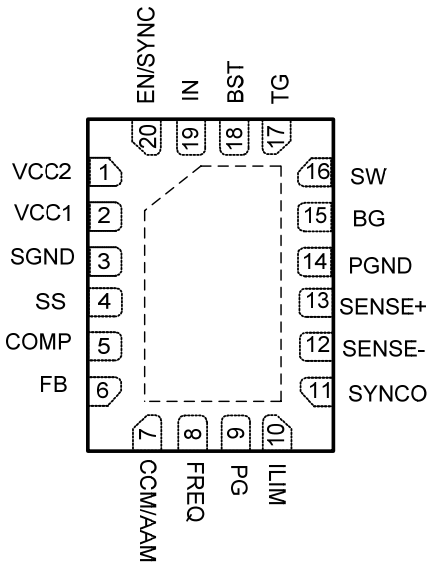
PACKAGE REFERENCE

TOP VIEW



TSSOP-20 EP

TOP VIEW



QFN-20 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}) ..... -0.3V to 65V
EN/SYNC ..... -0.3V to 50V
SW ..... -0.3V(-4V for <20ns) to 65V
BST - SW ..... -0.3V to 6.5V
Supply voltage (VCC1) ..... -0.3V to 6.5V
External supply voltage (VCC2) ..... -0.3V to 15V
SENSE + / - ..... -0.3V to 28V
Differential sense (SENSE+ to SENSE-) ..... -0.7V to +0.7V
TG ..... V_{SW} - 0.3V to V_{BST} + 0.3V
BG ..... -0.3V to VCC1 + 0.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C)(2)
TSSOP-20 EP 3.1W
QFN-20 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +175°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 60V(4)
Output voltage (V_{OUT}) ..... ≤24V
Supply voltage for (VCC2) ..... 5V to 12V
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
TSSOP-20 EP	40	8	°C/W
QFN-20 (3mmx4mm)	48	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) UVLO_rising is 5V but UVLO_falling is lower than 4V, so input must be >5V for startup, and after start up MP9928 can work down to 4V input voltage.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to 125°C, EN = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} UVLO threshold (rising)	IN_{UV_RISING}			4.5	5	V
V_{IN} UVLO threshold (falling)	$IN_{UV_FALLING}$			3.7	3.95	V
V_{IN} UVLO hysteresis	IN_{UV_HYS}			800		mV
V_{IN} supply current with VCC2 bias	I_{Q_VCC2}	VCC2 = 12V, external bias		25	40	µA
V_{IN} supply current without VCC2 bias	I_Q	VCC2 = 0, V_{FB} = 0.84V, V_{AAM} = 5V, SENSE+ = SENSE- = 0.3V		750	1000	µA
V_{IN} AAM current	I_{Q_AAM}	V_{AAM}=0.6V, V_{FB}=0.84V, SENSE+ = SENSE- = 0.3V		250	350	µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V		0.5	3	µA
V_{CC} Regulator						
VCC1 regulator output voltage from V_{IN}	$VCC1_{VIN}$	VIN > 6V		5		V
VCC1 regulator load regulation from V_{IN}		Load = 0 to 50mA, VCC2 floating or connects to GND		1	3	%
VCC1 regulator output voltage from VCC2	$VCC1_{VCC2}$	VCC2 > 6V		5		V
VCC1 regulator load regulation from VCC2		Load = 0 to 50mA, VCC2 = 12V		1	3	%
VCC2 UVLO threshold (rising)	$VCC2_{RISING}$			4.7	4.92	V
VCC2 UVLO threshold (falling)	$VCC2_{FALLING}$			4.45		V
VCC2 threshold hysteresis	$VCC2_{HYS}$			250		mV
VCC2 supply current	I_{VCC2}	V_{AAM} = 5V, V_{FB} = 0.84V, VCC2 = 12V		800	1200	µA
		V_{AAM} = 0.6V, V_{FB} = 0.84V, VCC2 = 12V		200	300	µA
Feedback (FB)						
Feedback voltage	V_{FB}	4V ≤ V_{IN} ≤ 60V, T_J=25°C	0.792	0.800	0.808	V
		4V ≤ V_{IN} ≤ 60V, T_J=-40°C to 125°C	0.788	0.800	0.812	V
Feedback current	I_{FB}	V_{FB} = 0.84V		10		nA
Enable (EN)						
Enable threshold (rising)	V_{EN_RISING}		1.16	1.22	1.28	V
Enable threshold (falling)	$V_{EN_FALLING}$		1.03	1.09	1.15	V
Enable threshold hysteresis	V_{EN_TH}			130		mV
EN input current	I_{EN}	V_{EN} = 2V		2		µA
Enable turn-off delay	T_{OFF}		10	15		µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to 125°C, EN = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Oscillator and Sync						
Operating frequency	F_{SW}	R_{Freq} = 65kΩ	240	300	360	kHz
Foldback operating frequency	$F_{SW_FOLDBACK}$	V_{FB} = 0.1V		50%		F_{SW}
Maximum programmable frequency	F_{SWH}		1000			kHz
Minimum programmable frequency	F_{SWL}				100	kHz
Sync/EN frequency range	F_{SYNC}		100		1000	kHz
Sync/EN voltage rising threshold	V_{SYNC_RISING}		2			V
Sync/EN voltage falling threshold	$V_{SYNC_FALLING}$				0.35	V
Current Sense						
Current sense common mode voltage range	$V_{SENSE+/-}$		0		24	V
Current limit sense voltage	V_{ILIMIT}	I_{LIM} = GND, V_{SENSE+} = 3.3V	15	25	35	mV
		I_{LIM} = VCC1, V_{SENSE+} = 3.3V	40	50	60	mV
		I_{LIM} = FLOAT, V_{SENSE+} = 3.3V	65	75	85	mV
Reverse current limit sense voltage	V_{REV_ILIMIT}	I_{LIM} = GND, V_{SENSE+} = 3.3V		8		mV
		I_{LIM} = VCC1, V_{SENSE+} = 3.3V		17		
		I_{LIM} = FLOAT, V_{SENSE+} = 3.3V		24		
Valley current limit	V_{VAL_ILIMIT}	I_{LIM} = GND, V_{SENSE+} = 3.3V		22.5		mV
		I_{LIM} = VCC1, V_{SENSE+} = 3.3V		47.5		
		I_{LIM} = FLOAT, V_{SENSE+} = 3.3V		72.5		
Input current of sensor	I_{SENSE}	$V_{SENSE+/-(CM)}$ = 0V		-45		µA
		$V_{SENSE+/-(CM)}$ = 3.3V		115		µA
		$V_{SENSE+/-(CM)}$ > 5V		150		µA
Soft Start (SS)						
Soft-start source current	I_{SS}	SS = 0.5V	2	4	6	µA
Error Amplifier						
Error amp transconductance	G_m	∆ V = 5mV		500		µA/V
Error amp open loop DC gain(6)	A_O			70		dB
Error amp sink/source current	I_{EA}	FB = 0.7/0.9V		±30		µA
Protection						
Over-voltage threshold	V_{OV}		110%	115%	120%	V_{FB}
Over-voltage hysteresis	V_{OV_HYS}			10%		V_{FB}
Thermal shutdown(7)				170		°C
Thermal shutdown hysteresis(7)				20		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to 125°C, EN = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
TG pull-up resistor	R_{TG_PULLUP}	Source 20mA		2		Ω
TG pull-down resistor	R_{TG_PULLDN}	Sink 20mA		1		Ω
BG pull-up resistor	R_{BG_PULLUP}	Source 20mA		3		Ω
BG pull-down resistor	R_{BG_PULLDN}	Sink 20mA		1		Ω
Dead time	T_{Dead}	C_{Load} = 3.3nF		60		ns
TG maximum duty cycle	D_{max}	V_{FB} = 0.7V	98	99.5		%
TG minimum on time(7)	$T_{ON_MIN_TG}$			92		ns
BG minimum on time	$T_{ON_MIN_BG}$			175	250	ns
Power Good						
Power good low	V_{PG_Low}	I_{SINK} = 4mA		0.1	0.3	V
PG rising threshold	PG_{Vth_RSING}	V_{OUT} rising	85%	90%	96.5%	V_{FB}
		V_{OUT} falling	101%	107%	112.5%	
PG falling threshold	$PG_{Vth_FALLING}$	V_{OUT} falling	81%	87%	92.5%	V_{FB}
		V_{OUT} rising	105%	110%	116.5%	
PG threshold hysteresis	PG_{Vth_HYS}			3%		V_{FB}
Power good leakage	I_{PG_LK}	PG = 5V			2	μA
Power good delay	T_{PG_delay}	PG rising and falling		25		μs
AAM/CCM						
AAM output current	I_{AAM}	R_{Freq} = 65 kΩ		9.2		μA
CCM required AAM threshold voltage	V_{CCM_TH}		2.3			V

NOTES:
6) Guaranteed by design, not tested.
7) Guaranteed by characterization, not production tested.

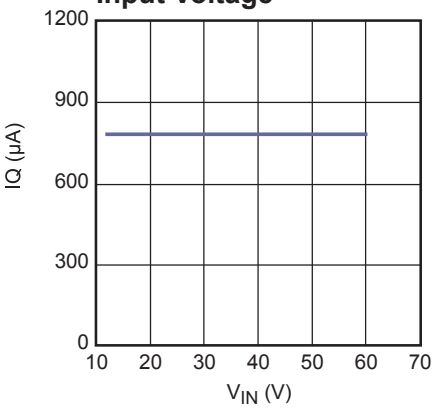
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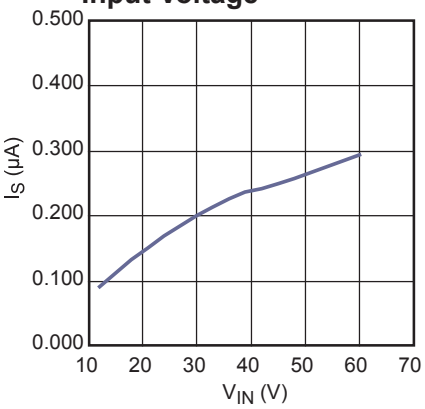
TYPICAL CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

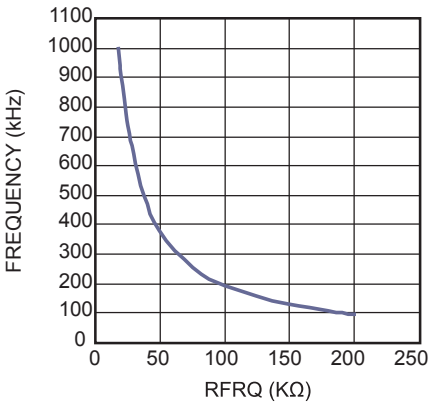
Quiescent Current vs. Input Voltage



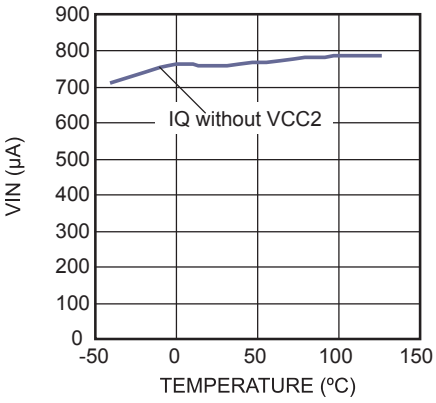
Shutdown Current vs. Input Voltage



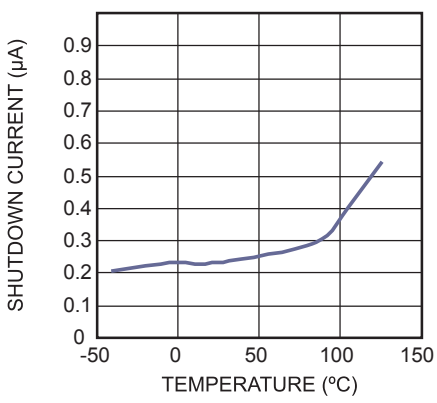
Frequency vs. Resistor



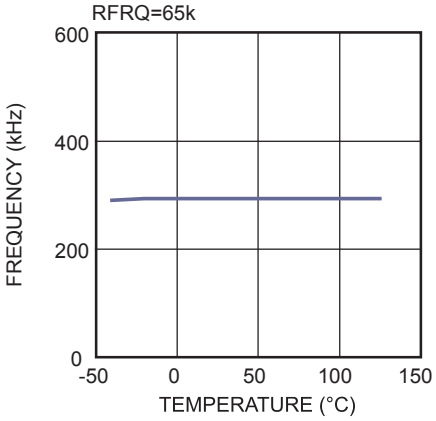
Quiescent Current vs. Temperature



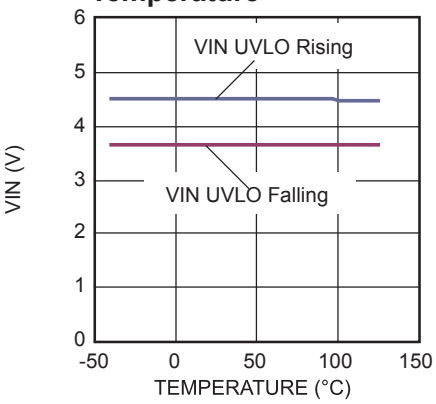
Shutdown Current vs. Temperature



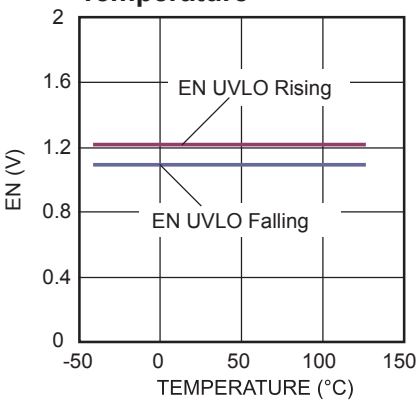
Frequency vs. Temperature



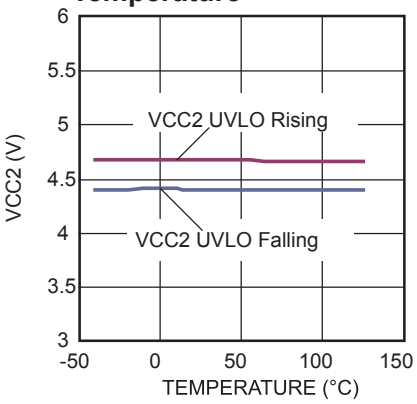
VIN UVLO vs. Temperature



EN UVLO vs. Temperature



VCC2 UVLO vs. Temperature



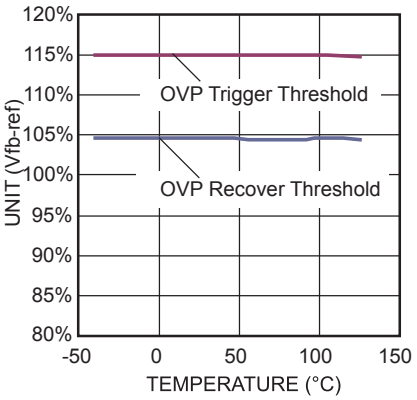
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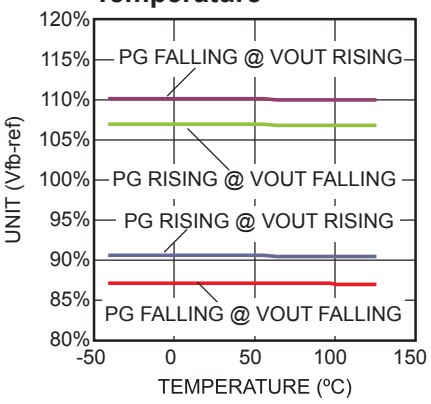
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

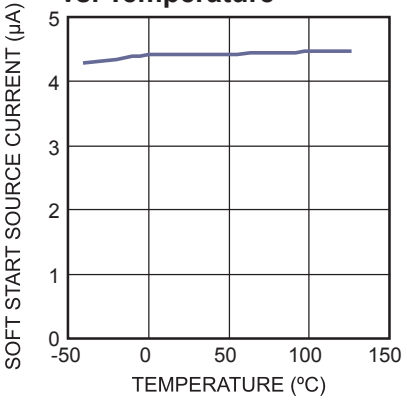
OVP vs. Temperature



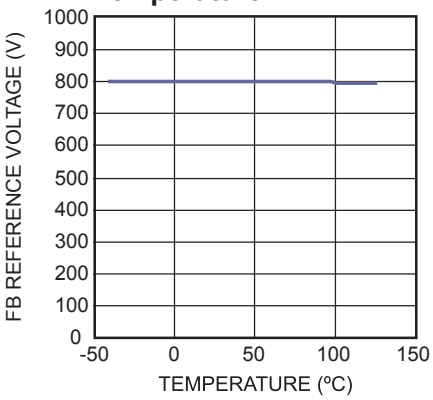
PG Threshold vs. Temperature



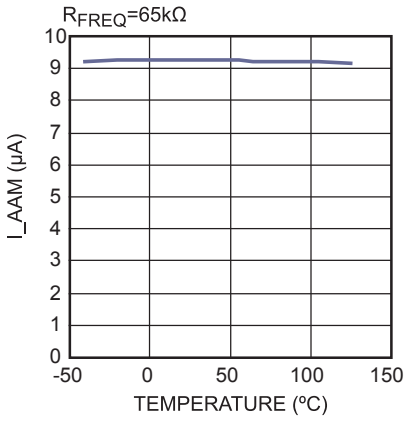
Soft Start Source Current vs. Temperature



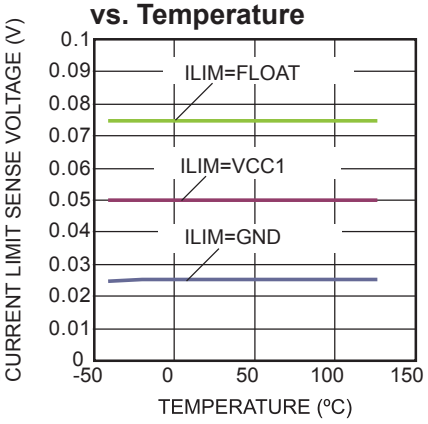
FB Reference Voltage vs. Temperature



I_AAM vs. Temperature



Internal Current Limit vs. Temperature



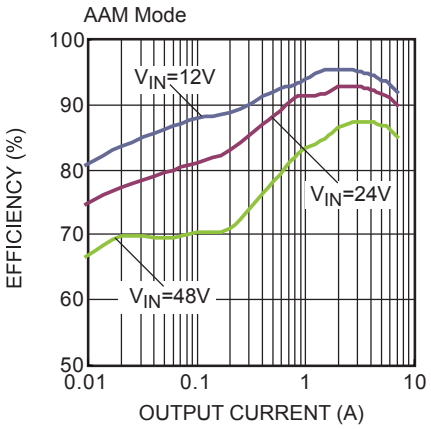
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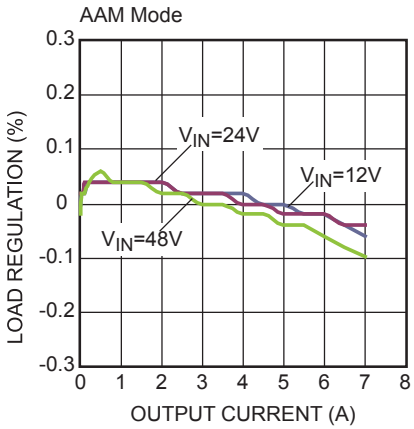
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

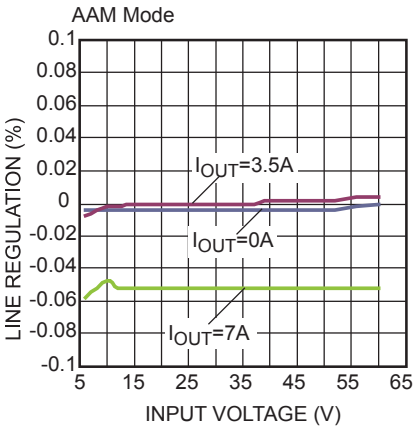
Efficiency



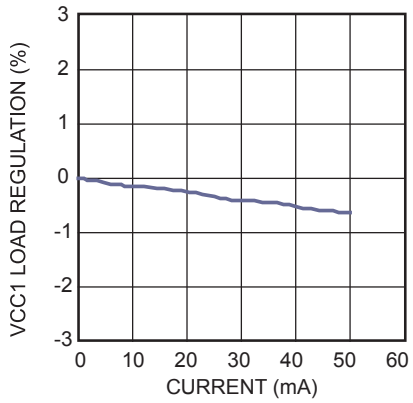
Load Regulation



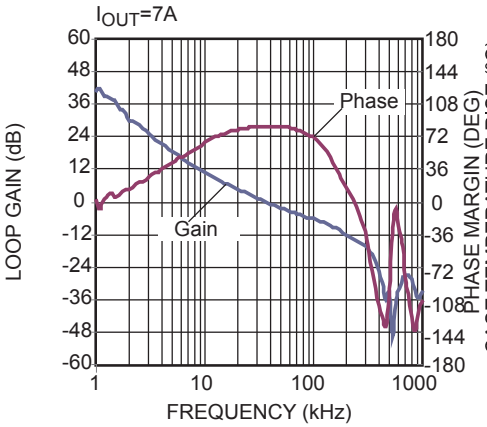
Line Regulation



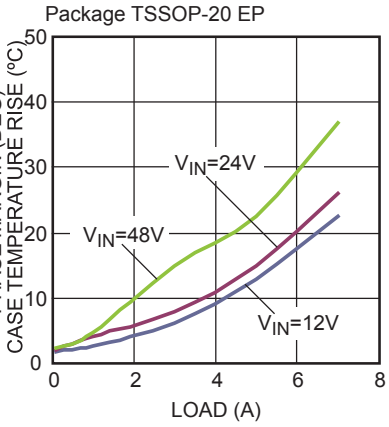
VCC1 Load Regulation



Bode Plot



Case Temp Rise



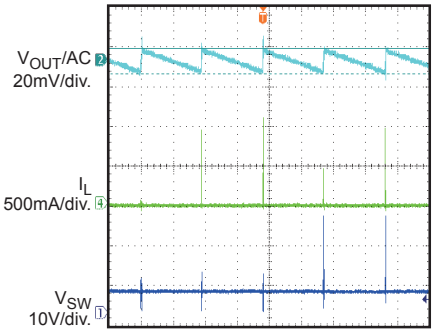
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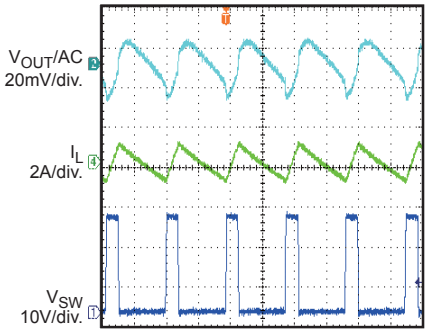
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, AAM Mode, T_A = +25°C, unless otherwise noted.

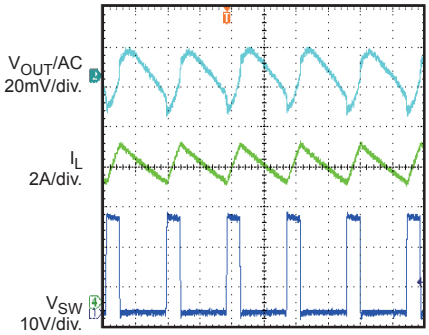
Steady State
I_{OUT}=0, AAM Mode



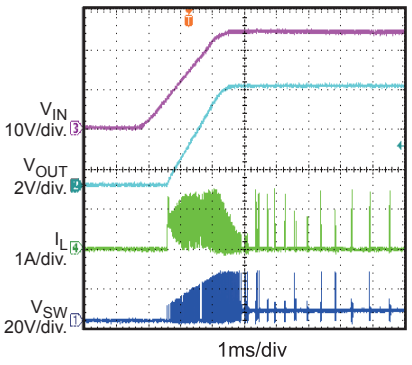
Steady State
I_{OUT}=0, Forced CCM Mode



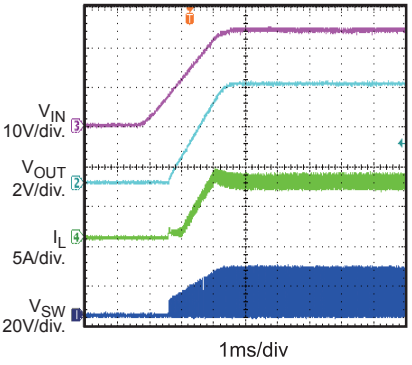
Steady State
I_{OUT}=7A



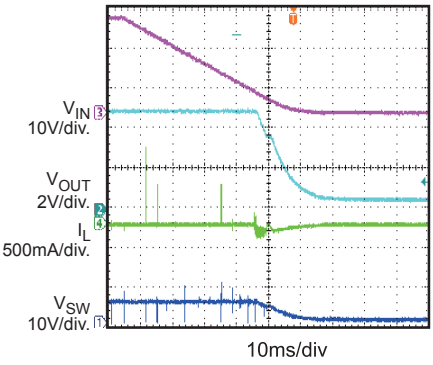
Start-Up Through VIN
I_{OUT}=0



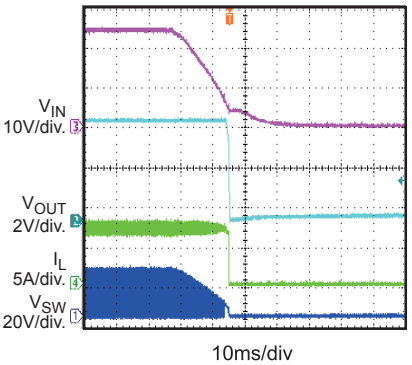
Start-Up Through VIN
I_{OUT}=7A



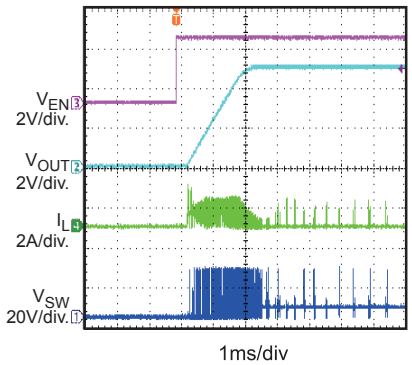
Shutdown Through VIN
I_{OUT}=0



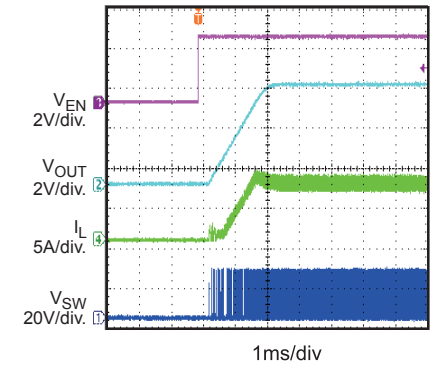
Shutdown Through VIN
I_{OUT}=7A



Start-Up Through EN
I_{OUT}=0



Start-Up Through EN
I_{OUT}=7A



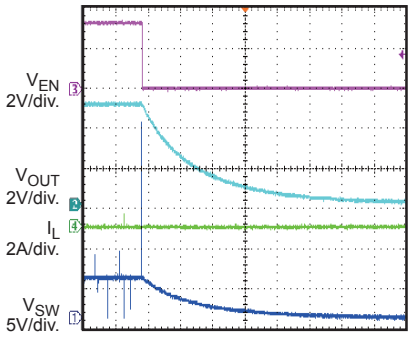
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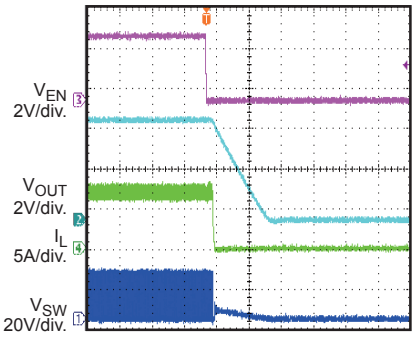
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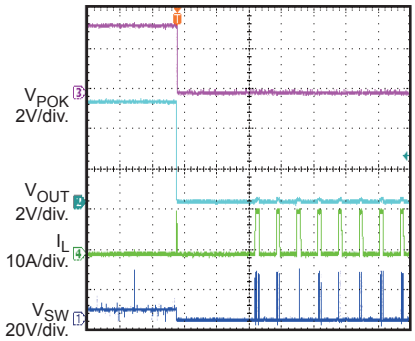
Shutdown Through EN
I_{OUT}=0



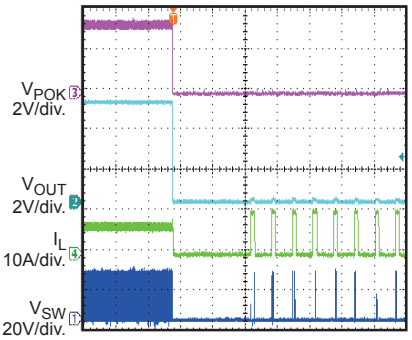
Shutdown Through EN
I_{OUT}=7A



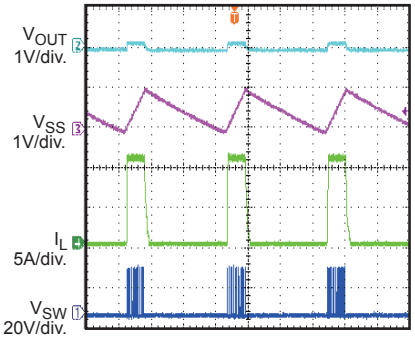
SCP Entry
I_{OUT}=0 to short circuit



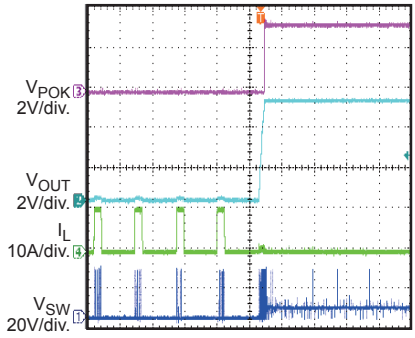
SCP Entry
I_{OUT}=7A to short circuit



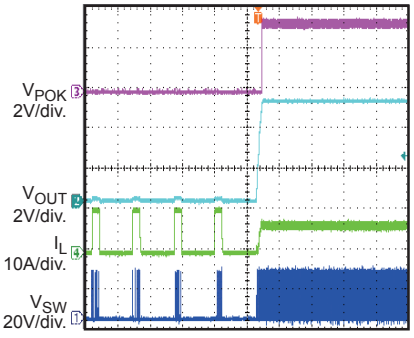
SCP Steady State



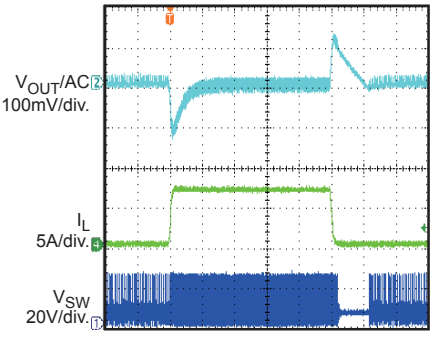
SCP Recovery
short circuit to I_{OUT}=0



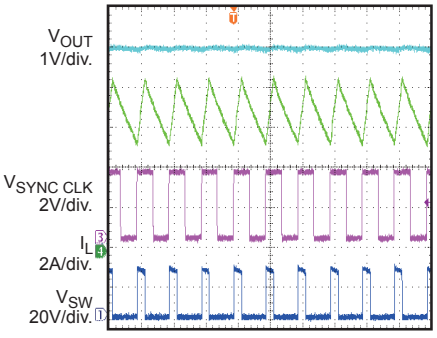
SCP Recovery
short circuit to I_{OUT}=7A



Load Transient
I_{OUT}=0.2A<->7A, 1.6A/µs



SYNC Function
V_{IN}=24V/V_{OUT}=5V/7A, F_{SYN}=100kHz



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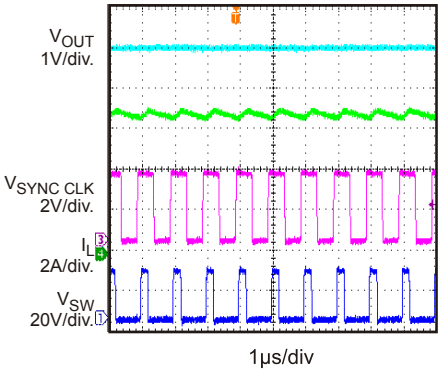
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, AAM Mode, T_A = +25°C, unless otherwise noted.

SYNC Function

V_{IN}=24V/V_{OUT}=5V/7A, F_{SYN}=1MHz



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PIN FUNCTIONS

TSSOP Pin #	QFN Pin #	Name	Description
1	19	IN	Input supply. The MP9928 operates from a 4V to 60V input. Ceramic capacitor is needed to prevent large voltage spikes from appearing at the input.
2	20	EN/SYNC	Enable input. The threshold is 1.22V with 130mV of hysteresis, and it is used to implement an input under voltage lockout (UVLO) function externally. If an external sync clock is applied to this pin, internal clock will follow the sync frequency.
3	1	VCC2	External power supply for the internal VCC1 regulator. It will disable the power from V_{IN} as long as VCC2 is higher than 4.7V. Do not connect >12V power supply to this pin. Connecting VCC2 pin to external power supply will reduce power dissipation and thus increases efficiency.
4	2	VCC1	Internal bias supply. Decouple with a 1μF ceramic capacitor or greater ceramic capacitor. But the capacitance should be no more than 4.7μF.
5	3	SGND	Low noise signal ground reference.
6	4	SS	Soft-start control input. This pin is used to program the soft-start period with an external capacitor between SS to SGND.
7	5	COMP	COMP is used to compensate the regulation control loop. Connect an RC network from COMP to GND to compensate for the regulation control loop.
8	6	FB	Feedback. This is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal +0.8V reference to set the regulation voltage.
9	7	CCM/AAM	Continuous conduction mode/advanced asynchronous mode set pin. Connect this pin to VCC1 pin or float can set the part operates in CCM mode. Connecting an appropriate external resistor from this pin to GND to make AAM at low level, can set the part operates in AAM. The AAM voltage should be no less than 480mV.
10	8	FREQ	Connect a resistor between FREQ and GND to set the switching frequency.
11	9	PG	Power good output. The output of this pin is open drain.
12	10	ILIM	Current sense voltage limit set. The voltage at this pin sets the nominal sense voltage at maximum output current. There are three fixed options (float, connect to VCC1 or connect to GND.)
13	11	SYNCO	outputs a clock which are 180° out-of-phase with internal Oscillator Clock or external Synchronize Clock when part works in CCM or DCM(but not Sleep mode) for dual channel co-pack. SYNCO outputs DC voltage in other cases(Sleep mode, Low Dropout mode, Fault protections, etc.).
14	12	SENSE-	Negative input for the current sense. The sensed inductor current limit threshold is determined by status of ILIM pin.
15	13	SENSE+	Positive input for the current sense. The sensed inductor current limit threshold is determined by status of ILIM pin.
16	14	PGND	Power ground reference for the internal low side switch driver and the VCC1 regulator circuit. Connect this pin directly to the negative terminal of the VCC1 decoupling capacitor.

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PIN FUNCTIONS *(continued)*

TSSOP Pin #	QFN Pin #	Name	Description
17	15	BG	Bottom gate driver output. Connect this pin to the gate of the synchronous N-channel MOSFET.
18	16	SW	Switch node. Reference for the V_{BST} supply and high current returns for bootstrapped switch.
19	17	TG	Top gate drive. The TG pin drives the gate of the top N-channel MOSFET. The TG driver draws power from the BST capacitor and returns to SW pin, providing a true floating drive to the top N-channel MOSFET.
20	18	BST	Bootstrap. This pin is the positive power supply for the internal floating high side MOSFET driver. Connect a bypass capacitor between this pin and SW pin. A diode from VCC1 to this pin charges the BST capacitor when the low side switch is off.

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BLOCK DIAGRAM

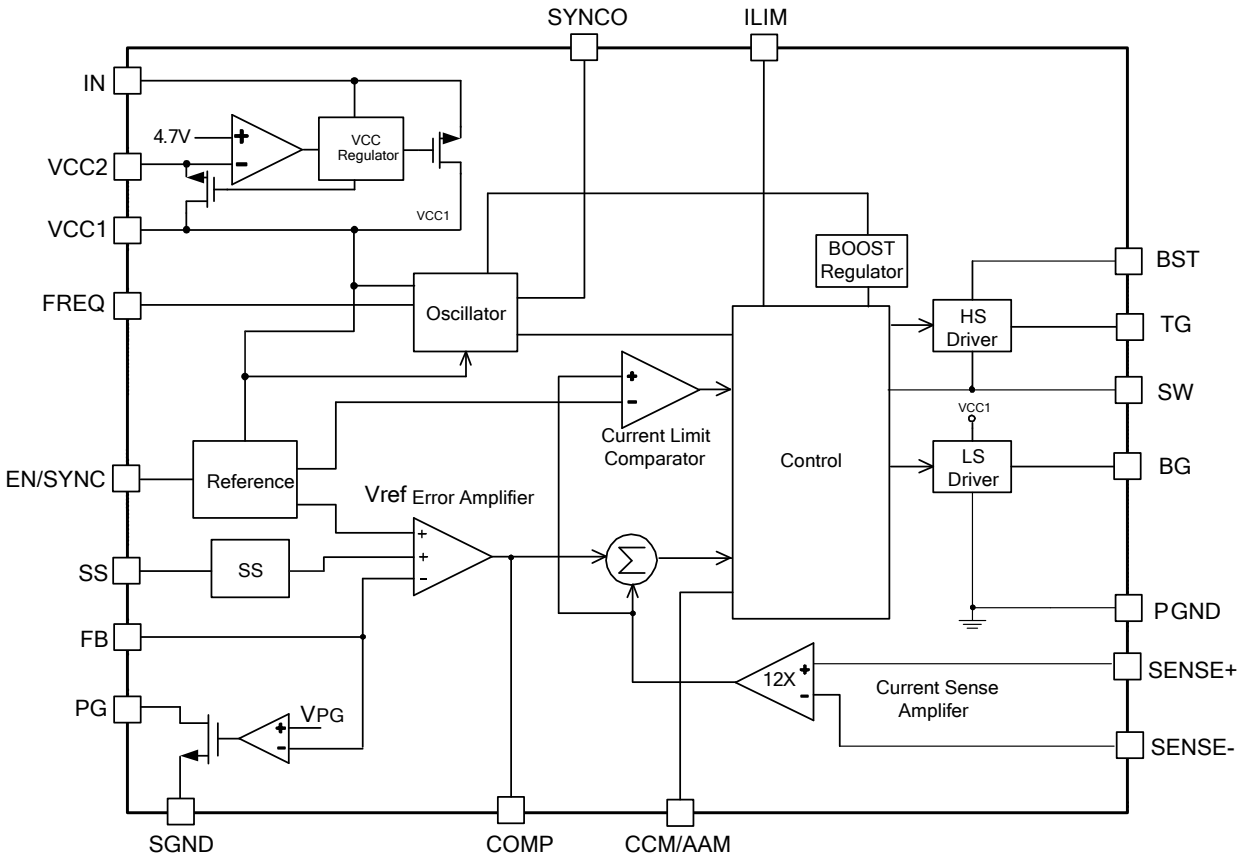


Figure 1: Block Diagram

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OPERATION

Overview

The MP9928 is a high-performance, step down, synchronous DC/DC converter controller IC with a wide input range. It implements current mode, switching frequency programmable control architecture to regulate the output voltage with external N-channel MOSFET switches.

The MP9928 senses the voltage at FB pin. The difference between the voltage on this pin and an internal 0.8V reference is amplified to generate an error voltage on COMP pin which is used as a threshold for the current sense comparator with a slope compensation ramp.

Under normal load condition, the controller operates in full PWM mode. At the beginning of each oscillator cycle, the top gate driver is enabled. Top gate turns on for a period determined by the duty cycle. When the top gate turns off, the bottom gate turns on after a dead time and stays on until the beginning of the next clock cycle.

There is an optional power save mode for light load or no load conditions, and see details in the following section.

AAM Mode

MP9928 employs AAM mode functionality to optimize the efficiency during light-load or no-load conditions. This AAM mode can be optional enabled when CCM/AAM pin is at a low level by connecting an appropriate resistor to GND to make sure that V_{AAM} is no less than 480mV.

$$V_{AAM}\,(mV) = I_{AAM}\,(\mu A) \times R_{AAM}\,(k\Omega)$$

Where, I_{AAM} is AAM pin output current, it can be shown below.

$$I_{AAM}\,(\mu A) = 600\,(mV) / R_{FREQ}\,(k\Omega)$$

R_{FREQ} is the resistor from FREQ to SGND, for given operating frequency, and its value is shown in 'Programmable Switching Frequency' section.

AAM is disabled when CCM/AAM pin is floating or connected to VCC1.

If AAM is enabled, the MP9928 will firstly enter non-synchronous operation as long as the inductor current approaches zero at light-load. If the load is further decreased or even no load that make COMP voltage below the voltage of AAM threshold at about V_{AAM}+V_{OFFSET}, MP9928 enters AAM mode, where V_{AAM} is the voltage of CCM/AAM pin and V_{OFFSET} is about 720mV. In AAM mode, the internal clock is reset every time when V_{COMP} crosses over AAM threshold, and the crossover time is taken as benchmark of the next clock. When the load increases and the DC value of V_{COMP} is higher than AAM threshold, the operation mode is DCM or CCM which has a constant switching frequency.

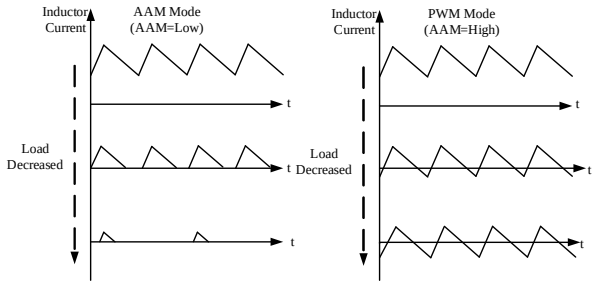


Figure 2: AAM and PWM

Floating Driver and Bootstrap Charging

The floating top gate driver is powered by an external bootstrap capacitor (C_{BST}), which is normally refreshed when the high-side MOSFET (HS-FET) turns off. This floating driver has its own UVLO protection. This UVLO's rising threshold is 3.05V with a hysteresis of 170mV.

VCC1 Regulator and VCC2 Power Supply

Both high-side and low-side MOSFET drivers and most of the internal circuitries are powered from the VCC1 regulator. An internal low dropout linear regulator supplies VCC1 power from VIN, usually a 1μF to 4.7μF ceramic capacitor is recommended from VCC1 to GND.

If VCC2 pin is left open or connected to a voltage <4.45V, an internal 5V regulator supplies VCC1 power from VIN. If VCC2 is >4.7V, the 5V regulator is disabled and another 5V regulator is triggered that supplies VCC1 power from VCC2. If 4.5V<VCC2<5V, the 5V regulator is in dropout and VCC1 is

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approximately equal to VCC2. When VCC2 is greater than 5V (max. is 12V), VCC1 is regulated to 5V. Using the VCC2 power supply allows the VCC1 power to be derived from a high-efficiency external source, such as one of the MP9928's switching regulator outputs.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two input voltages. This output current is then used to charge or discharge the external compensation network to form the COMP voltage, which is used to control the power MOSFET current. Adjusting the compensation network from COMP pin to GND could optimize the control loop for good stability or fast transient response.

Current Limit Function

There are three fixed options for current limit setting: When ILIM connects to GND, the current limit sense voltage is set to 25mV; when ILIM connects to VCC1, the current limit sense voltage is set to 50mV; when ILIM pin floats, the current limit sense voltage is set to 75mV.

When the peak value of the inductor current exceeds the set current limit threshold, meanwhile, output voltage starts to drop until FB is 62.5% of the reference. MP9928 enters hiccup mode to periodically restart the part. Meanwhile, the frequency would be lowered when FB<0.5V. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issues. The MP9928 exits the hiccup mode once the over-current condition is removed.

Low Dropout Operation

At low dropout mode, the MP9928 is designed to operate at HS max duty on mode as long as the voltage across BST - SW is greater than 3.05V, this improves dropout. When the voltage from BST to SW drops below 3.05V, an under-voltage lockout (UVLO) circuit turns off the high-side MOSFET (HS-FET), and at the same time, the low-side MOSFET (LS-FET) turns on to refresh the BST capacitor. After the BST capacitor voltage is re-charged, the HS-FET turns on again to regulate the output. Since the BST capacitor voltage is greater than 3.05V, the HS-FET can remain on for more switching cycles than are required to refresh the BST capacitor, thus increasing the effective duty cycle of the switching regulator. The low dropout operation makes the MP9928 suitable for application such as automotive cold-crank.

Power Good Function

The MP9928 includes an open-drain power good output that indicates whether the regulator's output is within about ±10% of its nominal value. When the output voltage falls outside this range, the PG output is pulled to low. It should be connected to a voltage source of no more than 5V through a resistor (e.g., 100kΩ). The PG delay time is 25μs.

PG pin has self-driving capability, if MP9928 is off and PG pin is pulled up to another DC power source through a resistor, the PG pin can also be pulled low by self-driving circuit.

Soft Start

The soft start (SS) is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage ramping up from 0V to 0.8V. When it is lower than the internal reference (REF), SS voltage overrides REF, so the error amplifier uses SS voltage as the reference. When SS voltage is higher than REF, REF regains control.

An external capacitor connected from SS to SGND is charged from an internal 4μA current source, producing a ramped voltage. The soft-start time (t_{SS}) is set by the external SS capacitor and can be calculated by below formula:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)}$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.8V), and I_{SS} is the 4μA SS charge current. There is no internal SS capacitor.

SS will be reset when a fault protection happened except for output over voltage protection.

Output Over-Voltage Protection

MP9928 output voltage is monitored by FB voltage. If FB voltage is typically 10% higher than

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the reference, it'll trigger OVP. Once it triggers OVP, MP9928 will go into discharge mode, the HS-FET is turned off, and the LS-FET is turned on and keeps on until the reverse current limit is triggered, after LS-FET is turned off, inductor current will increase to 0. The LS-FET will be turned on again next clock cycle. MP9928 works at discharge mode until the over-voltage condition is cleared.

Enable

The MP9928 has a dedicated enable control pin. It uses a bandgap generated precision threshold of 1.22V. By pulling it high or low, the IC can be enabled or disabled. To disable the part, EN/SYNC must be pulled low for at least 15μs.

Tie EN to VIN through a resistor divider R16 and R17 to program the VIN start up threshold (see Figure 3). The EN threshold is 1.08V (falling edge), so the VIN falling UVLO threshold is 1.08V x (1+ R16/R17).

In high input design, EN pin voltage should not be greater than 50V.

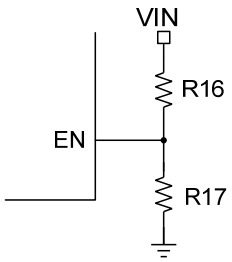


Figure 3: EN Resistor Divider

Synchronize

The MP9928 can be synchronized to an external clock range from 100kHz up to 1000kHz through EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge. The pulse width (both on and off) of external clock signal should be no less than 100ns.

Under-Voltage Lockout

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient input supply voltages. The MP9928 UVLO rising threshold is about 4.5V while its falling threshold is about 3.7V.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. When the silicon die temperature is higher than 170°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 150°C, the chip is enabled again.

Start-Up and Shutdown

If both VIN and EN are higher than their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents. And then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitry.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signal path is firstly blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subjected to this shutdown command.

Pre-Bias Start-Up

For MP9928, at startup, If SS<FB, which means output has pre-bias voltage, neither TG nor BG would be turned on until SS is greater than FB.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage.

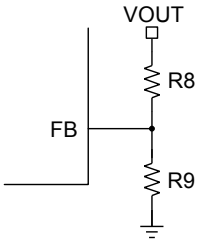


Figure 4: V_{OUT} Setting Resistor

If R8 is determined, then R9 can be calculated with below formula:

$$R_9 = \frac{R_8}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R8 (kΩ)	R9 (kΩ)
3.3	37.4 (1%)	12 (1%)
5	63.4 (1%)	12 (1%)
12	169 (1%)	12 (1%)

Setting Current Sensing

The MP9928 has three fixed options for current limit setting: when ILIM pin is connected to GND, the current sense voltage is set to 25mV; when ILIM pin is connected to VCC1, the current sense voltage is set to 50mV and when ILIM pin is floating, the current limit sense voltage is set to 75mV.

The current sense resistor, R_{SENSE}, monitors the inductor current. Its value is chosen based on the current limit threshold. The relationship between the peak inductor current I_{pk} and R_{SENSE} is:

$$R_{SENSE} = \frac{V_{ILIMIT}}{Ipk} \quad (5)$$

The typical values for R_{SENSE} are in the range of 5mΩ to 50mΩ.

Programmable Switching Frequency

There are a number of variables to consider when choosing the switching frequency. A high frequency will increase switching losses and gate charge losses, while a lower frequency requires more inductance and capacitance, which results in larger real estate and also higher cost. It is a trade off between power loss and passive component size. Additionally, in noise-sensitive applications, the switching frequency should be out of a sensitive frequency band.

The MP9928's frequency can be programmed from 100kHz to 1000kHz with a resistor from FREQ to SGND. The value of R_{FREQ} for a given operating frequency can be calculated by:

$$R_{FREQ}(k\Omega) = \frac{20000}{f_s(kHz)} - 1$$

To get f_S = 500kHz, set R_{FREQ} to 39kΩ.

Table 2: Frequency vs. Resistor

Resistor (kΩ)	Frequency (kHz)
65	300
39	500
19	1000

V_{CC} Regulator Connection

VCC1 can be powered from both VIN and VCC2. If connecting VCC2 to an external power supply to improve the overall efficiency, this VCC2 should be larger than 4.7V but smaller than 12V.

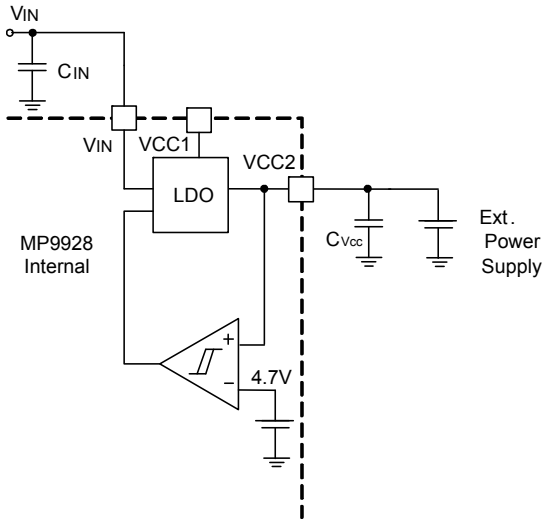


Figure 5: V_{CC} Power from External Supply

If V_{OUT} is higher than 4.7V but ≤12V, VCC2 can be connected to V_{OUT} directly.

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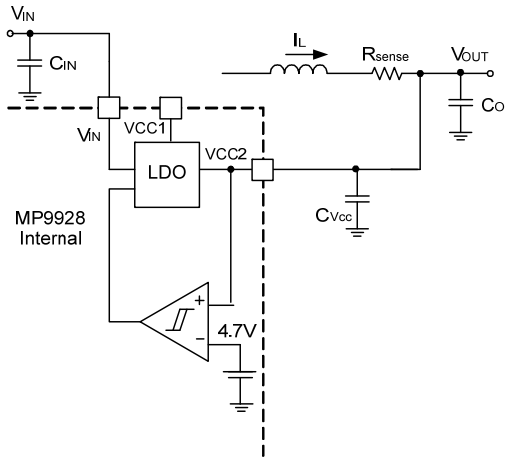


Figure 6: V_{CC} Power from V_{OUT}

Selecting the Inductor

An inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. A larger value inductor results in less ripple current and a lower output ripple voltage. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current. Generally, choose the inductor ripple current approximately 30% of the maximum load current. Then the inductance value can be then be calculated by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Where, I_{LOAD} is the load current.

Input Capacitor Selection

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The selection of the input capacitor is mainly based on its maximum ripple current capability. The RMS value of the ripple current flowing through the input capacitor can be described as:

$$I_{RMS} = I_{LOAD} \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{LOAD}/2$. So, the input capacitor selected must be capable of handling this ripple current.

Output Capacitor Selection

The output capacitor keeps the output voltage ripple small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right)$$

Where C_O is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For tantalum or electrolytic capacitor application, the ESR dominates the impedance at the switching frequency. So the above formula can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

Compensation Components

The MP9928 employs current-mode control for easy compensation and fast transient response. The COMP pin controls system stability and transient response. The COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop is:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_O \times \frac{V_{FB}}{V_{OUT}}$$

Where A_O is the error-amplifier voltage gain 3000V/V, G_{CS} is the current-sense transconductance, $1/(12xR_{SENSE})$ (A/V), and R_{LOAD} is the load resistor value.

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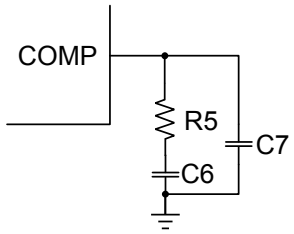


Figure 7: COMP External Compensation

The system has two important poles: one from the compensation capacitor (C6) and the output resistor of error amplifier and the other tone from the output capacitor and the load resistor. These poles can be calculated by:

$$f_{P1} = \frac{G_m}{2\pi \times C6 \times A_O}$$

$$f_{P2} = \frac{1}{2\pi \times Co \times R_{LOAD}}$$

Where G_m is the error-amplifier transconductance 500μA/V, and Co is the output capacitor.

The system has one important zero due to the compensation capacitor and the compensation resistor (R5). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C6 \times R5}$$

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero can be located at:

$$f_{ESR} = \frac{1}{2\pi \times Co \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C7) and the compensation resistor can compensate for the effect of the ESR zero. This pole is calculated by:

$$f_{P3} = \frac{1}{2\pi \times C7 \times R5}$$

The goal of the compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, and higher crossover frequencies lead to system instability. Set the crossover frequency to ~0.1×f_{SW}.

Follow the below steps to design the compensation:

1. Choose R5 to set the desired crossover frequency:

$$R5 = \frac{2\pi \times Co \times f_C}{G_m \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where, f_C is the desired crossover frequency.

2. Choose C6 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) < 0.25 x f_C to provide a sufficient phase margin. C6 is then:

$$C6 > \frac{4}{2\pi \times R5 \times f_C}$$

3. C7 is required if the ESR zero of the output capacitor is located at <0.5×f_{SW}, or the following relationship is valid:

$$\frac{1}{2\pi \times Co \times R_{ESR}} < \frac{f_{SW}}{2}$$

If this is the case, use C7 to set the pole (f_{P3}) at the location of the ESR zero. Determine C7:

$$C7 = \frac{Co \times R_{ESR}}{R5}$$

PCB Layout Considerations

For a controller, the layout is always an important step in design. A poor layout would result in reduced performance, EMI problems, resistive loss and even system instability. Following step would help to guarantee a good layout design:

1. Input power loop between input capacitor, high-side MOSFET and low-side MOSFET should be as small as possible, SW trace should be as possible as short and wide. At the same time, one small decoupling capacitor should be placed close to the IC's IN and GND pins.
2. Feedback loop should be far away from noise source such as SW trace, the feedback divider resistor should be as close as possible to FB and GND pin.

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3. Route the sensing traces (SENSE+, SENSE-) in paired way with smallest closed area. Avoid crossing noisy areas such as SW or high-side gate drive traces. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
4. A short and wide type resistor is recommend for current sense.
5. VCC1 and VCC2 capacitors should be placed as close as possible to VCC1 pin and VCC2 pin.
6. Layout the gate drive traces as directly as possible. Layout the forward and return traces close together, either running side by side or on top of each other on adjacent layers to minimize the inductance of the gate drive path.
7. The ground return of input/output capacitor should be tied close with large GND copper area, and then connect to IC GND pin through single point.
8. For heavy load, suggest layout large copper, more layers and more vias for heat sink.

Figure 8 shows the recommended components place for MP9928 in TSSOP20-EP package. Figure 9 shows the recommended components place for MP9928 in QFN20 package. For the layout, the corresponding schematic can be found on Figure 10.

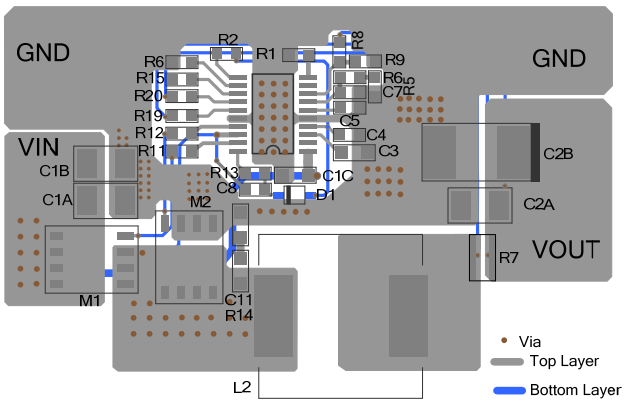


Figure 8: Layout Recommendation

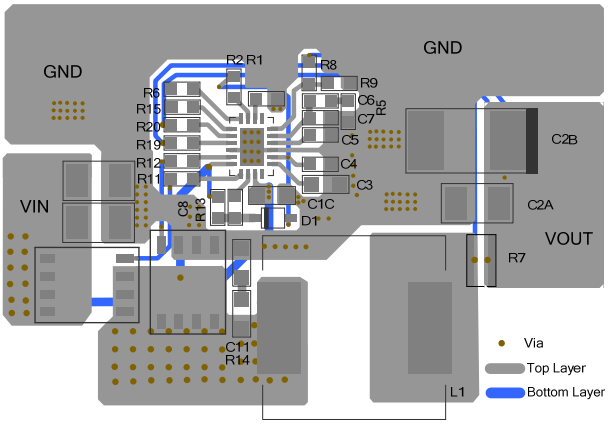


Figure 9: Layout Recommendation

Design Example

Below is a design example following the application guidelines for the following specifications:

Table 3: Design Example

V_{IN}	6V to 60 V
V_{OUT}	5V
I_{OUT}	0A-7A

The typical application circuit for V_{OUT} = 5V in Figure 10 shows the detailed application schematic, and it is the basis for the typical performance waveforms. This circuit can work down to 4V after startup, but V_{OUT} may drop when V_{IN} is low due to maximum duty cycle limit. For more detailed device applications, please refer to the related Evaluation Board Datasheets

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TYPICAL APPLICATION CIRCUITS

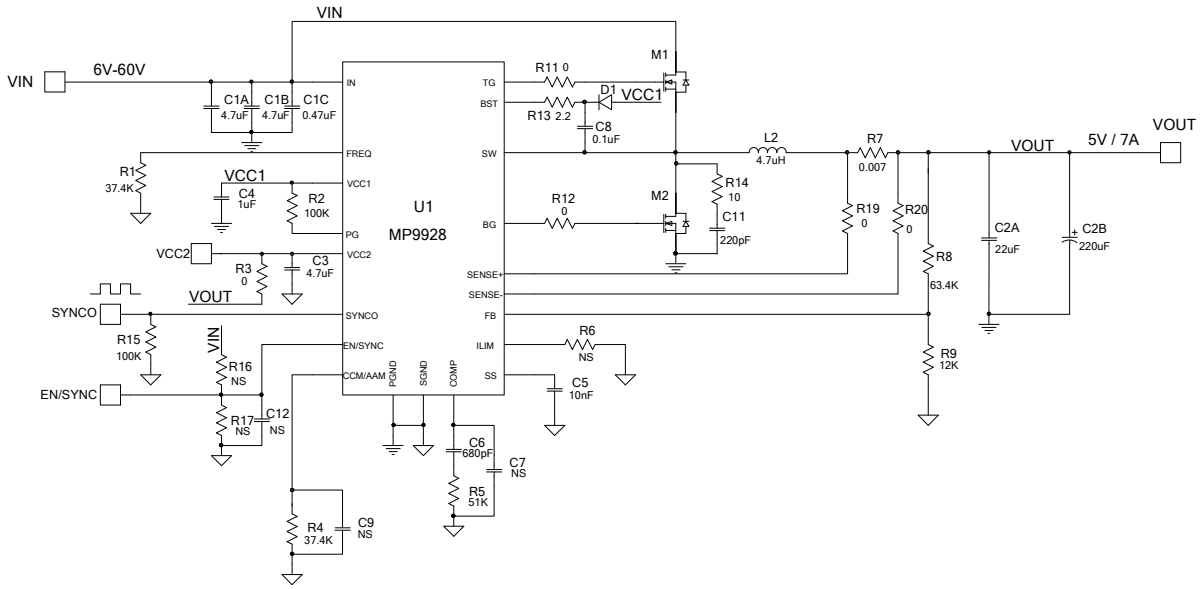


Figure 10: Application Circuit for 5V Output

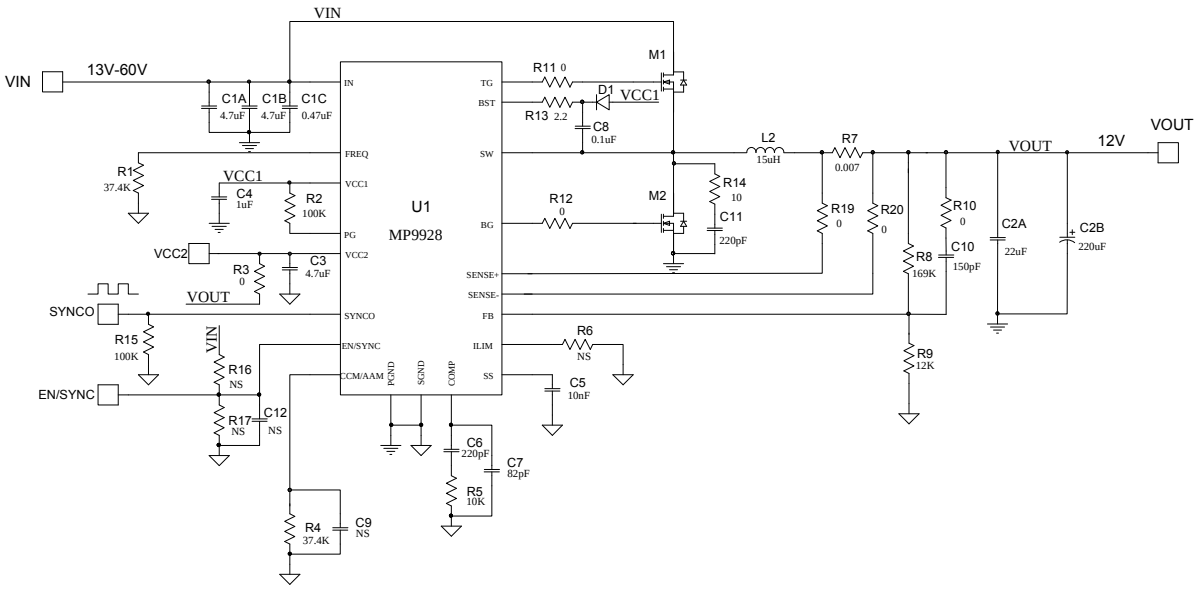


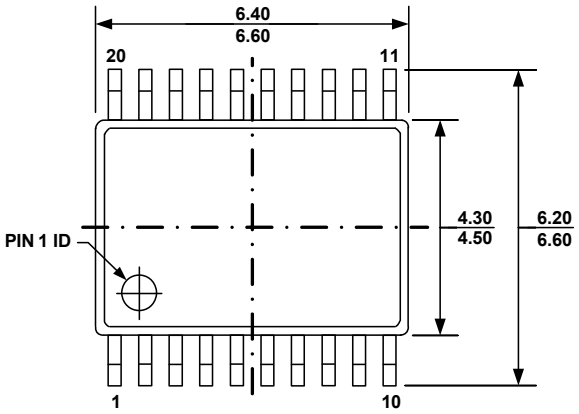
Figure 11: Application Circuit for 12V Output

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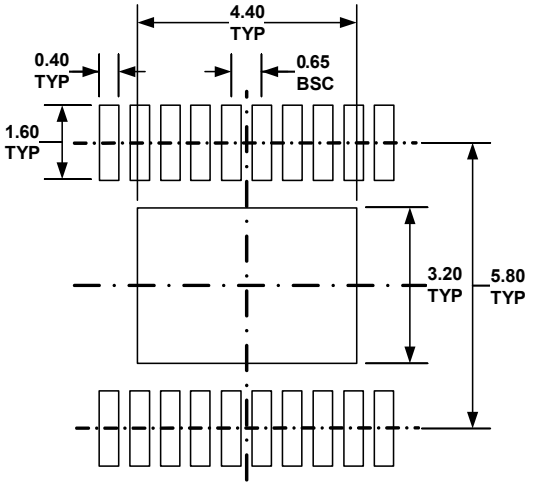
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PACKAGE INFORMATION

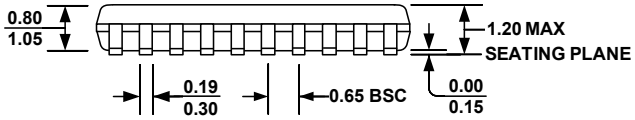
TSSOP-20 EP



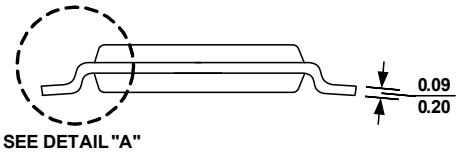
TOP VIEW



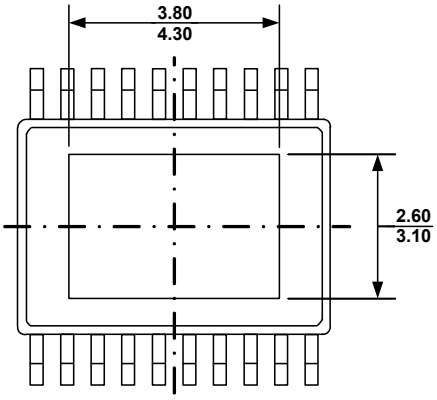
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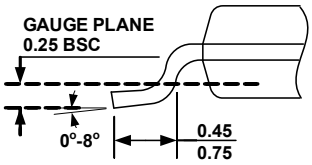
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

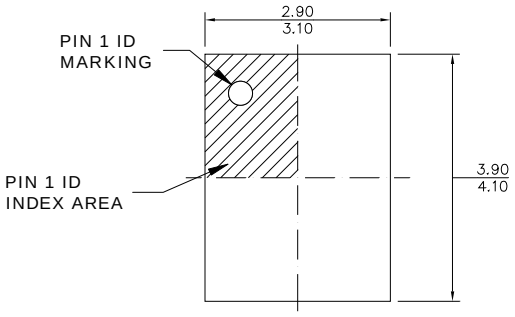
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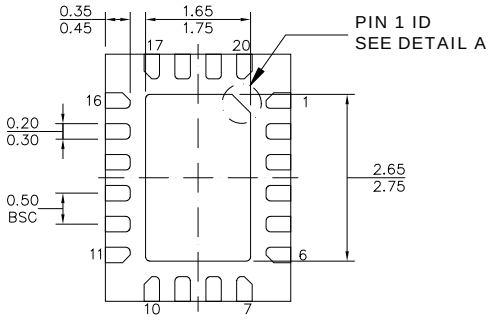
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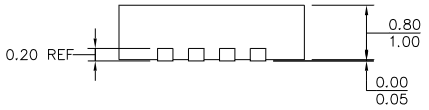
QFN-20 (3mmx4mm)



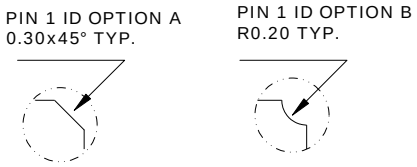
TOP VIEW



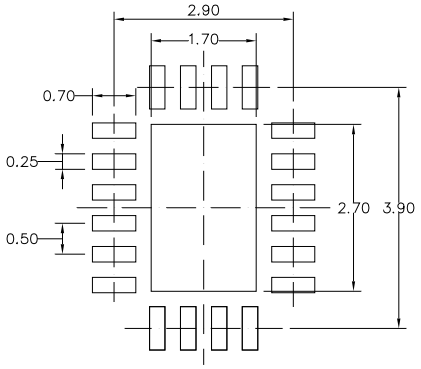
BOTTOM VIEW



SIDE VIEW



DETAIL A



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