LX7730-EVB Evaluation Board User Guide

Introduction

The LX7730-EVB evaluation board contains a ZIF socket to accept the included LX7730LMFQ-ES sample or other LX7730 ceramic parts as shipped with tie-bars. The GUI provided allows an LX7730's registers to be written and read using a PC via an included USB-to-serial-interface adapter.

This user guide also provides a walkthrough of the LX7730's internal blocks and operation using the GUI and a bare minimum set of equipment. It is intended to help an engineer get familiar with the functions of the LX7730 using a short practical exercise.

Kit Contents

- LX7730 Evaluation Board
- LX7730LMFQ-ES sample in protective case
- FTDI C232HM-DDHSL-0 USB to Multi Protocol Synchronous Serial Engine (MPSSE) dongle
- USB stick with support material

Ordering Information

Product	Order Number
LX7730-EVB Evaluation Board	LX7730-EVB

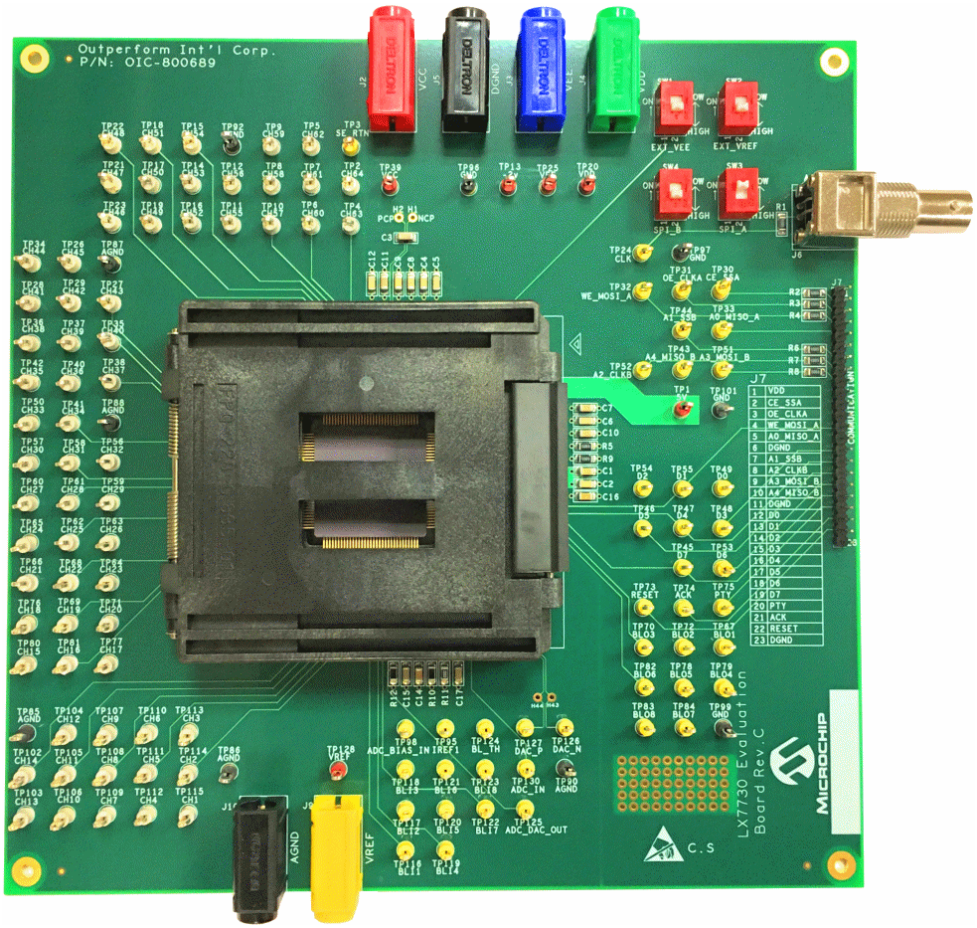


Figure 1. LX7730 Evaluation Board rev. C

1 Setup Procedure

1.1 Software

Copy the FTDI C232HM-DDHSL-0 USB MPSSE device drivers and LX7730 software GUI to your PC from the USB drive. Run CDM212364_Setup.exe to set up drivers for the FTDI C232HM-DDHSL-0 USB interface dongle. These drivers were obtained from https://www.ftdichip.com/Drivers/D2XX.htm. If you're not sure whether you have the drivers installed already, then try running LX7730 v0_2a.exe. If an error message appears, then the drivers are not installed.

1.2 Placing The LX7300 In The Socket

An LX7730 part may already be already installed in the socket on the LX7730-EVB. If it isn't installed, install it carefully. There are eight possible orientations of the LX7730 part in the socket, and only one is correct, so please double check. The LX7730 can be safely left installed between uses if the LX7730-EVB is stored/shipped in an antistatic bag.

With the socket open, pin 1 of the socket is the corner without a metal guide pin and is in the upper right corner nearest the four power banana jacks. The IC is placed upside down (bottom side up). Pin 1 can be identified on the package underside by an additional metal tab on the lead and the largest corner chamfer (Figure 2 below).

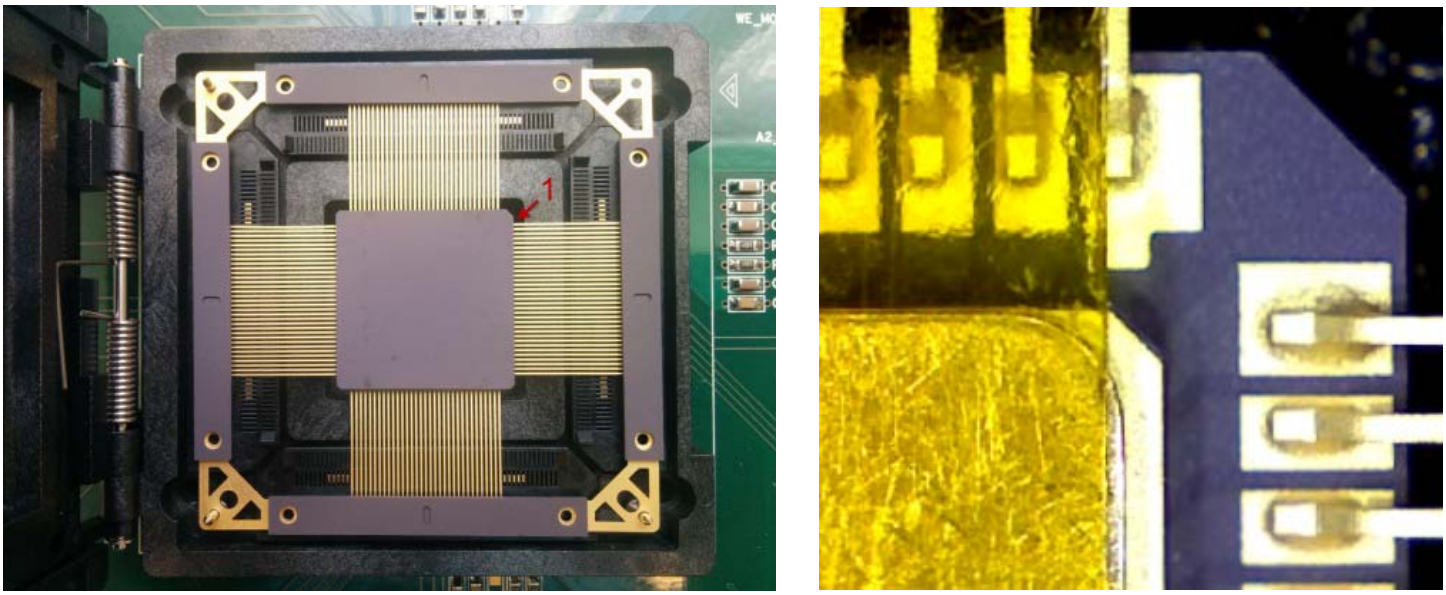


Figure 2. LX7300 ceramic packaged in socket (left), LX7300 pin 1 identification (right)

1.3 Hardware Connections

- Check that the red slide switch SW3 (bottom right) is up, and the remaining three switches down, as shown in the rev. B connection picture in Figure 1 on page 1. This configuration selects the SPI_A interface (used by the FTDI dongle), internal 5V VREF, and internal VEE supply
- Connect the black 4mm socket to the bench power supply's 0V output, usually black
- Connect the red 4mm socket to the bench power supply's positive output, usually red, after double checking that the power supply is set between 12V and 15V (13.5V is a good choice) and a current limit of 300mA. This is the LX7730's VCC main supply
- The FTDI USB interface dongle provides the LX7730's 3.3V VDD logic supply
- Connect a bench signal generator configured to provide a 500kHz square wave with unloaded amplitude 0V to 3.3V to the BNC CLK input. The LX7730-EVB does not use a 50Ω termination resistor. If the signal generator expects a 50Ω termination resistor (load), then the unloaded output voltage will double, so set the amplitude to 0V to 1.65V
- Plug the USB end of the FTDI dongle into your PC that will run the LX7730v0_2a.exe GUI software
- The FTDI USB interface dongle's flying leads are connected to the J7 connector, and the correct connections are shown in the Figure 3 or page 3. The grey, white, blue, and purple leads are unused. The only difference between boards rev. B and rev. C is that the rev. C board adds a pin to the 0.1" header J7 to simplify the connection to the FTDI USB interface by taking the red lead directly to a 0.1" header pin

- The pin order for the rev. B board is brown (top by BNC plug, pin 1), orange, yellow, green, black. The red lead connects to the green 4mm socket via an adapter cable.
- The pin order for the rev. C board is red (top by BNC plug, pin 1), brown, orange, yellow, green, black

Figure 3. FTDI Dongle's Connections to LX7730-EVB Rev. B board (left), LX7730-EVB Rev. C board (right)

2 LX7730 Tutorial

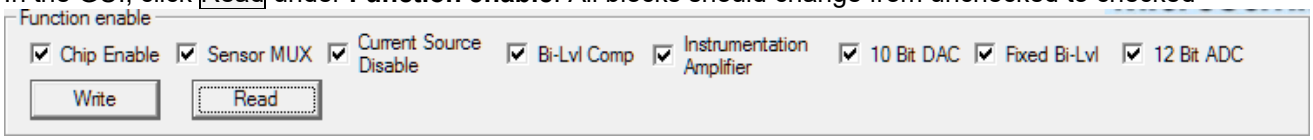
This section provides a walkthrough of the LX7730's internal blocks and operation. It is intended to help an engineer new to the LX7730 get familiar with the operation. It may also provide useful to check out the evaluation board and the supplied (or other) LX7730. Most of the walkthrough can be followed without having the 500kHz clock source. Section 3 covers the general instructions for operating the GUI if the walkthrough is skipped.

Apart from the setup described in section 1, a minimum of extra equipment is needed:

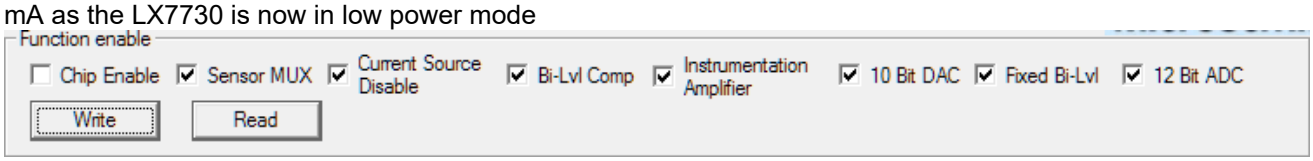
- A DVM or multimeter (the cheapest one will be fine) to check voltages and for basic functional testing
- Three short (200mm or more) test leads with a spring clip at each end for basic functional testing
- Two 1kΩ leaded resistors for basic functional testing of the 10-bit DAC and ADC

Additionally, the bench power supply should have a built in ammeter to monitor VCC current.

- Plug the FTDI dongle into a spare USB port of your PC, and start the GUI by running LX7730v0_2a.exe
  - This powers up the LX770's VDD logic supply to 3.3V from the USB interface
- Turn on the external bench power supply providing 12V to 15V to VCC
  - The LX7730-EVB is now powered up, and will draw about 60mA because the LX7730 powers up in operating mode
- Use the DVM to check that the:
  - 5V test point TP1 and the VREF output TP25 are both close to 5V
  - VEE output at TP25 is about -(VCC - 2)V, so about -11.5V if VCC was set to about 13.5V
  - m2v output at TP13 is about -2V
- In the GUI, click Read under **Function enable**. All blocks should change from unchecked to checked



- Now uncheck **Chip Enable** under **Function enable**, and click Write. The current consumption should drop to a few mA as the LX7730 is now in low power mode



- If the ADC is going to be used, connect a 500kHz square wave with unloaded amplitude 0V to 3.3V to the BNC
- The LX7730-EVB is now set up

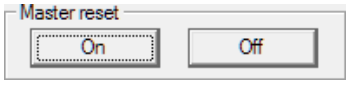
2.1 Basic Functional Testing and Demonstration

The functional testing uses a DVM, two 1kΩ resistors, and three short (200mm or more) test leads with a spring clip at each end. The test leads are use to connect resistors and test points together on the LX7730-EVB. The 500kHz signal generator isn't required for checking out the BLI/BLO comparators (Section 2.1.2) or the 10-bit DAC (Section 2.1.3).

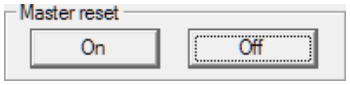
2.1.1 Reset the LX7730

First of all we reset the LX7730 to clear all registers to the default settings.

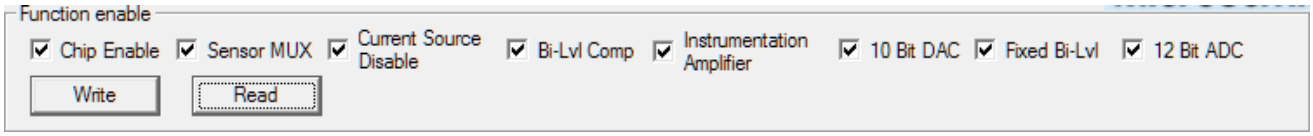
- In **Master reset**, click the On button. The current consumption should be about 60mA as the LX7730 because the LX7730 resets to operating mode, same as on power up



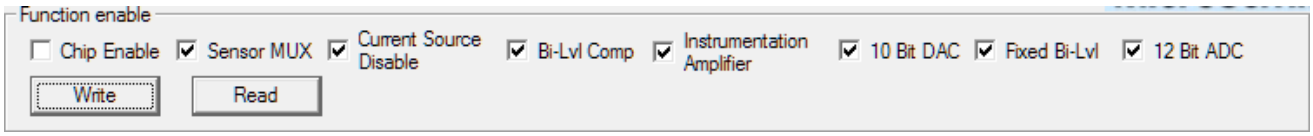
- In **Master reset**, click the Off button



- In **Function enable**, click Read. All functions should show checked due to the reset



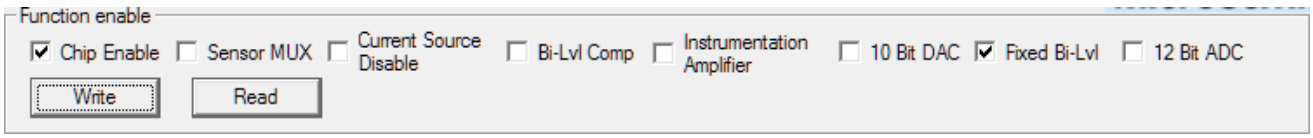
- Now uncheck **Chip Enable** under **Function enable**, and click Write. The current consumption should drop to a few mA as the LX7730 is now in low power mode



2.1.2 BLI/BLO Comparators

These 8 comparators have input pins and output pins, so the internal registers are only used to configure them.

- In **Function enable**, set only **Chip Enable** and **Fixed Bi-Lvl** checked, and click Write. The current consumption should be about 10mA as the LX7730 is only operating the 8 bi-level comparators



- Connect the DVM between the comparator output BLO1 test point TP67 and one of the GND or AGND test points. The DVM should read 0V (logic low), as all the BLI comparator inputs have weak internal pulldowns caused by normal leakage to GND (under 1.5µA) in the input protection circuits

- Connect a test lead between the comparator input BLI1 test point TP116 and the +5V test point TP1. The DVM should read about 3.3V (logic high), as the comparator input is higher than it's +2.5V trip threshold

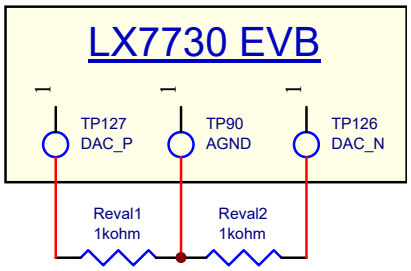
- Move the test lead from the +5V test point TP1 to one of the GND or AGND test points. The DVM should now read 0V (logic low), as the comparator input is lower than the +2.5V trip threshold

- Repeat the procedure for the remaining 7 comparators at input BLI2-8, outputs BLO2-8 if desired

2.1.3 10-Bit DAC Outputs DAC_P and DAC_N

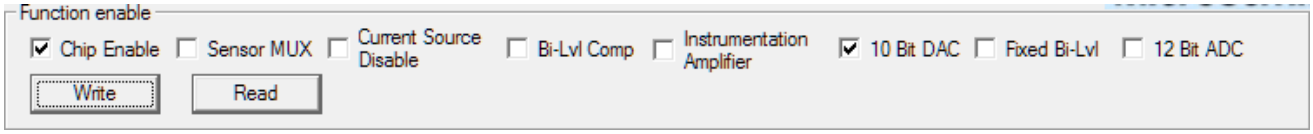
The 10-bit DAC is checked out by configuring it's outputs to be complementary current sources to the DAC_P and DAC_N pins. These currents are converted to voltages using two 1kΩ resistors, so that the outputs can be observed using the DVM. The complementary DAC outputs source 0-2mA and 2-0mA respectively, so the full scale output voltages with 1kΩ resistor output loads will be 0-2V and 2-0V respectively

- Connect a test lead between an AGND test point and one side of both 1kΩ resistors. Connect a test lead between the other end of one resistor to the DAC_P test point TP127. Connect a test lead between the other end of the other resistor to the DAC_N test point TP126. Both DAC outputs now have a load resistor to AGND



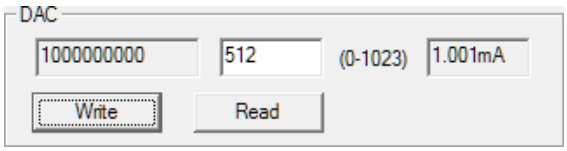
- Connect the DVM from the DAC_N test point TP126 and AGND. It should read 0V, because the 10-bit DAC was disabled in the setup for the previous test

- In **Function enable**, set only **Chip Enable** and **10 Bit DAC** checked, and click Write. The current consumption should be about 10mA as the LX7730 is only operating the 10-bit DAC



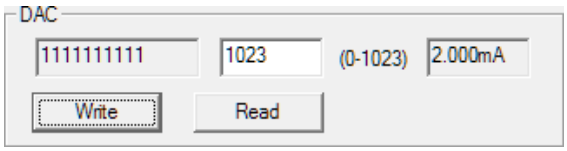
- The DVM on DAC_N should now read about 2V. Move the DVM to the DAC_P test point, which should read 0V. This represents the default DAC setting of 0

- Select **Page2** in the top left corner of the GUI. In **DAC**, type 512 into the white box, and click Write. This sets the DAC to half full scale



- Use the DVM to read the DAC_P and DAC_N outputs. They should both be about 1V, representing half full scale

- In **DAC**, type 1023 into the white box then click Write. This sets the DAC to full scale

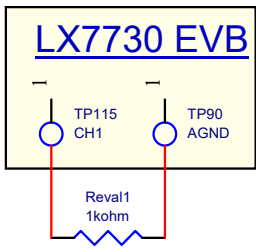


- Use the DVM to read the DAC_P and DAC_N outputs. DAC_P should be about 2V, and DAC_N at 0V, representing full scale
- Select **Page1** in the top left corner of the GUI
- Remove the test leads from the test points

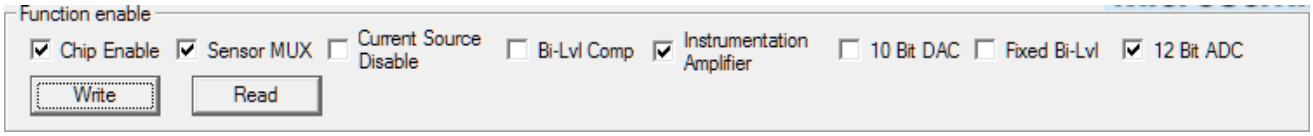
2.1.4 ADC AND SENSOR CURRENT SOURCE

The ADC is configurable to measure differential and single-ended inputs with a range of sensitivities, and can additionally force a programmable current into an external resistive sensor, such as a thermistor. In this section, we use one of the 1kΩ resistors as a dummy external resistive sensor, drive it from an internal current source.

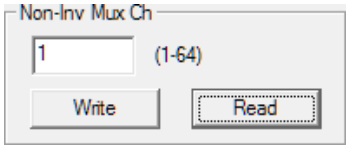
- Use two test leads to connect a 1kΩ resistor between the CH1 analog input TP15 and an AGND test point



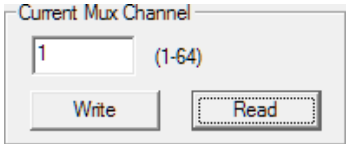
- Connect the DVM between the ADC_IN test point TP130 and AGND. This will be measuring the voltage at the end of the analog input signal chain and the input to the ADC itself
- In **Function enable**, check **Chip Enable**, **Sensor Mux**, **Instrumentation Amplifier**, and **12 Bit ADC,** and click Write. The current consumption should be about 63mA as the LX7730 is operating the entire ADC signal chain



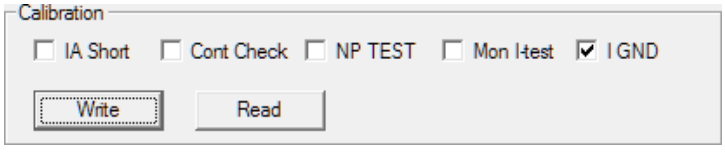
- Click Read under **Non-Inv Mux Ch** to check that CH1 is selected. This is the default setting of the inverting input to the internal instrumentation amplifier after reset



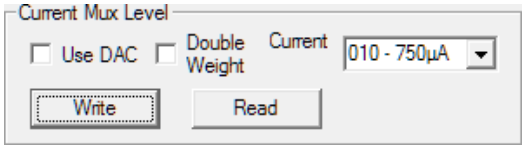
- Click Read under **Current Mux Ch** to check that CH1 is selected as the destination for the internal current source. This is the default setting after reset



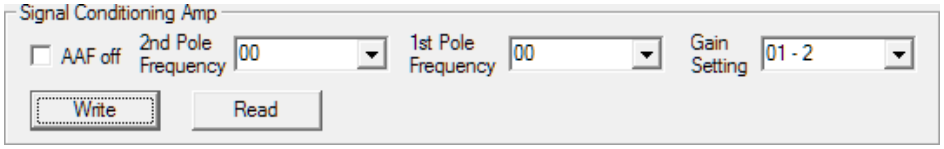
- Select **Page2** in the top left corner of the GUI. In **Calibration**, check **IGND**, and click Write. This sets the non-inverting input to the internal instrumentation amplifier to AGND internally



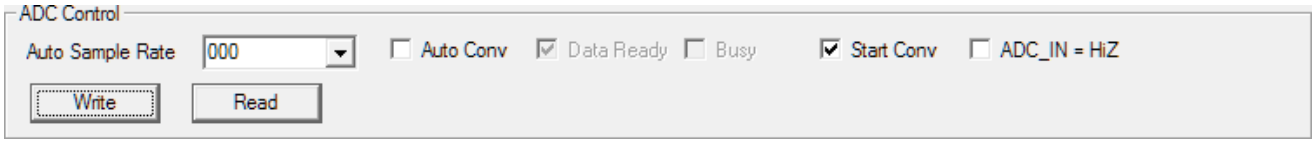
- Select **Page1** in the top left corner of the GUI
- In **Current Mux Level**, select **010 - 750µA** current, and click Write. This selects a current source of actually 727µA out of the CH1 pin from the LX7730. This will pass through the 1kΩ resistor that fitted earlier from CH1 to AGND, and the voltage at CH1 will be nominally 0.727V, plus or minus due to tolerances
- The DVM will now show a voltage of about 290mV, which is 727mV times the default input amplifier gain of 0.4



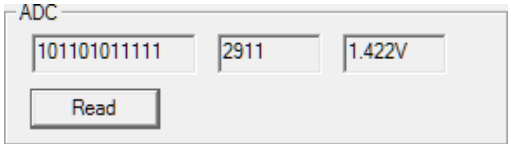
- In **Signal Conditioning Amp**, select **01 - 2** gain setting, and click Write. This selects a voltage gain of 2, so the 0.727V nominal at CH1 will become 1.454V at the ADC input, which has a full scale of 2V. The DVM will now show a voltage of about 1.454V



- Now we can take ADC measurements. In **ADC Control**, ensure that only **Start Conv** is checked, and click Write. This initiates a single ADC conversion



- In **ADC**, click Read to display the ADC conversion result

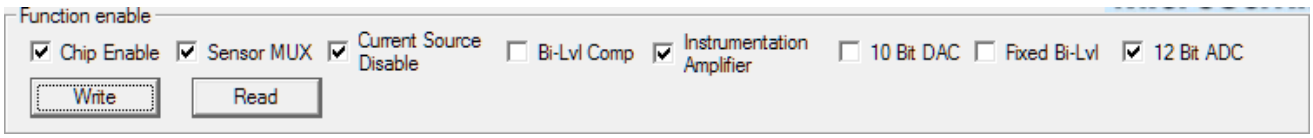


- Repeat clicking Write under **ADC Control** followed by Read under **ADC** to take more readings. Change the current source value in the **Current Mux Level** setting and see how the ADC readings change. If the **Current Mux Level** setting is changed to **100 - 1250µA**, then the input voltage at the ADC will be about 2.4V, as shown by the DVM. However, this exceeds the ADC's 2V full scale, so the ADC will simply return a value of full scale
- Remove the two test leads with the 1kΩ resistor from the test points, but leave the DVM in place for the next section

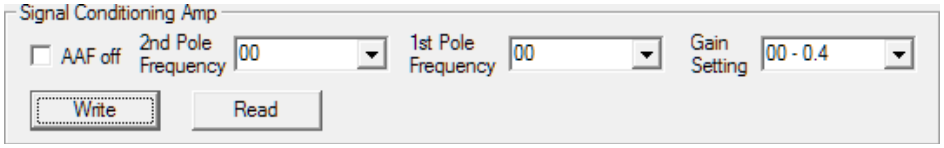
2.1.5 Using the ADC for Internal Diagnostics

The ADC multiplexor can be switched to monitor the reference and power supplies for diagnostics. In this section we configure the ADC to measure the VCC supply.

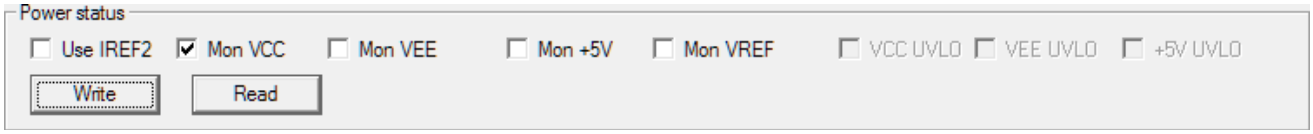
- In **Function enable**, check **Chip Enable**, **Sensor Mux**, **Current Source Disable**, **Instrumentation Amplifier**, and **12 Bit ADC,** and click Write



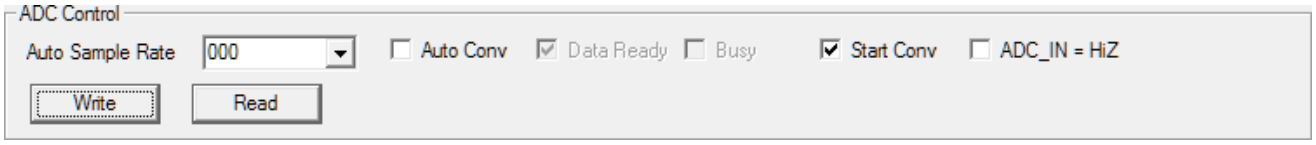
- In **Signal Conditioning Amp**, select **00 - 0.4** gain setting, and click Write. This selects a voltage gain of 0.4



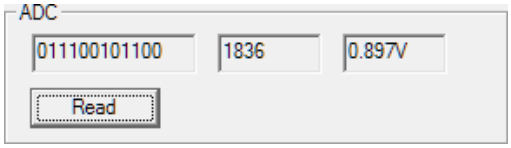
- In **Power status**, check **Mon Vcc**, ensure the other boxes are unchecked, and click Write. The input multiplexor now selects the VCC supply divided by 6, which will be 2.25V when VCC is set to 13.5V. As we have set the amplifier to a gain of 0.4V, the expected ADC input voltage is therefore (13.5V / 6 * 0.4) = 900mV



- Now we can take an ADC measurement. In **ADC Control**, ensure that only **Start Conv** is checked, and click Write. This initiates a single ADC conversion



- In **ADC**, click Read to display the ADC conversion result



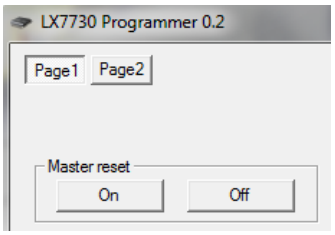
- When finished testing, uncheck **Chip Enable** under **Function enable**, and click Write. The current consumption should drop to a few mA as the LX7730 is now in low power mode

3 Using the Software GUI

To execute a command in the GUI, select the desired check boxes or other information, and then click the associated Write button to write the data to the LX7730's register(s). Optionally click the Read button to read back and verify that the command was received.

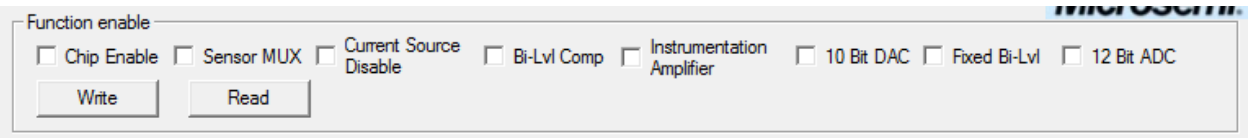
3.1 Master Reset

The Master reset button performs a master reset which returns all internal registers to the power on (default) state.



3.2 Function Enable

The Function enable panel powers down selected functions that are not needed; the default state is everything enabled as indicated. This feature allows user the flexibility to conserve power while keeping needed functions alive.



At this point you may wish to verify that the various LX7730 internal supplies are up and working. The various voltages on the LX7730 Evaluation Board are shown in Table 1 on page 9.

Name	Test Point	Measured Voltage
VCC	TP39	External analog supply voltage, in the range 11.4V to 16V
m2v	TP13	-2V, internally regulated by the LX7730
VEE	TP25	Switch SW1 is in the up position, setting $\overline{\text{EXT\_VEE}}$ = 0: User supplied external VEE supply in the range -10V to -16V applied to the blue VEE 4mm socket Switch SW1 is in the down position, setting $\overline{\text{EXT\_VEE}}$ = 1: LX7730's internal charge pump generates VEE at around -(VCC - 2)V
VDD	TP20	+3.3V (supplied by the USB cable)
CLK	TP24	External 500kHz, 0 to 3.3V square wave clock input
5V	TP1	+5V, internally regulated by the LX7730
VREF	TP128	Switch SW2 is in the up position, setting $\overline{\text{EXT\_VREF}}$ = 0: User supplied external VREF supply in the range 0V to -5.5V applied to the yellow VREF 4mm socket Switch SW2 is in the down position, setting $\overline{\text{EXT\_VREF}}$ = 1: LX7730's internal 5V VREF is used

Table 1. LX7730 Evaluation Board Supply Voltages

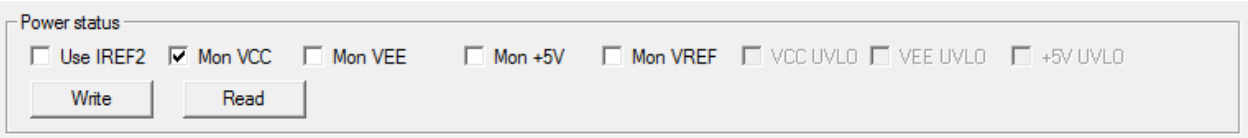
The Function Enable Register features are shown in Table 2 below:

Name	Default	Description
Chip Enable	1	If de-asserted everything but the active power supplies and digital interface to the FPGA is turned off but the internal register contents are preserved; this is a low power sleep mode. CH# and BLI# and DAC pins are cold spared. If de-asserted, functions corresponding to bits 0 thru 6 are disabled
Sensor MUX	1	If de-asserted, all CH switching and routing (Analog or Bi-Level) is turned off. CH# pins are cold spared
Current Source Disable	1	If asserted, the multiplexed current source directed to a CH# pin is not used and powered down. If de-asserted, the multiplexed current source is enabled and directed to the CH# selected in the Analog MUX section
Bi-level comp	1	If de-asserted, power is removed from the bi-level comparators but doing so does not affect the functionality of the Analog Multiplexer and ADC
Analog Amplifiers	1	If de-asserted, the instrumentation amplifier is powered down. The ADC and Bi-level comparators are not affected; however the ADC must be driven by an external signal using ADC_IN pin (with Filter Off bit asserted or ADC=Hi Z asserted)
10 Bit DAC	1	If de-asserted, the 10 bit DAC is not used and powered down. DAC outputs are cold spared
Fixed Bi-Level	1	If de-asserted, the Fixed Bi-level converters are not used and powered down. BLI# inputs are cold spared
12 Bit ADC	1	If de-asserted, the 12 bit ADC is not used and powered down

Table 2. LX7730 Function Enable Register

3.3 Power Status

The power supply pins for the LX7730 can be monitored by selecting special calibration registers: MON VCC, MON VEE, MON +5V, MON VREF. The voltages are divided down by a factor of 6 for the VCC & VEE rails and a factor of 2 for the 5V and VREF pins and routes the selected pin voltage to the non-inverting terminal of the IA (instrumentation amplifier). It overrides the setting of the Analog MUX Inverting MUX Channel and applies GND to the inverting terminal of the Instrumentation Amplifier for the positive voltages and GND to the non-inverting input of the IA for Mon VEE.



For example if Mon VCC is selected as shown above and the Signal Conditioning Amp Gain Setting is set to a gain of 0.4 and the ADC Controls Auto Conv box is checked then when reading the ADC a measurement of about 1V should be indicated (15V divided by a gain of 6 (internal divider), times 0.4 (gain setting).

The LX7730 provides a redundant precision reference current IREF2 which can be selected should IREF1 (TP95) fail. The GUI allows selection of IREF2 internal resistor by checking the box in the Power Status window.

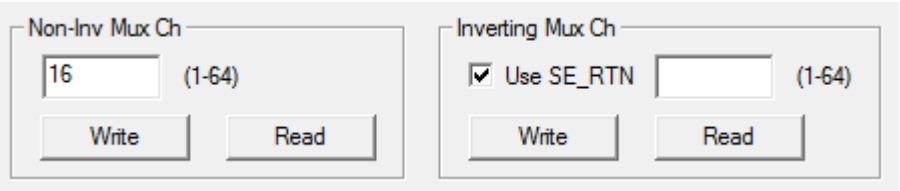
The VCC UVLO, VEE UVLO and +5V UVLO flags will be asserted when VCC, VEE, or +5V respectively are below their corresponding UVLO thresholds. To find the UVLO status for any of these supplies select the Read button, and look for the corresponding status box check mark. They are greyed-out since they are output only and cannot be selected.

3.4 Analog Mux

The analog multiplexer (AMUX) consists of 64 inputs. The Bi-level MUX and the AMUX are not independent; the En BL Sw Pos (found in the Bi-level Bank Switch Position section page 9) must be de-selected in order to use the AMUX. For a single ended input measurement the common SE_RTN reference pin can be selected checking the box Use SE_RTN.

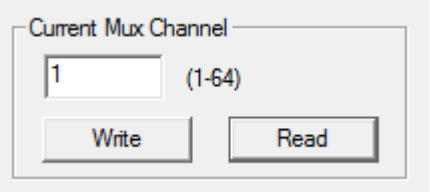
When selecting SE_RTN then TP3 SE_RTN pin is used as a common return for single ended sensor inputs.

When using differential sensor inputs, there are constraints since the AMUX is physically divided into eight banks of eight inputs. Only one CH#, from one input bank can be selected at a time which means that differential measurements must consist of two CH#s from two different input banks. For example CH1 can be connected with any other channel number except those in Bank 0 (i.e. CH9, 17, 25, 33, 41, 49 and 57). See the Sensor Multiplexer Block Diagram (Figure 4 on page 11).

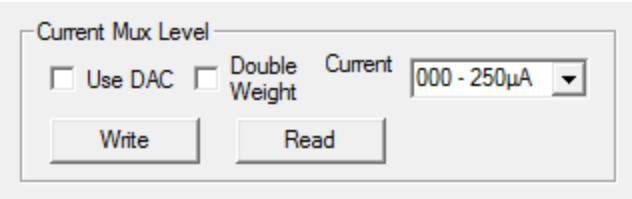


3.5 Current De-Mux

The current de-mux routes a programmable current to whichever of the 64 channel inputs is selected. The default channel in CH1, the default current is 250µA. There are several modes of operation depending on the current amplitude required.



There are eight selectable levels range from 250µA to 2mA using the drop down box. When the Double_Weight box is checked the selected value is doubled for a range from 500µA to 4mA. If the Use DAC box is selected, the 10bit DAC is used to set the de-mux current instead of the programmable current source; each LSB has a weight of 10µA. A maximum of 300µA is suggested (code 31) when operating in this mode. The current de-mux can be shut off selecting the Current Source Disable box in Function Enable. The current De-MUX defaults to the off state at power up.



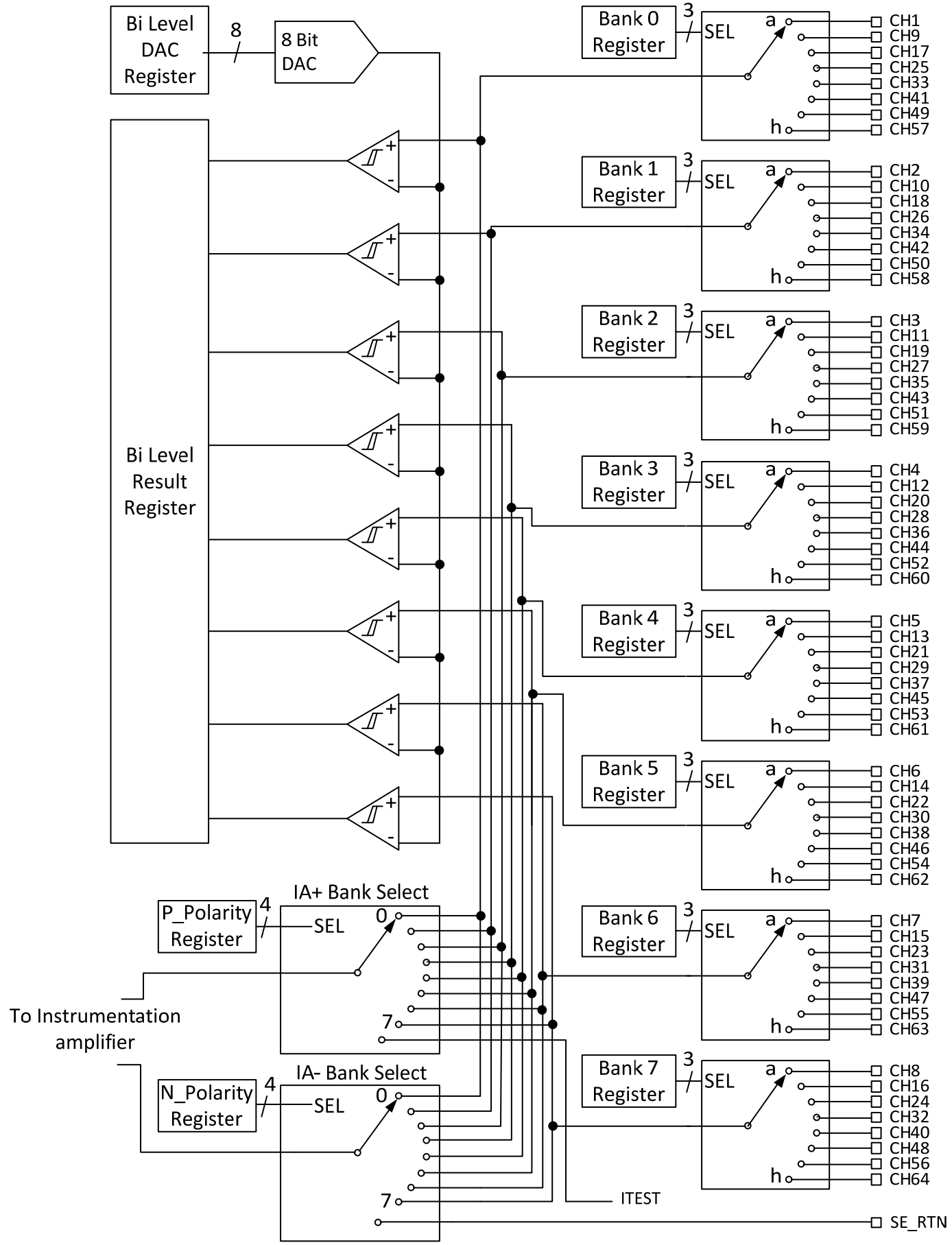
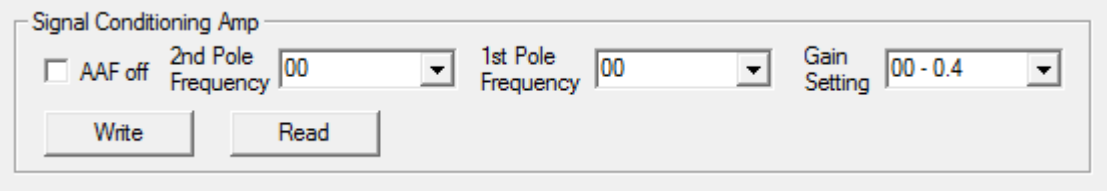


Figure 4. Sensor Multiplexer Block Diagram

3.6 Signal Conditioning Amp

The instrumentation amplifier, anti-aliasing filter, and ADC range scaling reside between the output of the analog multiplexer and the input to the ADC. The output of the entire gain and filter stage is accessible at the pin ADC_IN (TP130). If the AAF off box is selected the AAF filter is off and the ADC can be driven from ADC_IN.

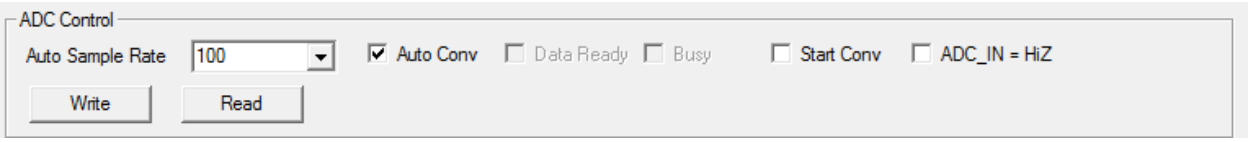


The AAF poles are set to nominally 00, 01, and 10 for 400, 2k or 10k in Hertz, respectively. Either one or both poles can be selected. The ADC sensitivity is set by adjusting the amplifier gain. The gain can be set to 10, 2 or 0.4.

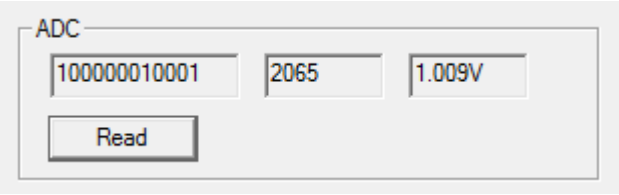
To allow operating room for the ADC (which operates from a 5V rail) the ADC_IN range is 0 to 2V. If an external input is to be sampled by the ADC, the internal circuitry driving the ADC_IN pin can be made high impedance by setting the Hi-Z bit in the ADC programming register.

3.7 Analog To Digital Converter

The ADC uses a successive approximation register (SAR) design. The CLK input sequences the ADC logic. The Auto Sample Rate is set to multiples of the Sample Period (tSAMP). This 3 bit N binary value sets the ADC auto sample rate = tSAMP x 2N.. The ADC can be set to convert continuously (Auto Conv) or to convert on request using (Start Conv). Whenever a conversion is in process the Busy status bit is asserted. When the conversion is complete the Data Ready bit is set. The ADC value registers are updated when the Data Ready bit is asserted, but will not change during the process of a data read which starts by reading the upper byte and ends by reading the lower byte. If you select the Read button the Data Ready or Busy will display.

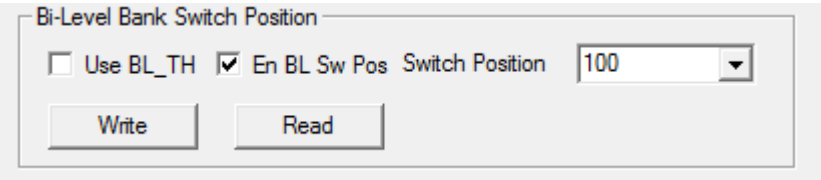


The ADC window will display the result of the latest conversion when the Read button is selected.

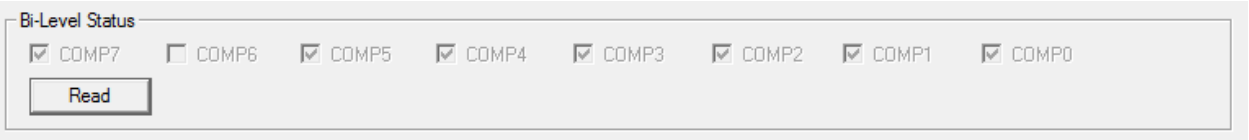


3.8 Bi-Level Inputs

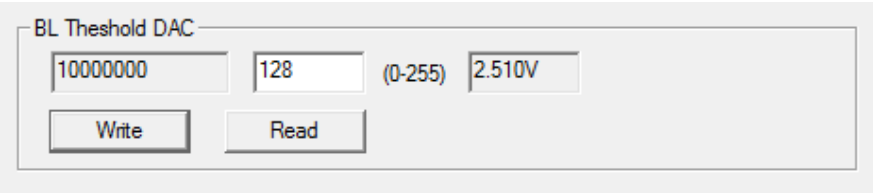
There are two sets of 8 bi-level inputs on the LX7730, first the 64 sensor inputs can be used as bi-level detection inputs. The Bi-level MUX and the AMUX are not independent; the En BL Sw Pos must be selected to use the Bi-Level MUX. The bi-level detection comparators monitor one position, simultaneously, from each of the input banks; the position is register selectable (bank 0 to 7, 000 to 111). See the Sensor Multiplexer Block Diagram (Figure 4 on page 11). For example, code 000 will connect CH1 to CH8 to the 8 bi-level comparators, and code 001 to CH9 to CH16 respectively. The comparators are sampled during the clock cycle that the Bi-Level Status is read, and the result placed in the Bi-Level Result Register shown in the GUI as Bi-Level Status.



The outputs of the group of 8 comparators available in this register are continuously updated and can be polled to monitor the status. The GUI allows you to see the status of the Bi-Level Result Register in the Bi-Level Status Window using the Read button. These functions are greyed-out because they cannot be selected but only show a change by the check mark appearing or disappearing.



The selected eight bi-level inputs are compared to a common adjustable threshold that is developed using an 8 bit binary DAC.



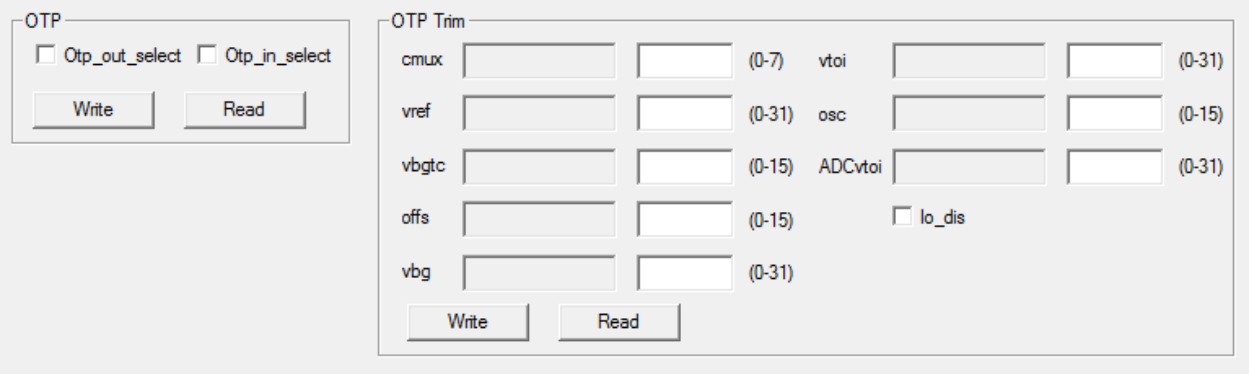
In addition to these register based Bi-level comparators utilizing the Sensor inputs, the IC and the evaluation board includes 8 external Bi-level input pins (TP116 to TP123) that can be compared to either an internal 2.5V reference level or an external threshold voltage (BL_TH TP125) selected by checking the box Use BL_TH in the GUI. BLO1 to BLO8 are the comparator outputs of these 8 inputs (TP67 to TP83) and are referenced to VDD logic levels.

3.9 Current DAC

The outputs of the DAC should be terminated in resistors 1.5kΩ or less to ensure the DAC stays within its compliance range. A parallel 1nF or greater capacitor can also be used to minimize bit change glitches. The DAC has complementary outputs that are accomplished by steering the current between the two outputs based on the DAC setting. At zero LSBs, the DAC_N is full scale and DAC_P is off. The Current DAC outputs are available at DAC_N (TP126) and DAC_P (TP127).

3.10 Power & Reference Adjust (OTP)

When Otp_out_select is checked and written to LX7730 the setting in the OTP trim boxes will override the default settings in the trimming register. These settings are temporary and must be re-written with a power cycle. If Otp_out_select is unchecked and Write pressed, the contents of the trim registers will revert back to the default values. If Otp_in_select is checked and written the default OTP bits are read into the display upon Read.

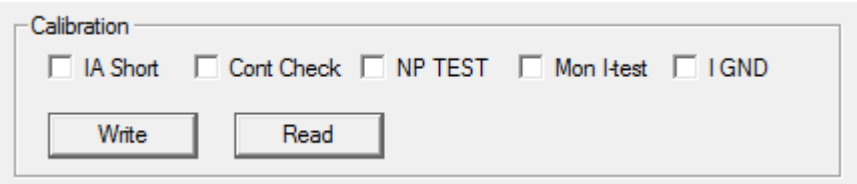


3.11 Calibration

The calibration buttons write to register 16 and are used to perform calibration of the amplifier offset and testing of the multiplexer switches and programmable current source multiplexer. For more information, see the LX7730 datasheet that includes diagrams depicting the following modes.

Table 3. Calibration Modes

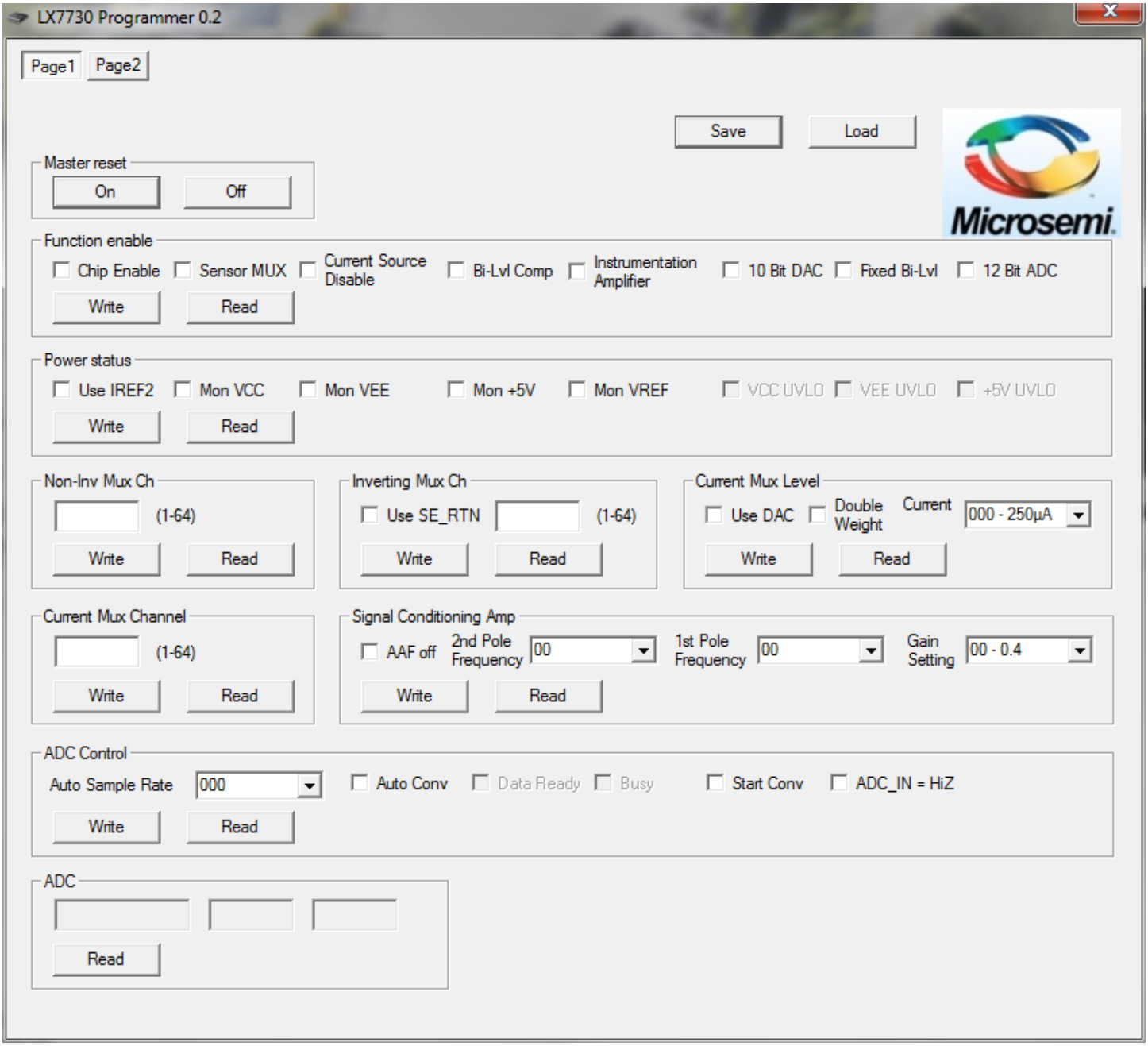
Function Selected	Instrumentation Amplifier Modification	Function Behavior	Register Over-Ridden
I GND	Non-inverting input connected to multiplexer as normal Inverting input tied to AGND instead of multiplexer	This option connects the instrumentation amplifier's inverting input to GND internally. This allows the acquisition of a single-ended signal using only one CH input. The inverting input can alternatively be connected to an external GND via the SE_RTN pin using the Inverting Mux Channel Select register	Inverting Mux Channel Select register 4
NP Cont Check	Non-inverting input tied to VREF/2 instead of multiplexer Inverting input connected to the multiplexer current source (set as normal) as well as the multiplexer	Use this setting to perform a continuity check of the instrumentation amplifier's inverting input multiplexer. An open multiplexer path (including input source) is detected by the current source pulling up the inverting input higher than VREF/2 causing the amplifier output to go low. If an external sensor is properly attached, the voltage read by the ADC is the difference of VREF/2 and the product of the current source and the impedance of the sensor plus the impedance of the two multiplexer switches encountered in the current path.	Non-Inverting Mux Channel Select register 3 Current Mux Channel Select register 6
Cont Check	Non-inverting input connected to the multiplexer current source (set as normal) as well as the multiplexer Inverting input is connected to the multiplexer as normal	Use this setting to perform a continuity check of the instrumentation amplifier's non-inverting input multiplexer. An open multiplexer path (including input source) is detected by the current source pulling up the non-inverting input causing the amplifier output to go high. A working multiplexer path allows the total resistance of the two multiplexers in series with the input source to be measured as a voltage drop due to the current source. If the inverting input is selected as the same channel input as the non-inverting input, then the resistance of the non-inverting input multiplexer can be measured	Current Mux Channel Select register 6
IA Short	Non-inverting input connected to multiplexer as normal Inverting input is tied to the non-inverting input	This option allows the instrumentation amplifier's offset and common mode errors to be measured	Inverting Mux Channel Select register 4



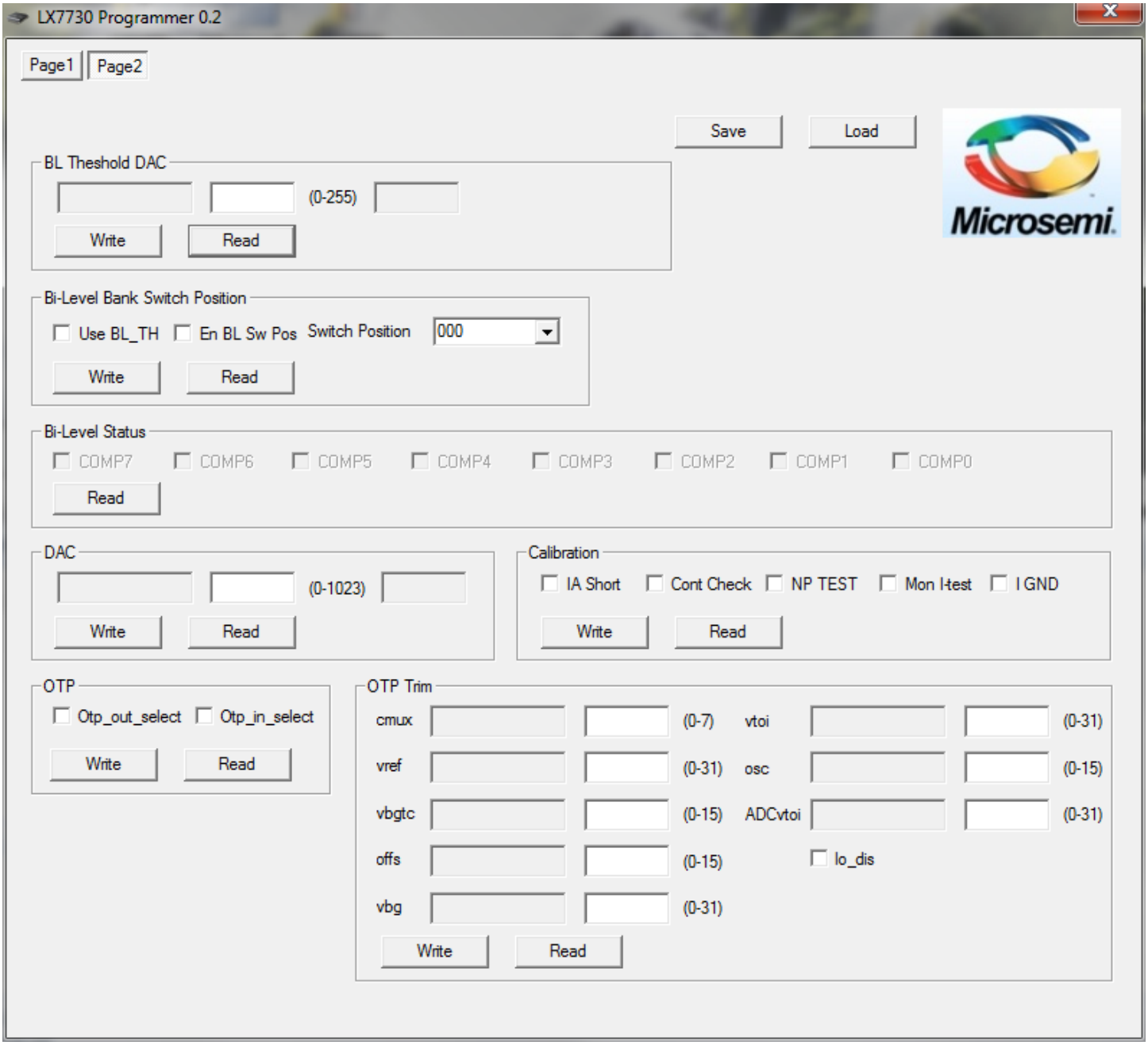
3.12 Save / Load

The SAVE / LOAD function allows the current settings of the GUI to be save to a txt file on your computer. You can restore a previous configuration by loading back this file and using the WRITE commands to restore each setting.

4 Programmer Page 1



5 Programmer Page 2



6 Other Features Of The Evaluation Board

6.1 +5V TP1

This pin is the low voltage power rail. It is generated internally using a linear regulator connected to the VCC rail. It is bypassed by C1 1µF and C2 100nF capacitors.

6.2 VREF TP126

This pin is a +5V reference voltage that can be used to provide a voltage reference to sensors for precision measurements. It is bypassed by capacitors C14 1µF and C15 100nF to AGND. The internal reference can be disabled and an external reference connected to this pin; the internal voltage reference must be disabled in this case using the /EXT_REF programming pin SW2.

6.3 PARALLEL INTERFACE

J7 pins 11 to 20 allow connection to the parallel interface these are logic I/O pins providing data bits, D0 (LSB) (pin 14) through D7 (pin 21. There is a weak pull-down on these pins.

J7 pin 19 provides the parity bit for the parallel data communication. Even parity is used for the combination of address and data bits and is used in both directions. There is a weak pull-down on this pin.

J7 pin 20 is the acknowledge bit In the event of a parity error encountered in a serial or parallel data transfer, the /ACK pin is de-asserted (pulled high). It remains high until the start of the next data transfer logic sequence.

6.4 RESET

J7 pin 21 is the system reset logic input. This pin provides an external forced reset to the default state of all registers and flip-flops within the LX7730. A pulse width of greater than 500ns is required; there is a weak pull-down on this pin.

7 Bill of Materials

Designator	Quantity	Description	Manufacturer & Order Code
C1, C4, C7, C8, C9, C10, C14	7	Capacitor 1µF 50V X7R 1206	NIC NMC1206X7R105K50TRPLPF
C2, C5, C6, C12, C15, C17	6	Capacitor 0.1µF 50V X7R 1206	AVX 12065C104KAT2A
C3	1	Capacitor 0.47µF 50V X7R 1206	TDK CGA5L2X7R1H474K160AA
C11	1	Capacitor 4.7µF 50V X7R 1206	Samsung CL31B475KBHVPNE
C16	1	Capacitor 1000pF 50V X7R 1206	Kemet C1206C102K5RACTU
J2	1	Test socket Red	Deltron 571-0500
J5, J10	2	Test socket Black	Deltron 571-0100
J3	1	Test Socket Blue	Deltron 571-0200
J4	1	Test Socket Green	Deltron 571-0400
J9	1	Test Socket Yellow	Deltron 571-0700
J6	1	RF connector R/A PCB jack	Amphenol 31-5637
J7 (rev. B)	1	22 pin 0.1" header	
J7 (rev. C)	1	23 pin 0.1" header	
R1, R2, R3, R4, R5, R6, R7, R8, R9	9	Resistor 49.9Ω 1% 1206	Vishay CRCW120649R9FKEB
R11	1	Resistor 20kΩ 1% 1206	Panasonic ERJ-8ENF2002V
R10	1	Resistor 7.87kΩ 0.1% 1206	Panasonic ERA-8AEB7871V
R12	1	Resistor 158Ω 0.1% 1206	Panasonic ERA-8AEB1580V
SW1, SW2, SW3, SW4	1	DIP Switch 2PST	Grayhill 78F01ST
TP85, TP86, TP87, TP88, TP90, TP92, TP96, TP97, TP99, TP101	10	PC Test Point Black	Keystone 5011
TP9, TP5, TP22, TP18, TP15, TP21, TP17, TP14, TP12, TP8, TP7, TP2, TP23, TP19, TP16, TP11, TP10, TP6, TP4, TP28, TP34, TP29, TP26, TP27, TP36, TP37, TP35, TP42, TP40, TP38, TP50, TP41, TP57, TP58, TP56, TP60, TP61, TP59, TP65, TP62, TP63, TP66, TP68, TP64, TP76, TP69, TP71, TP80, TP81, TP77, TP104, TP107, TP110, TP113, TP102, TP105, TP108, TP111, TP114, TP103, TP106, TP109, TP112, TP115	64	PC Test Point White	Keystone 5012
TP13, TP20, TP25, TP39, TP128, TP1	6	PC Test Point Red	Keystone 5010
TP3, TP24, TP32, TP31, TP30, TP44, TP33, TP52, TP43, TP51, TP54, TP55, TP49, TP46, TP47, TP48, TP45, TP53, TP73, TP74, TP75, TP70, TP72, TP67, TP82, TP78, TP79, TP83, TP84, TP98, TP95, TP124, TP127, TP126, TP118, TP121, TP123, TP130, TP117, TP120, TP122, TP125, TP116, TP119	44	PC Test Point Yellow	Keystone 5014
U1	1	Clamshell ZIF Socket	Enplas FPQ-228-0.635-01

8 Schematics

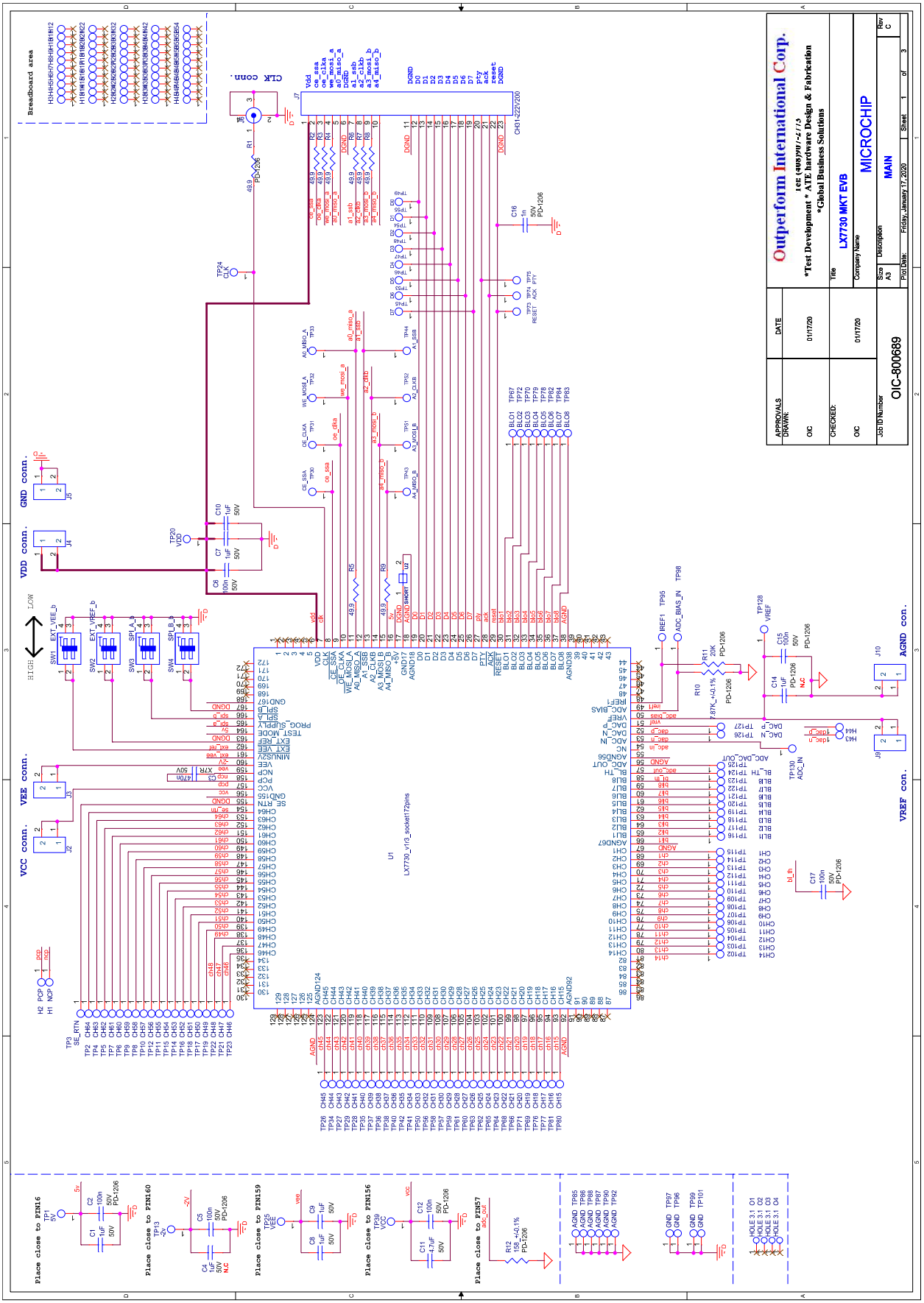


Figure 5. Rev. C Schematic

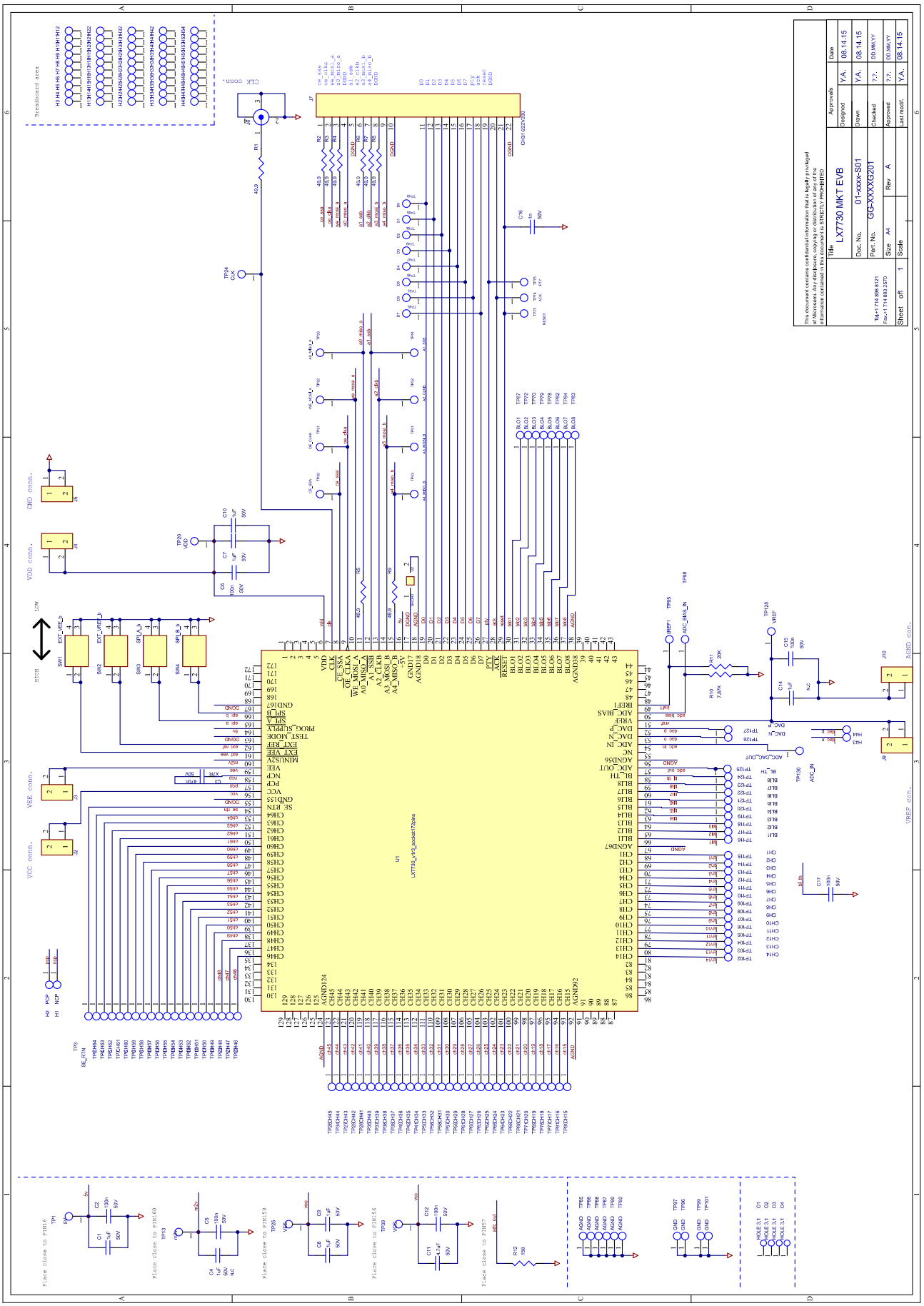


Figure 6. Rev. B Schematic

9 PCB Layout

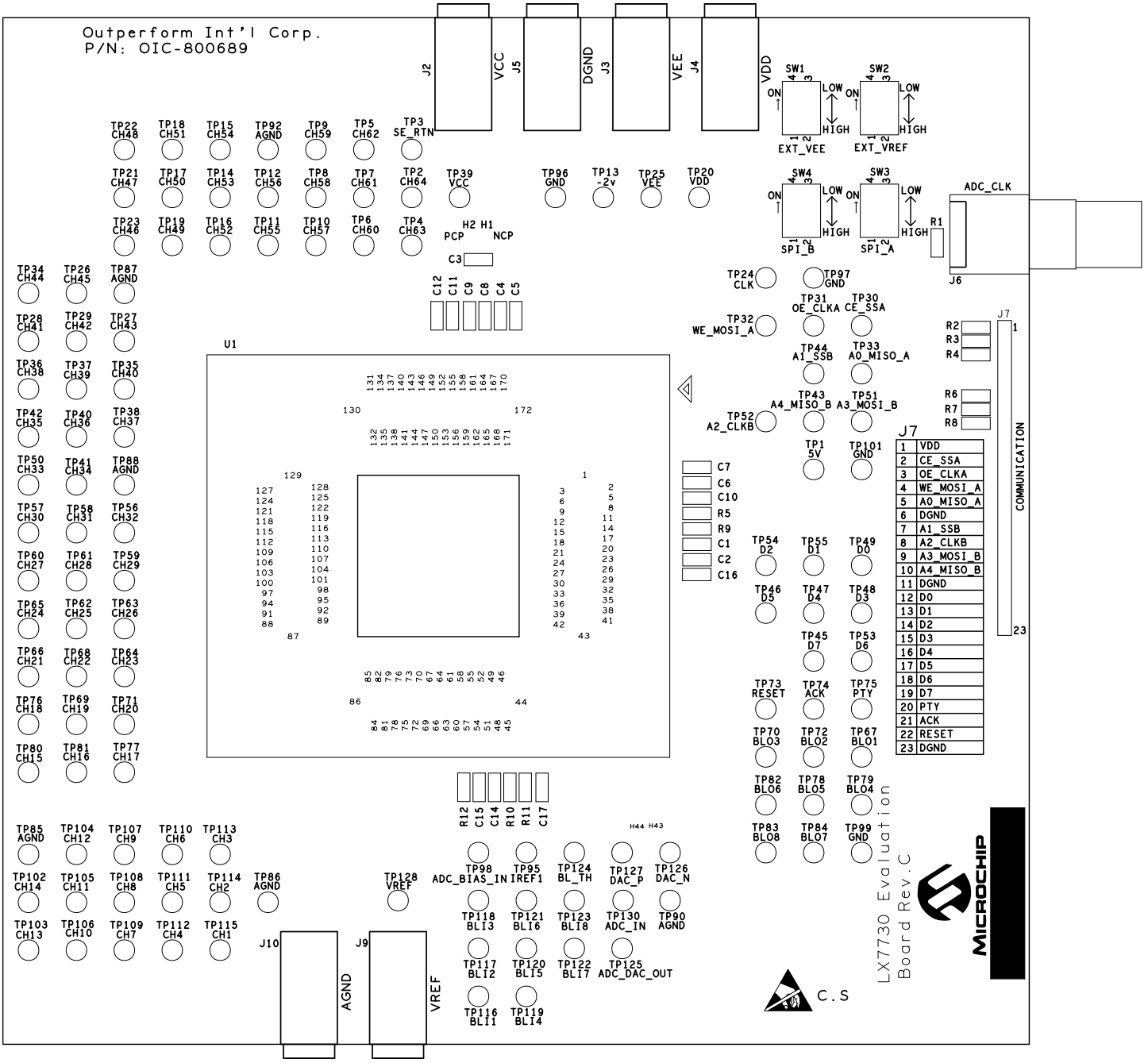


Figure 7. Rev. C Top Legends

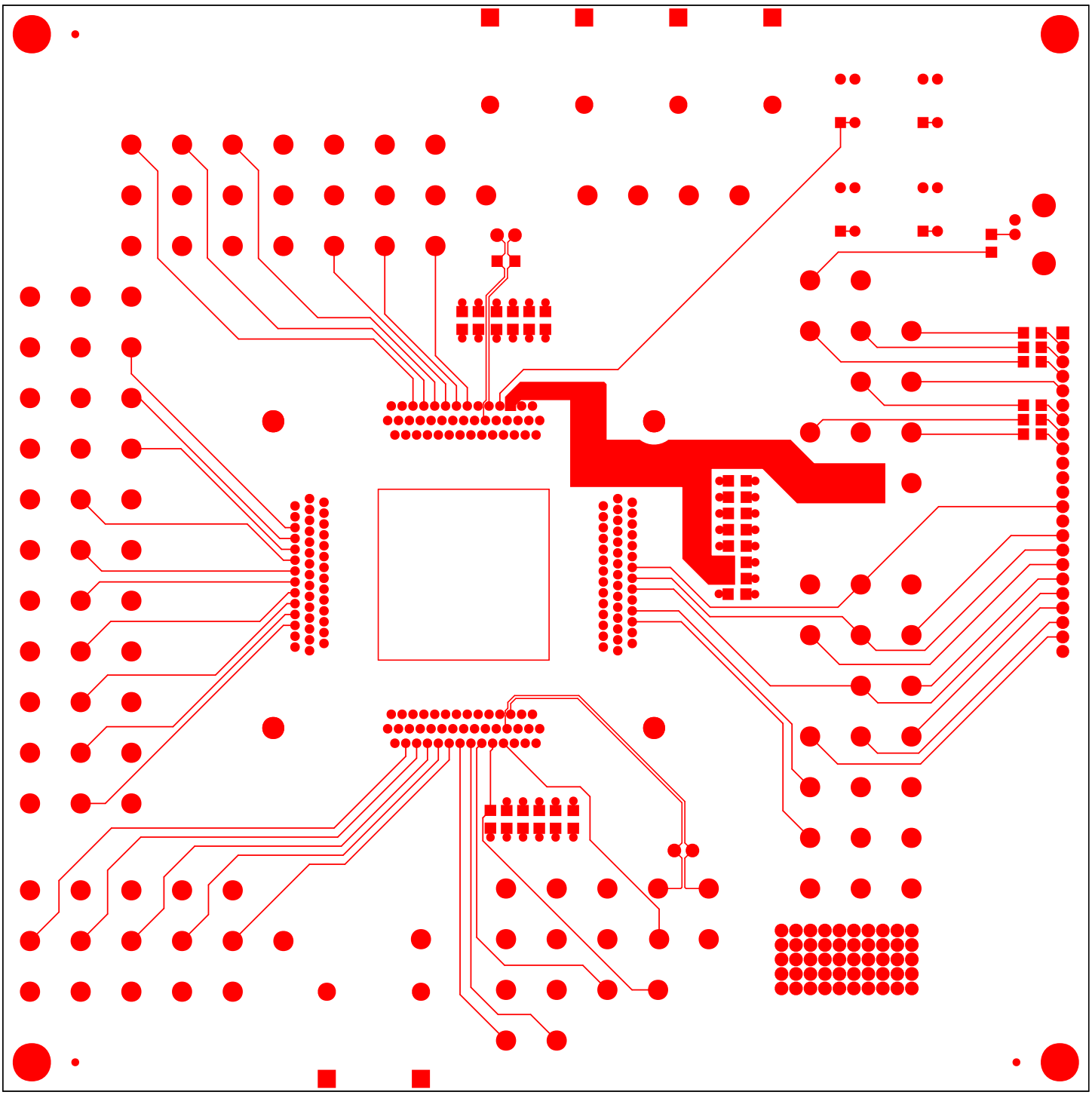


Figure 8. Rev. C Top Layer

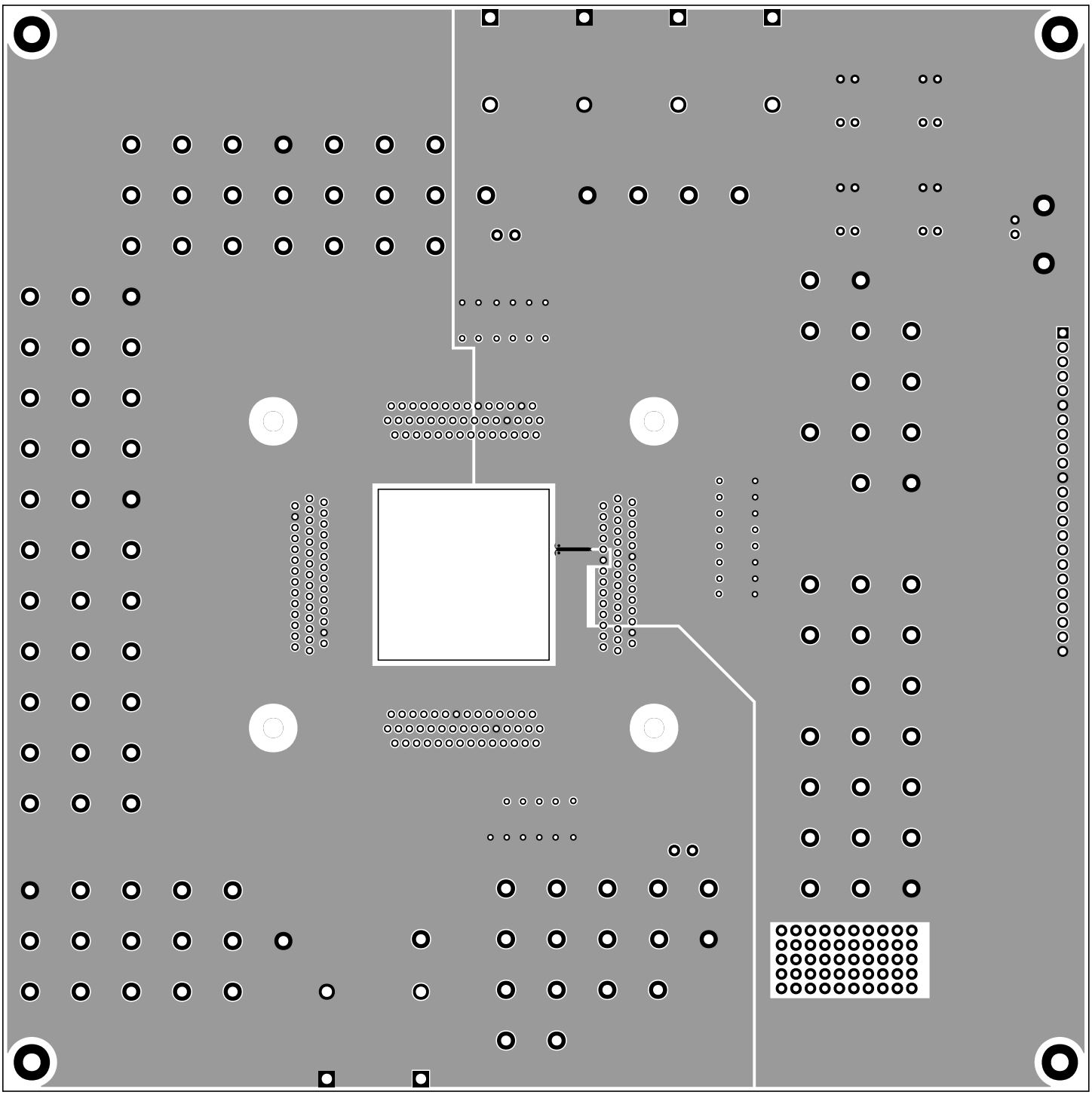


Figure 9. Rev. C Layer 2 - GND

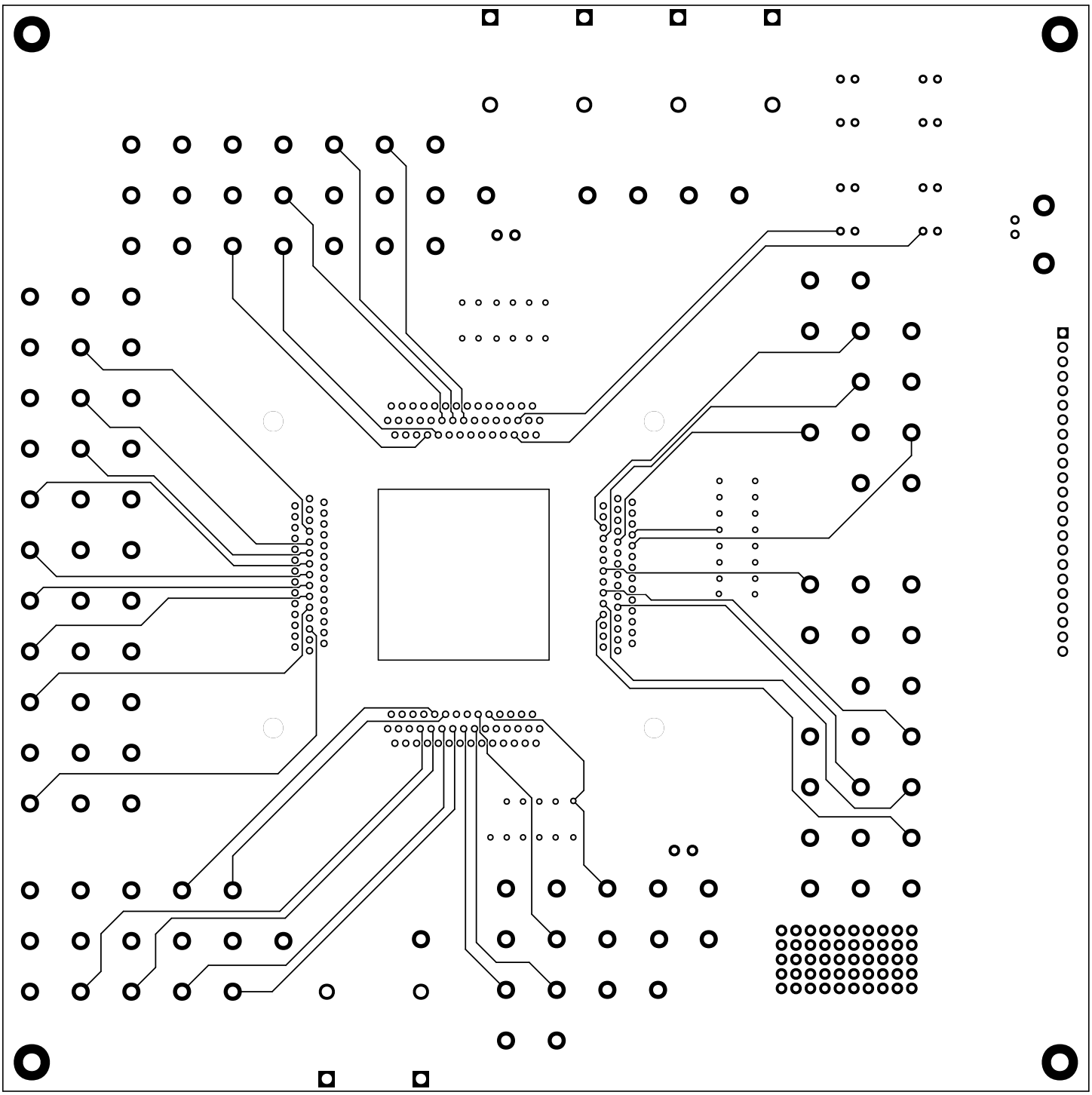


Figure 10. Rev. C Layer 3 - Signal 1

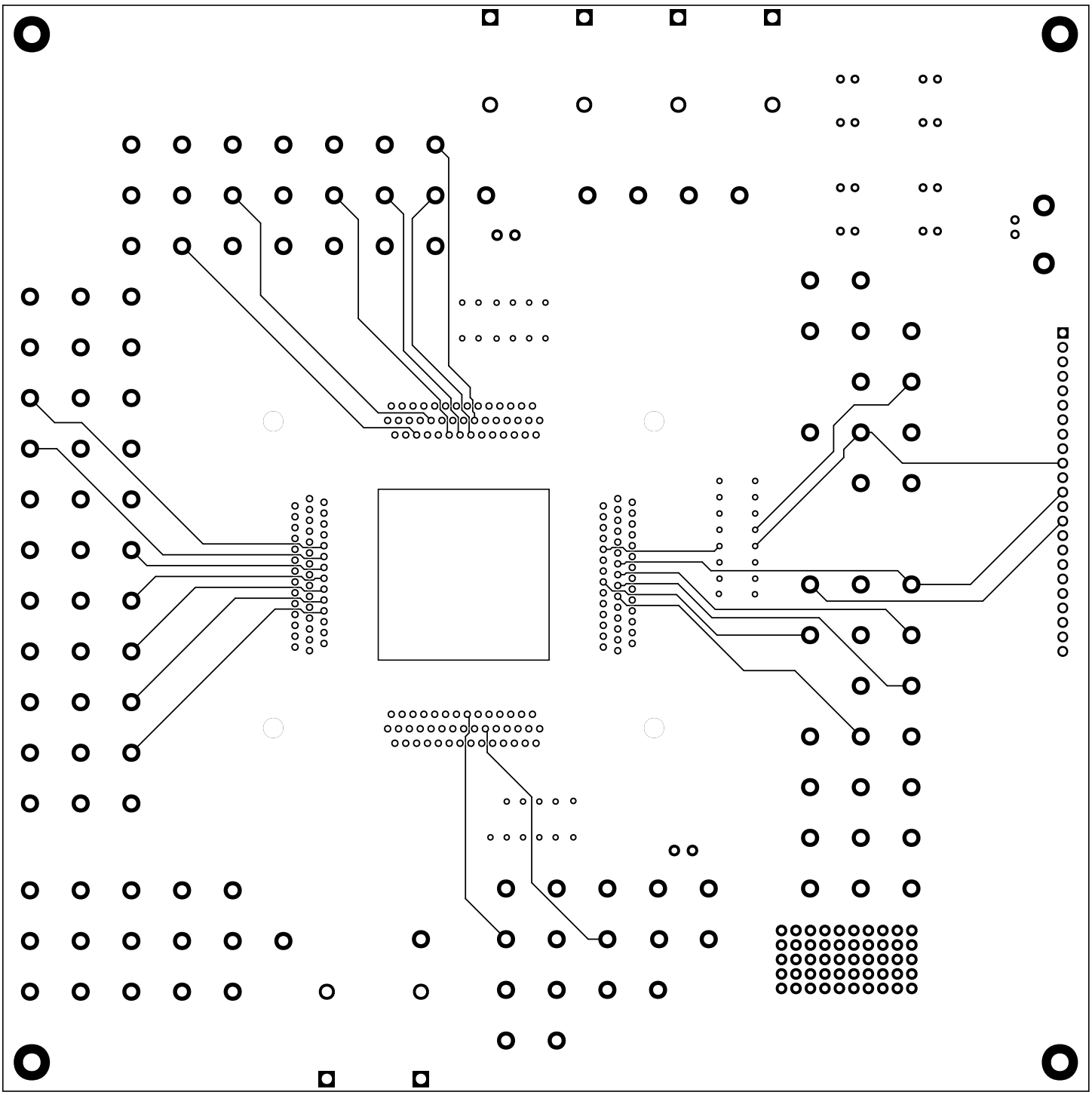


Figure 11. Rev. C Layer 4 - Signal 2

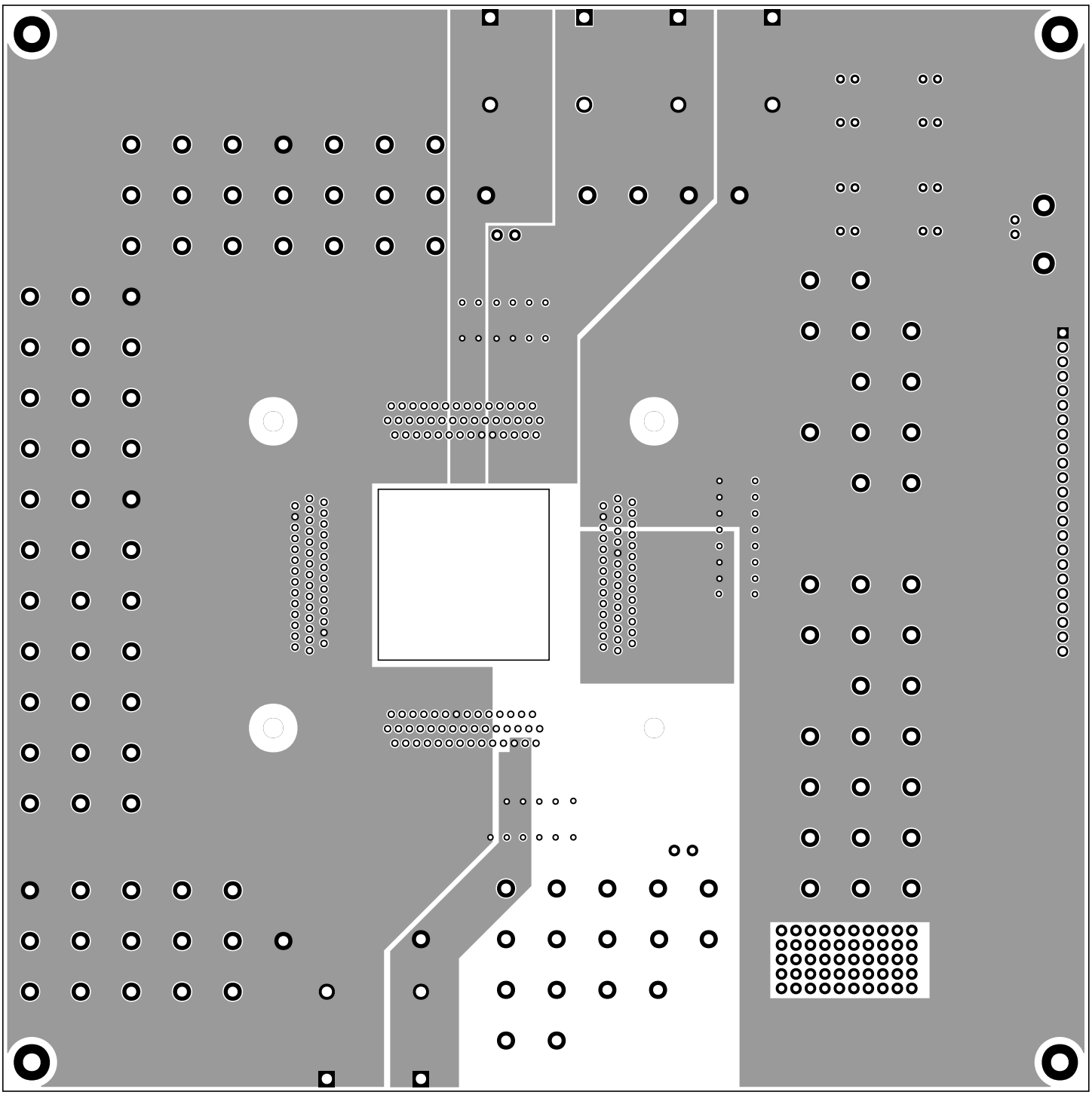


Figure 12. Rev. C Layer 5 - Power

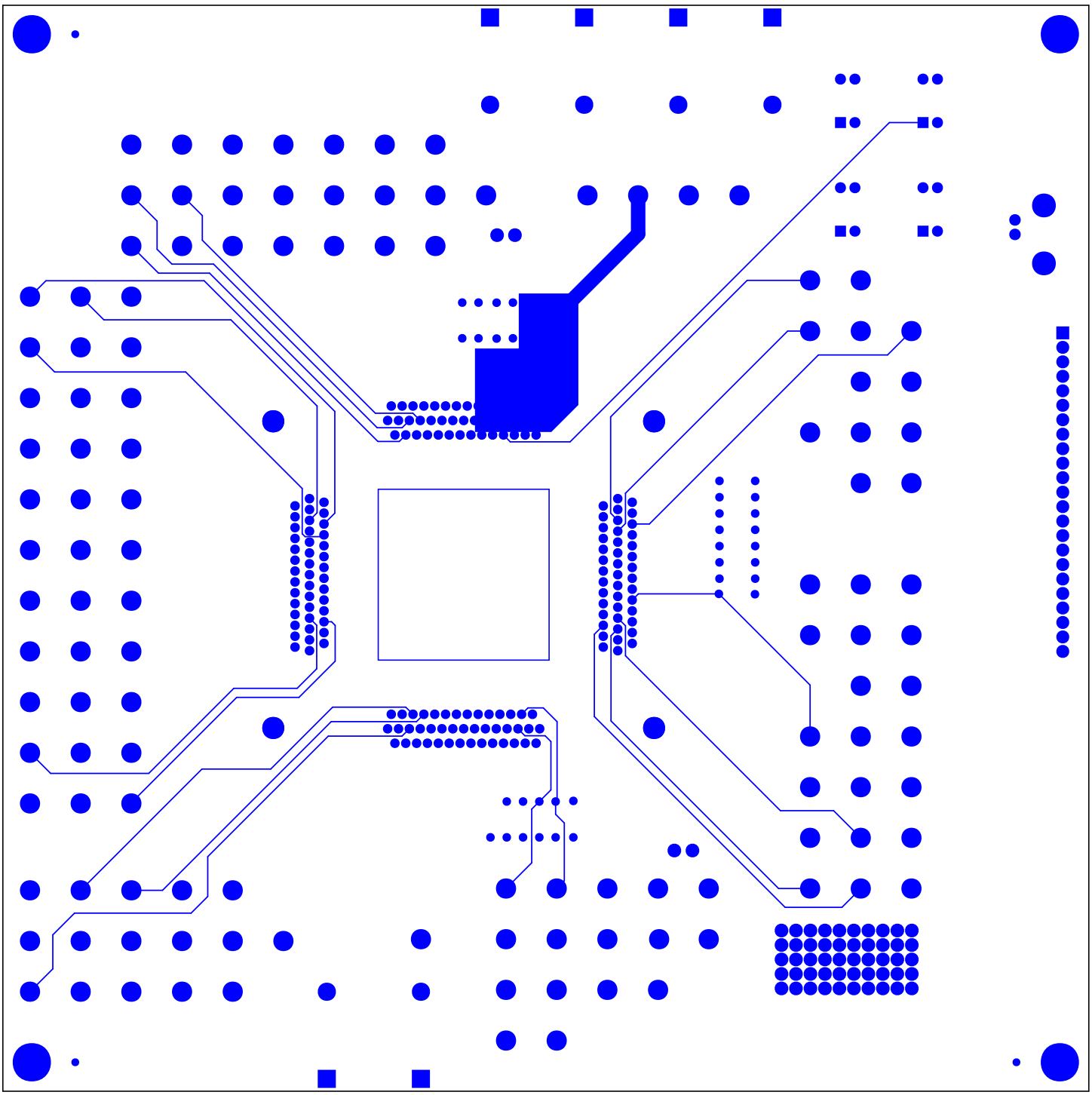


Figure 13. Rev. C Layer 6 - Bottom

10 Revision History

10.1 Revision 0.6 - June 2016

First release.

10.2 Revision 1 - September 2020

Branding moved from Microsemi to Microchip, and some terminology changed.
Schematic quality improved.
BOM added.

10.3 Revision 1.1 - March 2022

Added the inclusion of a LX7730MFQ-ES sample to kit content, updated LX7730 homepage weblink on page 1.

10.4 Revision 1.2 - March 2022

Added support for the rev. C version of the evaluation board.

10.5 Revision 2 - May 2023

Major revision merging the Get-Started Guide into this document, re-writing the Setup section 1.
Added more descriptive detail to Table 1.
Added schematic and PCB drawings for the rev. C version.

10.6 Revision 2.1 - July 2023

Corrected Kit Contents section on the first page that the included sample is LX7730LMFQ-ES not LX7730MFQ-ES.

10.7 Revision 2.2 - May 2024

Updated web links and minor document style elements.

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Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable"

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Quality Management System

For information regarding Microchip's Quality Management Systems, please visit https://www.microchip.com/quality.

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