IS62C256

32K x 8 LOW POWER CMOS STATIC RAM

FEATURES

- Access time: 45, 70 ns
- Low active power: 200 mW (typical)
- Low standby power
  - — 250 µW (typical) CMOS standby
  - — 28 mW (typical) TTL standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply

DESCRIPTION

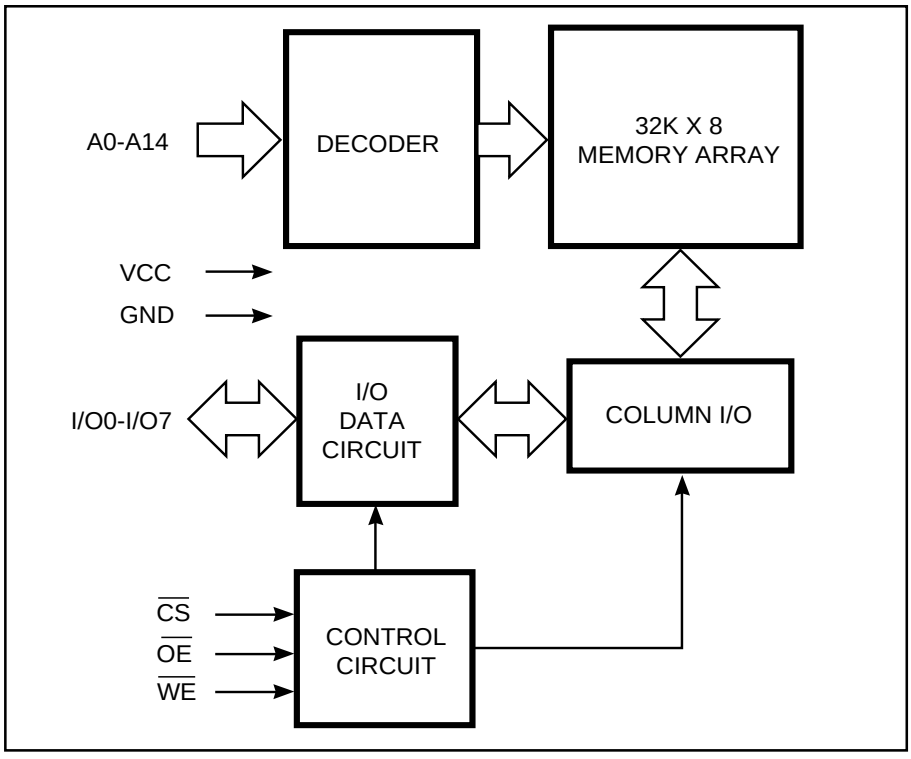
The *ISSI* IS62C256 is a low power, 32,768 word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance, low power CMOS technology.

When $\overline{CS}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) at CMOS input levels.

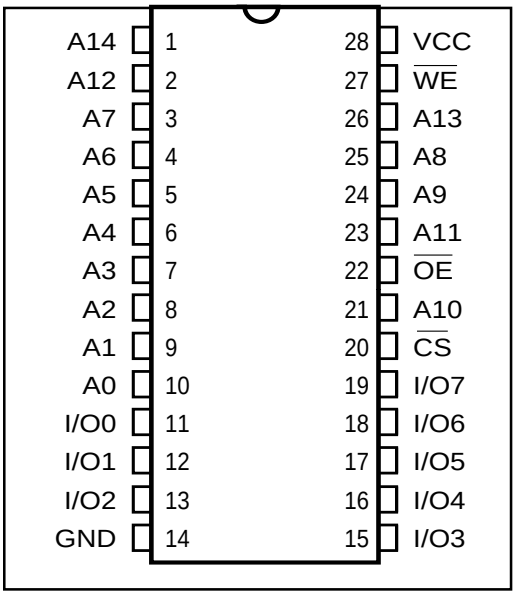
Easy memory expansion is provided by using an active LOW Chip Select ($\overline{CS}$) input and an active LOW Output Enable ($\overline{OE}$) input. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62C256 is pin compatible with other 32K x 8 SRAMs in plastic SOP or TSOP (Type I) package.

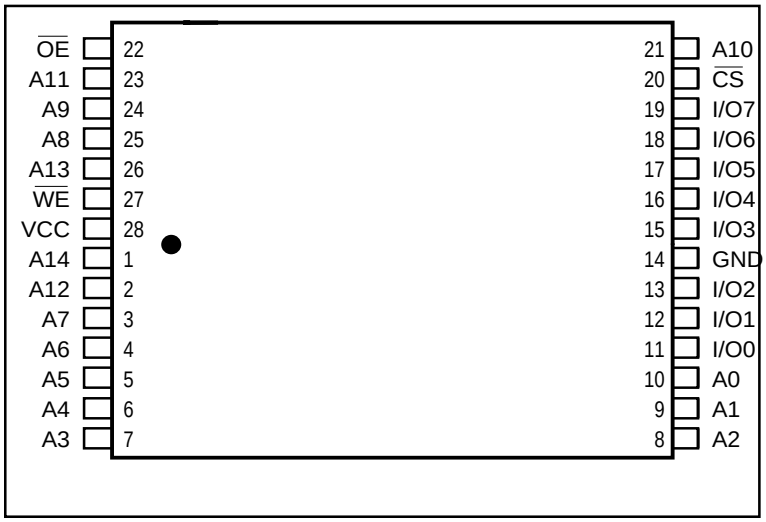
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin SOP



PIN CONFIGURATION
28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–2 –10	2 10	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com. Ind.	–2 –10	2 10	µA

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	Unit
I_{CC1}	Vcc Operating Supply Current	V_{CC} = Max., $\overline{CS}$ = V_{IL} I_{OUT} = 0 mA, f = 0	Com. Ind.	— —	60 70	— —	60 70	mA
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CS}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	70 80	— —	65 75	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS}$ ≥ V_{IH}, f = 0	Com. Ind.	— —	5 10	— —	5 10	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	— —	0.5 1.0	— —	0.5 1.0	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{DR}	V_{CC} for retention of data		2.0	—	V
I_{DR1}	Data retention current	V_{DR} = 3.0V, T_A = 0°C to +25°C	—	200	µA
I_{DR2}	Data retention current	V_{DR} = 3.0V, T_A = 0°C to +70°C	—	200	µA

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-45 ns		-70 ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	45	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	70	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACS}	$\overline{CS}$ Access Time	—	45	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	20	0	25	ns
t_{LZCS}[2]	$\overline{CS}$ to Low-Z Output	3	—	3	—	ns
t_{HZCS}[2]	$\overline{CS}$ to High-Z Output	0	20	0	25	ns
t_{PU}[3]	$\overline{CS}$ to Power-Up	0	—	0	—	ns
t_{PD}[3]	$\overline{CS}$ to Power-Down	—	30	—	50	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

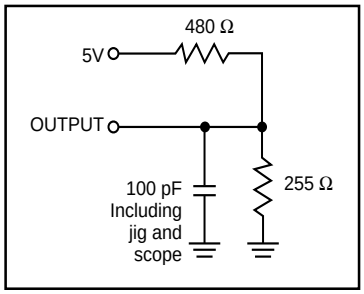


Figure 1.

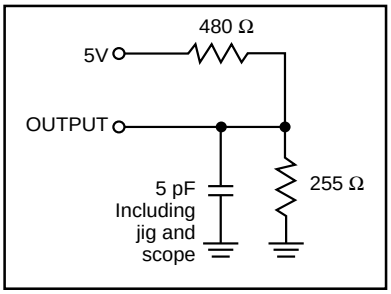
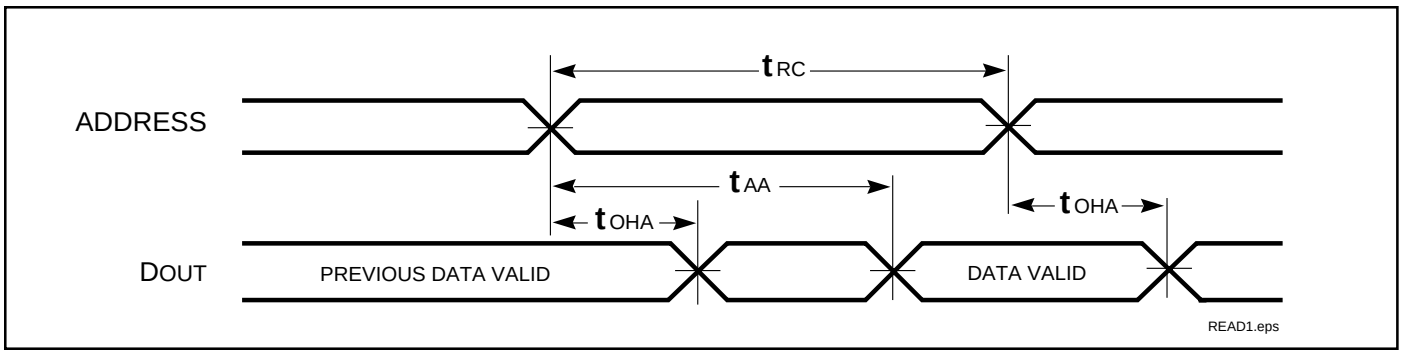


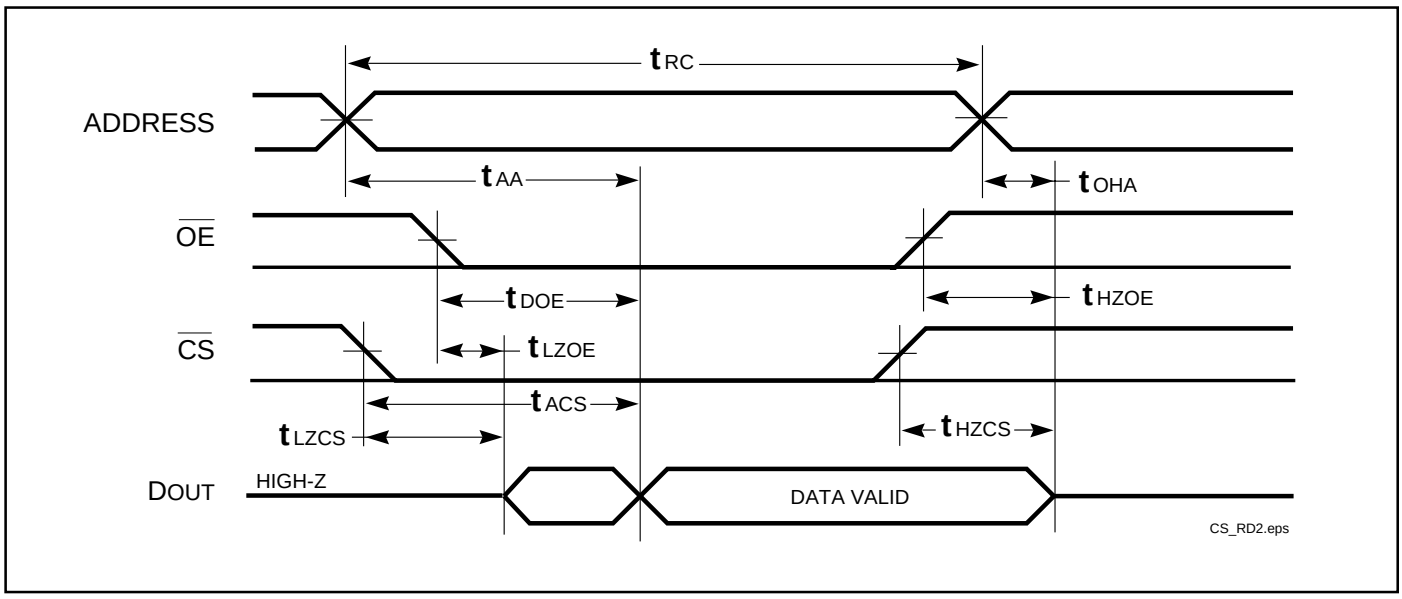
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CS}$ LOW transitions.

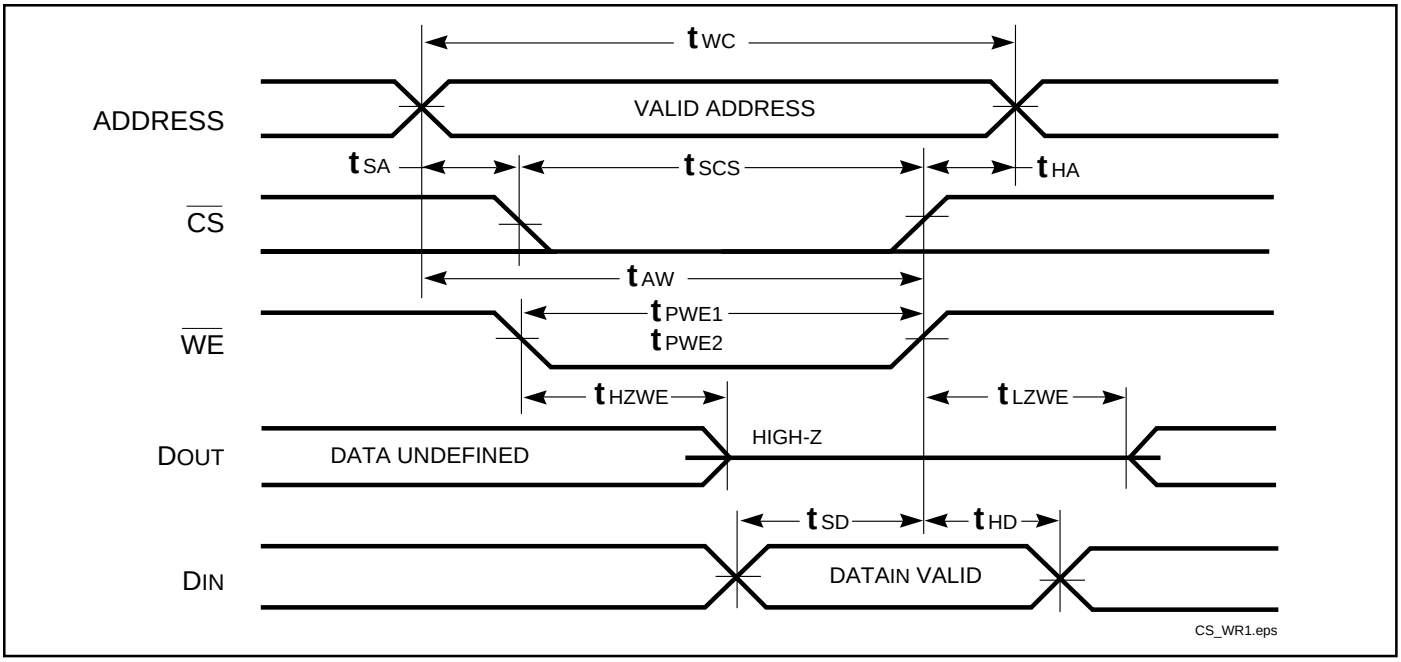
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-45 ns Min.	-45 ns Max.	-70ns Min.	-70ns Max.	Unit
t_{WC}	Write Cycle Time	45	—	70	—	ns
t_{SCS}	$\overline{CS}$ to Write End	35	—	60	—	ns
t_{AW}	Address Setup Time to Write End	25	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	25	—	55	—	ns
t_{SD}	Data Setup to Write End	20	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ HIGH.

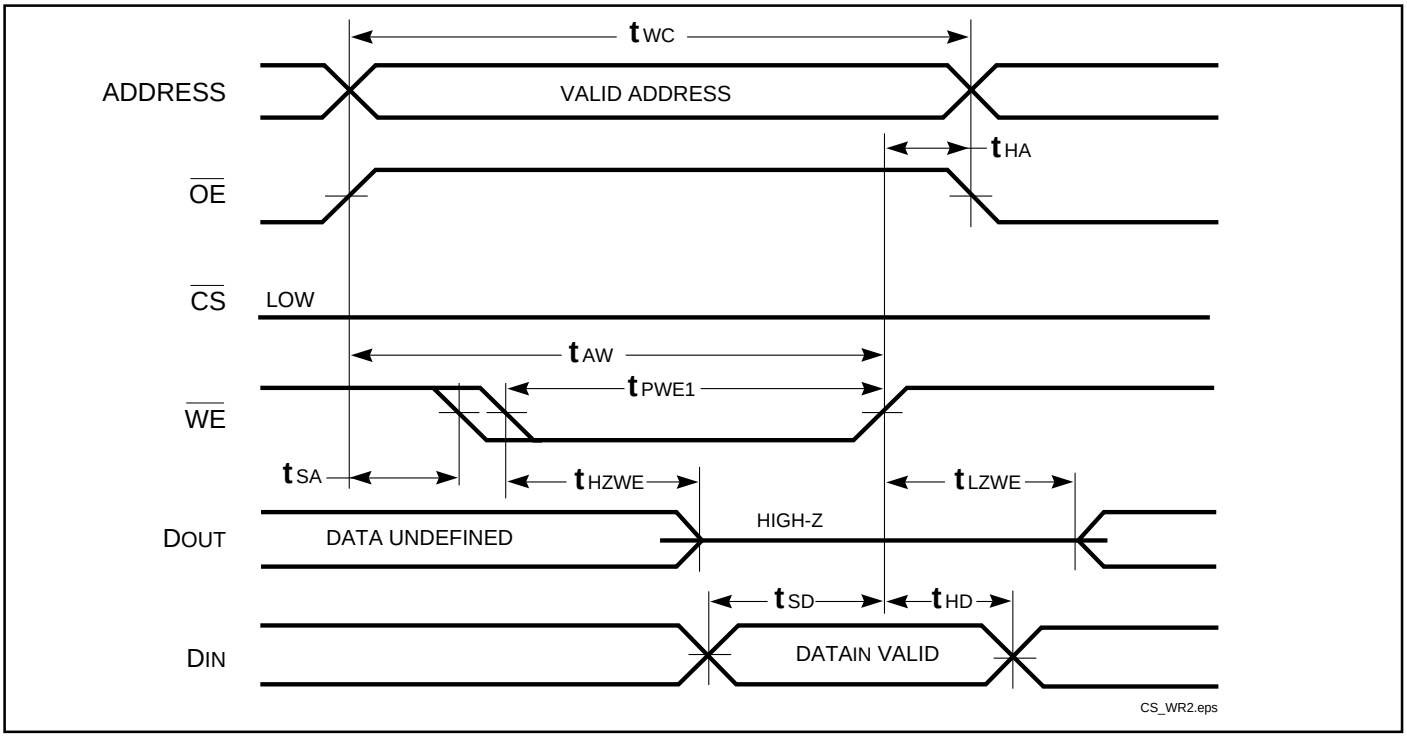
AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{CS}$ Controlled, $\overline{OE}$ is HIGH or LOW) [1]

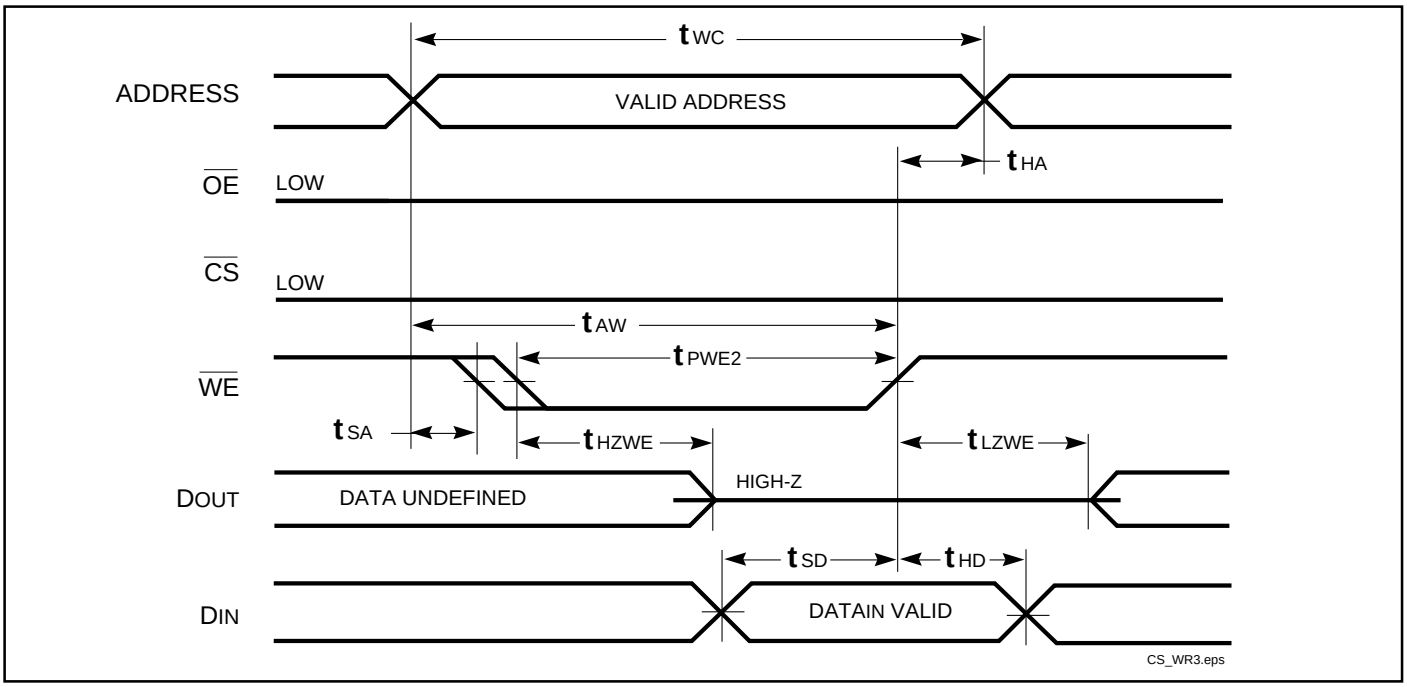


AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) (1,2)



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) (1)



Notes:

1. The internal write time is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

ORDERING INFORMATION
Commerical Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62C256-45T	TSOP
	IS62C256-45U	Plastic SOP
70	IS62C256-70T	TSOP
	IS62C256-70U	Plastic SOP

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62C256-45TI	TSOP
	IS62C256-45UI	Plastic SOP
70	IS62C256-70TI	TSOP
	IS62C256-70UI	Plastic SOP

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