Automotive 2V to 36V, 6A Buck-Boost Converters

MAX25239/MAX25240

General Description

The MAX25239/MAX25240 are small, synchronous, buck-boost converters with integrated H-bridge switches. These ICs provide a fixed-output regulation voltage and an externally adjustable output voltage in the 3V to 20V range with an input voltage above, below, or equal to the output regulation voltage. The ICs have typical 8.2A and 10A input current limit options and can support continuous load currents up to 6A depending on the input-to-output voltage ratio and operating frequency. The devices also have a wide input voltage range of 2V to 36V.

The MAX25239/MAX25240 have three switching frequency options: 2.1MHz, 400kHz, and 200kHz. The 2.1MHz high switching frequency allows small external components and reduced output ripple, and guarantees no AM band interference, while the 400kHz or 200kHz switching frequency offers better efficiency and relieves the power consumption concern. The SYNC input allows three operation modes: skip mode with ultra-low quiescent current, forced fixed-frequency PWM operation, and synchronization to an external clock. The ICs also include spread-spectrum frequency modulation to minimize EMI interference.

The MAX25239/MAX25240 feature a power-OK (POK) indicator, undervoltage lockout, overvoltage protection, cycle-by-cycle current limit, and thermal shutdown. The ICs are available in small, 4.25mm x 4.25mm x 0.75mm, 22-pin FC2QFN and 5.00mm x 5.00mm x 0.75mm, 18-pin FCQFN packages.

Applications

- ADAS ECU
- Infotainment Systems
- Body Electronics
- Start-Stop Systems
- Point-of-Load Power Supplies

Benefits and Features

- Meets Stringent Automotive Quality and Reliability Requirements
  - 2V to 36V Operating Input Voltage Range Allows Operation in Cold-Crank Conditions
  - Tolerates Input Transients up to 42V
  - EN Pin Compatible up to 42V
  - 8.2A/10A Typical Input Current Limit
  - Fixed and Adjustable Output Voltage Options
  - -40°C to +125°C Grade 1 Automotive Temperature Range
- AEC-Q100 Qualified High Integration and Thermally Enhanced Package Reduces BOM Cost and Board Space
  - Integrated FETs H-Bridge Architecture
  - 2.1MHz/400kHz/200kHz Switching Frequency Options
  - Phase-Locked Loop (PLL) Frequency Synchronization
  - Thermally Enhanced, 22-Pin and 18-Pin FC2QFN Packages
- Low Quiescent Current Meets Stringent OEM Current Requirements
  - 95µA Quiescent Current in Standby Mode
  - 10µA Maximum Shutdown Current
- Reduced EMI Emissions at Switching Frequency
  - Spread-Spectrum Function Enabled/Disabled by SPS Pin
- Protection Features Improve System Reliability
  - Supply Undervoltage Lockout and Thermal Protection
  - Output PGOOD Indicator, Overvoltage, and Short-Circuit Protection

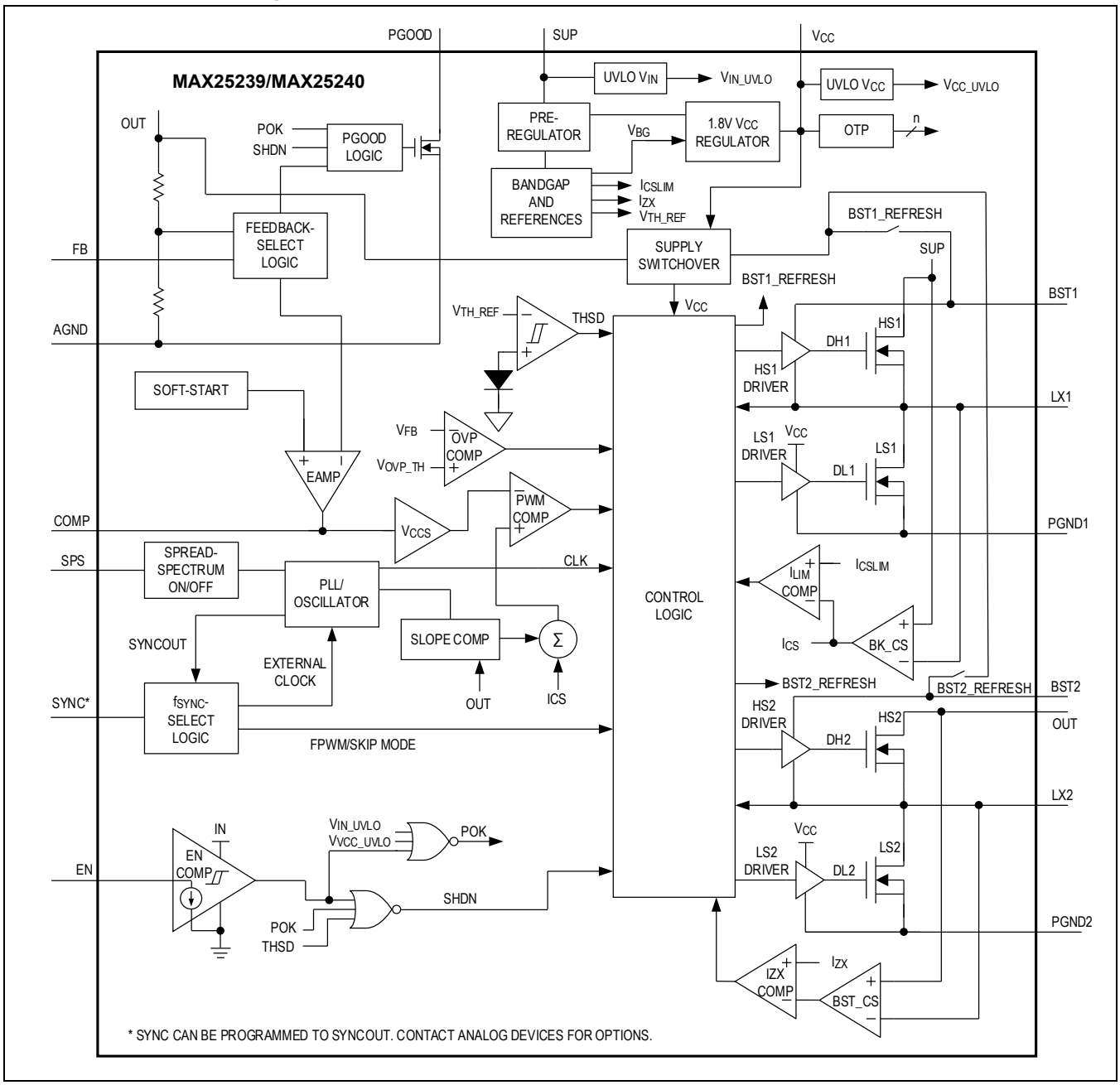
***Ordering Information* appears at end of data sheet.**

19-101236; Rev 14; 7/26

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Simplified Block Diagram



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Absolute Maximum Ratings

SUP, EN to AGND ..... -0.3V to +42V
LX1 to PGND1 ..... -0.3V to V_{SUP} +0.3V
LX2 to PGND2 ..... -0.3V to V_{OUT} +0.3V
OUT to AGND ..... -0.3V to +28V
BST1 to LX1, BST2 to LX2 ..... -0.3V to +2.2V
BST1 to PGND1 ..... -0.3V to +44V
BST2 to PGND2 ..... -0.3V to +30V
V_{CC}, SPS to AGND ..... -0.3V to +2.2V
COMP, FB to AGND ..... -0.3V to V_{VCC} +0.3V
PGND_ to AGND ..... -0.3V to +0.3V
SYNC, PGOOD to AGND ..... -0.3V to +6V
ESD Protection .....
Human Body Model ..... ±2kV
Machine Model ..... ±100V
Continuous Power Dissipation (T_A = +70°C, derate 30mW/°C above +70°C) 2404mW
Operating Junction Temperature ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

22 FC2QFN

Package Code	F224A4FY+1	
Outline Number	*21-100399*	
Land Pattern Number	*90-100137*	
THERMAL PARAMETERS	**4-LAYER JEDEC BOARD**	**4-LAYER EV KIT BOARD**
Junction-to-Ambient Thermal Resistance (θ_{JA})	33.3°C/W	22.4°C/W
Junction-to-Case (Top) Thermal Resistance (θ_{JCt})	6.8°C/W	—
Junction-to-Case (Bottom) Thermal Resistance (θ_{JCb})	6.4°C/W	7.5°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	7.6°C/W	9.6°C/W
Junction-to-Top Thermal Characterization Parameter (Ψ_{JT})	3.3°C/W	3.3°C/W
Junction-to-Bottom Thermal Characterization Parameter (Ψ_{JB})	8.5°C/W	9.4°C/W

18 FC2QFN

Package Code	F1855FY+1F	
Outline Number	*21-100745*	
Land Pattern Number	*90-100260*	
THERMAL PARAMETERS	**4-LAYER JEDEC BOARD**	**4-LAYER EV KIT BOARD**
Junction-to-Ambient Thermal Resistance (θ_{JA})	31.6°C/W	18.5°C/W
Junction-to-Case (Top) Thermal Resistance (θ_{JCt})	13.7°C/W	—
Junction-to-Case (Bottom) Thermal Resistance (θ_{JCb})	8.1°C/W	6.5°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	9.1°C/W	8.4°C/W
Junction-to-Top Thermal Characterization Parameter (Ψ_{JT})	2.9°C/W	2.2°C/W

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Junction-to-Bottom Thermal Characterization Parameter (Ψ_{JB})	8.9°C/W	8.8°C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. Note 1 and Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUP INPUT SUPPLY						
SUP Voltage Range	V_{SUP}	Initial start up	4.5		36	V
Shutdown Supply Current	$I_{SUP_SHUTDOWN}$	V_{EN} = 0V, T_A = +25°C		5	10	µA
Standby Supply Current	$I_{SUP_STANDBY}$	V_{EN} = V_{SUP}, V_{OUT} = 5V, no load, V_{SYNC} = 0V		95		µA
SUP Undervoltage Lockout	V_{UVLO_RISE}	V_{SUP} rising		4.2	4.45	V
	V_{UVLO_FALL}	V_{SUP} falling			1.9	
V_{CC} REGULATOR						
V_{CC} Output Voltage	V_{VCC}	V_{SUP} > 3.5V, I_{VCC} = 1mA to 50mA		1.8		V
V_{CC} Undervoltage Lockout	V_{UVLO_VCC}	V_{VCC} falling		1.6		V
	$V_{UVLO_VCC_HYS}$	V_{VCC} hysteresis, (Note 3)		100		mV
V_{CC} Short-Circuit Current Limit	I_{VCC_SC}	V_{CC} shorted to AGND		50		mA
BUCK-BOOST CONVERTER						
Fixed Output Voltage	V_{OUT_5V}	V_{FB} = V_{VCC}, FPWM = SYNC = 1.8V	4.9	5.0	5.1	V
	V_{OUT_11P5}	V_{FB} = V_{VCC}, FPWM = SYNC = 1.8V	11.27	11.5	11.73	
Soft-Start Ramp Time	t_{SOFT_START}			2.5		ms
Auto Retry Time	t_{AUTO}	Auto retry time after an output short condition is detected		5		ms
Minimum ON Time	t_{ON_MIN}	In buck mode, f_{SW} = 2.1MHz		100		ns
		In buck mode, f_{SW} = 400kHz, (Note 3)		125		
Dead Time	t_{DEAD}	(Note 3)		3		ns
LX1, LX2 Rise Time	t_{LX_RISE}	(Note 3)		1.5		ns
LX1, LX2 Fall Time	t_{LX_FALL}	(Note 3)		3		ns
POWER MOSFET						
DMOS On-Resistance	R_{DSON_DMOS}	V_{VCC} = 1.8V, I_{DSON} = 0.2A		20	35	mΩ
LX1 Leakage Current	I_{LX1_LKG}	V_{EN} = 0V, V_{SUP} = V_{LX1} = 36V, T_A = +25°C			5	µA
LX2 Leakage Current	I_{LX2_LKG}	V_{EN} = 0V, V_{LX2} = 12V, T_A = +25°C			5	µA
CURRENT SENSE						
Current Limit	I_{LIM}	10A, (Note 4)	8	10	12	A
		8.2A	6.8	8.2	9.5	

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(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. *Note 1* and *Note 2*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		12A, (*Note 5*)		10	12	14	
ERROR AMPLIFIER							
Regulated Feedback Voltage	V_{FB}			0.786	0.800	0.814	V
Feedback Leakage Current	I_{FB_LKG}	V_{FB} = 0.8V, T_A = +25°C			0.02	1	µA
Transconductance (from FB to COMP)	g_M	V_{FB} = 0.8V, V_{VCC} = 1.8V		85	100	115	µS
SWITCHING FREQUENCY							
PWM Switching Frequency	f_{SW}	400kHz option		350	400	450	kHz
		2.1MHz option		1.9	2.1	2.3	MHz
SYNC External Clock Input	f_{SYNC}	Minimum sync pulse of 100ns	400kHz option	280		520	kHz
			2.1MHz option	1.5		2.7	MHz
Spread Spectrum	SPS				±6		%
OUTPUT MONITORS							
Output Overvoltage Threshold	V_{OUT_OVP}	Detected with respect to V_{FB} rising		106	108	110	%
Output Overvoltage Hysteresis	$V_{OUT_OVP_HYS}$				3		%
PGOOD Threshold	V_{PGOOD_TH}	% of V_{OUT}, V_{OUT} rising		92	94	96	%
		% of V_{OUT}, V_{OUT} falling		91	93	95	
PGOOD Output Low Voltage	V_{PGOOD_LOW}	I_{SINK} = 1mA				0.2	V
PGOOD Leakage Current	I_{PGOOD_LKG}	V_{PGOOD} = 5.5V, T_A = +25°C				1	µA
PGOOD Debounce Time	t_{PGOOD_DB}	Fault detection, rising and falling			40		µs
LOGIC INPUTS (EN, SYNC, SPS)							
Input High Level	V_{HIGH}	Voltage rising		1.3			V
Input Low Level	V_{LOW}	Voltage falling				0.5	V
Input Leakage Current (EN, SPS)	I_{IN_LEAK}	T_A = +25°C				1	µA
Input Leakage Current (SYNC)	I_{IN_LEAK}	T_A = +25°C, SYNC = 1.8V, EN = high			20	50	µA
THERMAL SHUTDOWN							
Thermal Shutdown Threshold	T_{SHDN}	*Note 3*			175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}	*Note 3*			20		°C

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design and characterization.

Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 3: Guaranteed by design, not production tested.

Note 4: Boost mode current limit.

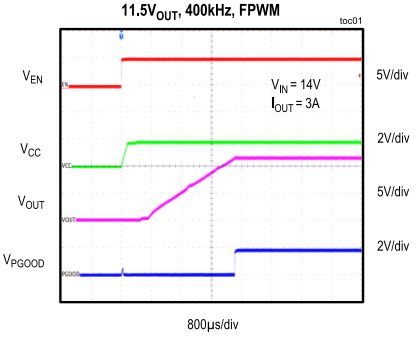
Note 5: Output short circuit not allowed, see the *Ordering Information* table specifications for further details.

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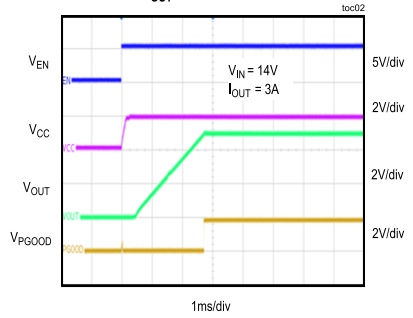
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

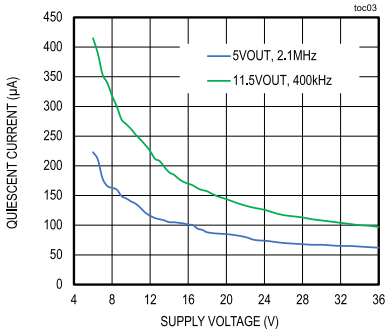
START UP INTO FULL LOAD
$11.5V_{OUT}$, 400kHz, FPWM



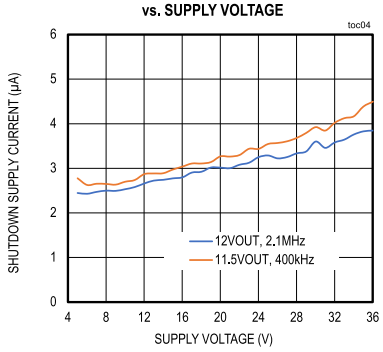
START UP INTO FULL LOAD
$5V_{OUT}$, 2.1MHz, FPWM



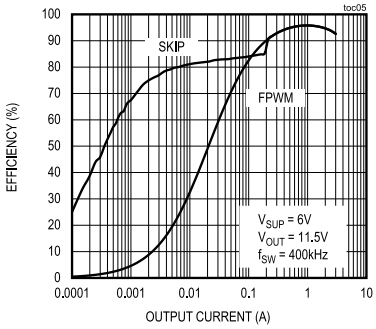
QUIESCENT CURRENT
vs. SUPPLY VOLTAGE



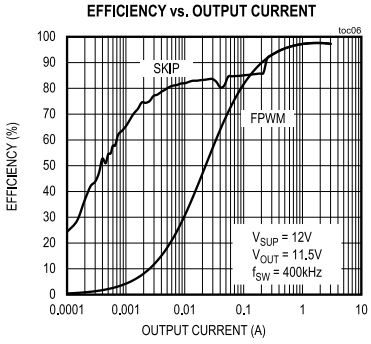
SHUTDOWN SUPPLY CURRENT
vs. SUPPLY VOLTAGE



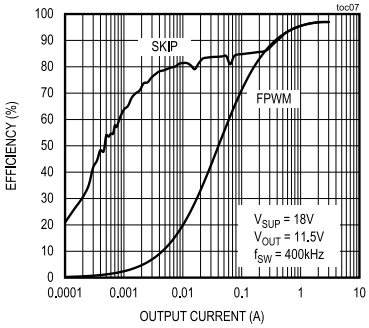
EFFICIENCY vs. OUTPUT CURRENT



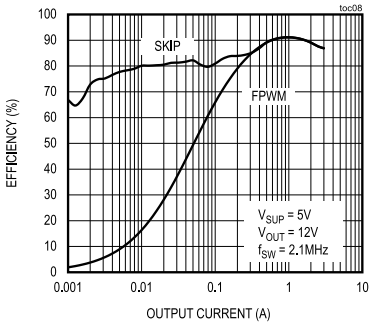
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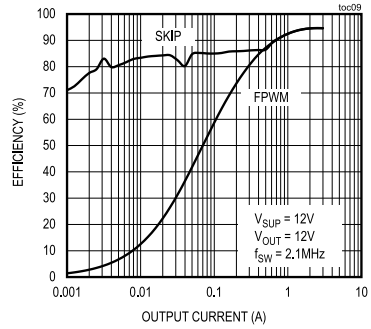
EFFICIENCY vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT



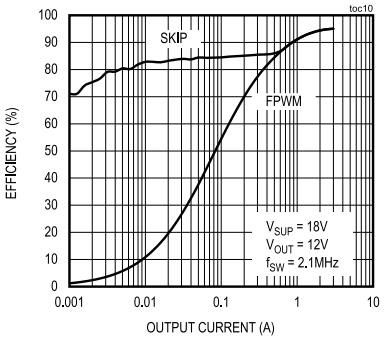
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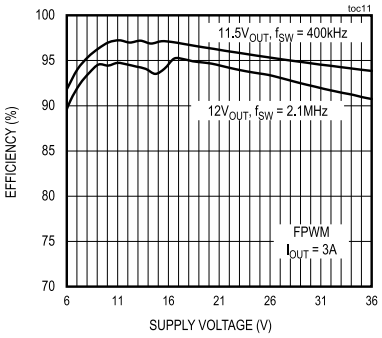
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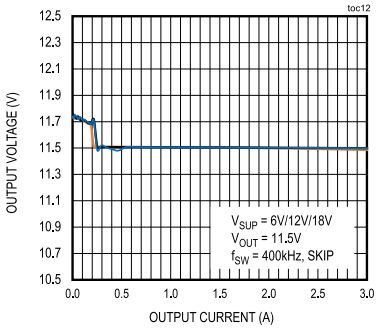
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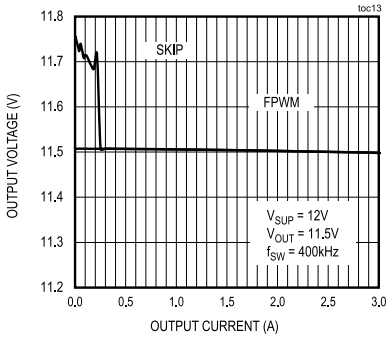
EFFICIENCY vs. SUPPLY VOLTAGE



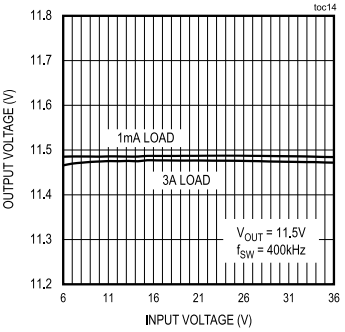
OUTPUT VOLTAGE LOAD REGULATION



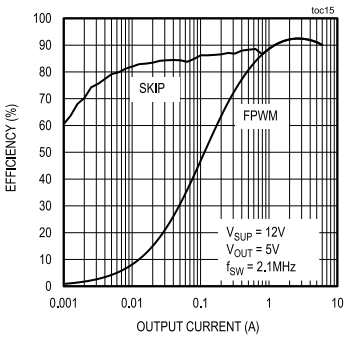
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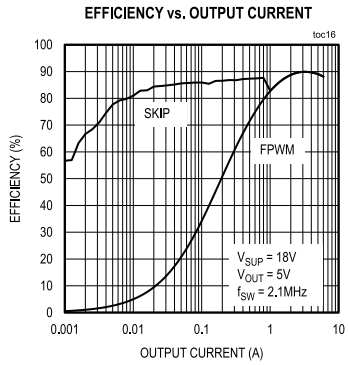
OUTPUT VOLTAGE LINE REGULATION



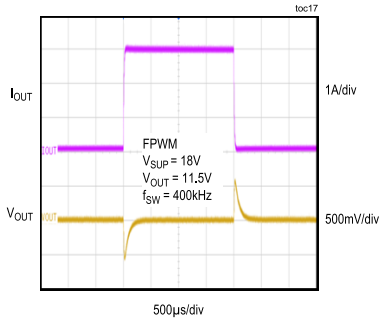
EFFICIENCY vs. OUTPUT CURRENT



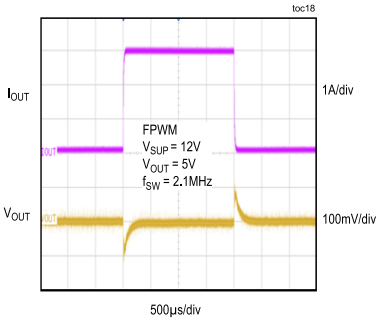
EFFICIENCY vs. OUTPUT CURRENT



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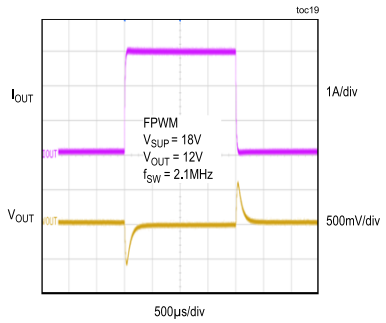
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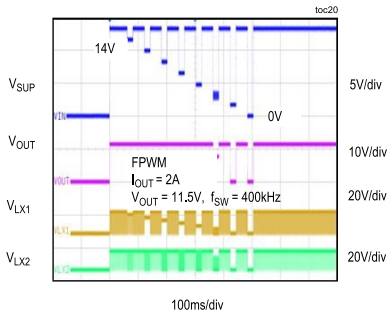
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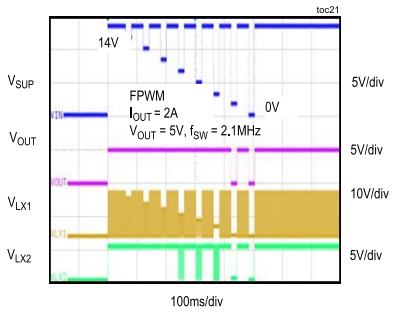
LOAD TRANSIENT RESPONSE



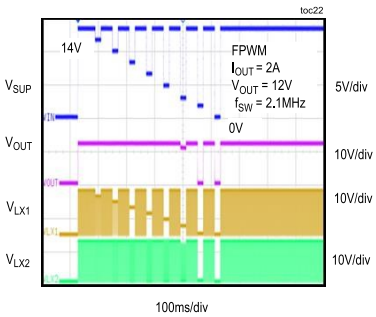
DIPS AND DROPS



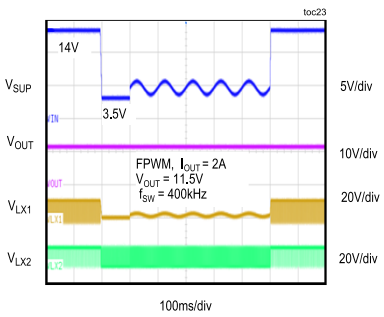
DIPS AND DROPS



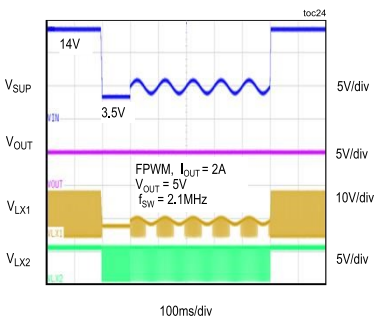
DIPS AND DROPS



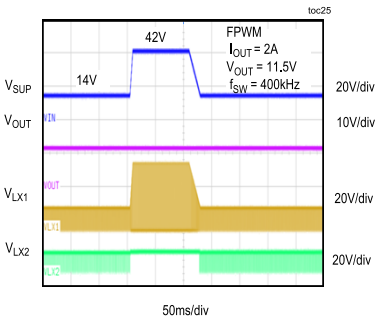
COLD CRANK



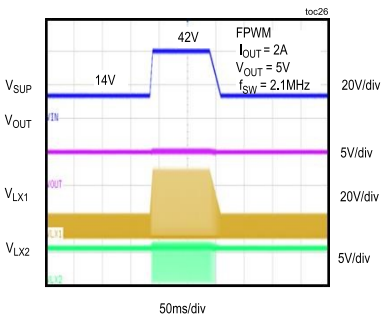
COLD CRANK



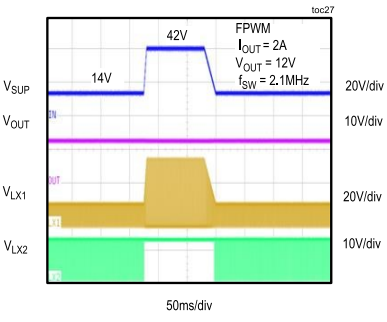
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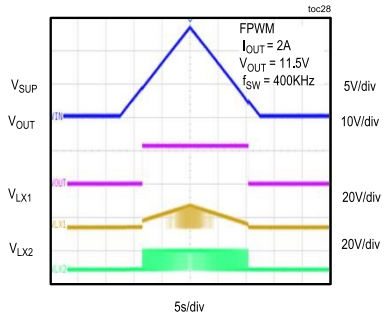
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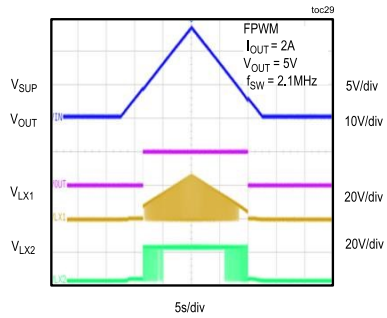
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(T_A = +25°C, unless otherwise noted.)

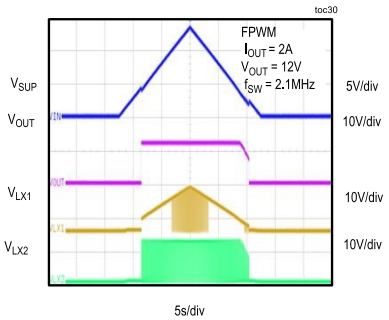
SLOW INPUT VOLTAGE RISING



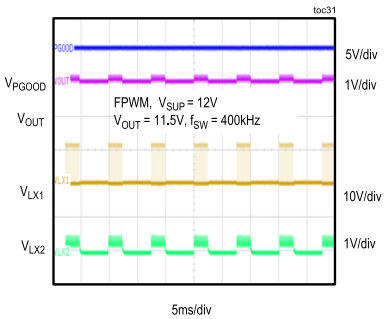
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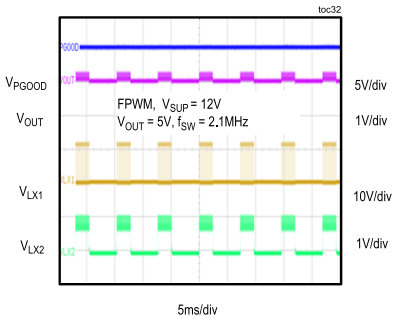
SLOW INPUT VOLTAGE RISING



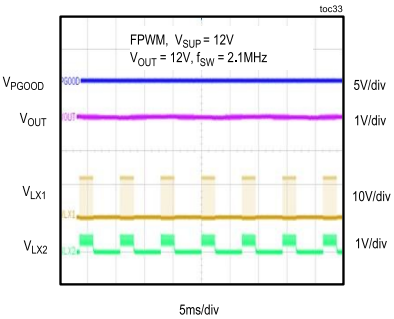
OUTPUT SHORT TO GROUND



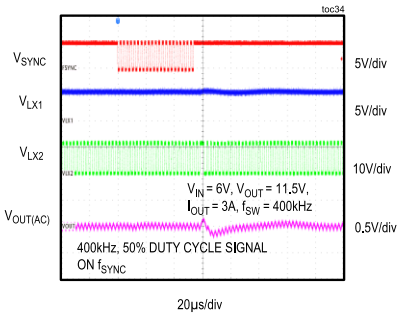
OUTPUT SHORT TO GROUND



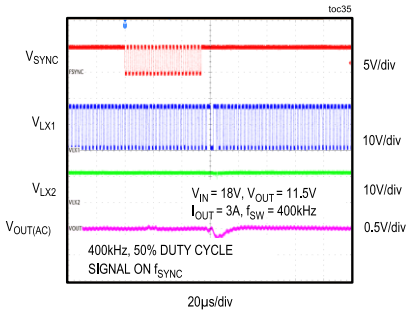
OUTPUT SHORT TO GROUND



f_{SYNC} SYNCHRONIZATION



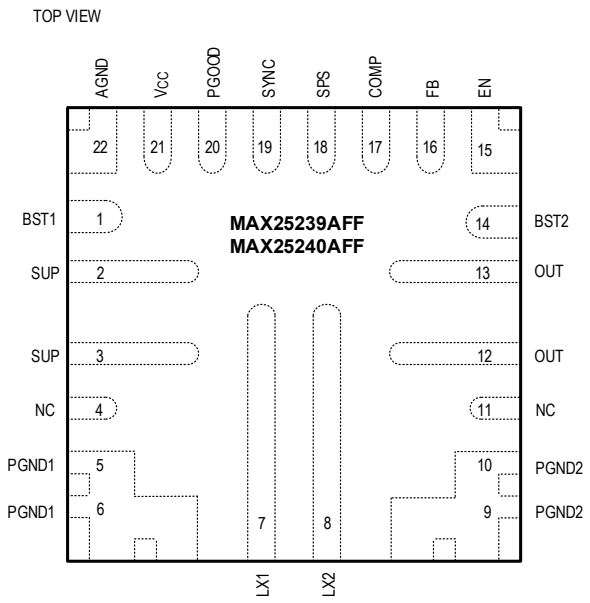
f_{SYNC} SYNCHRONIZATION



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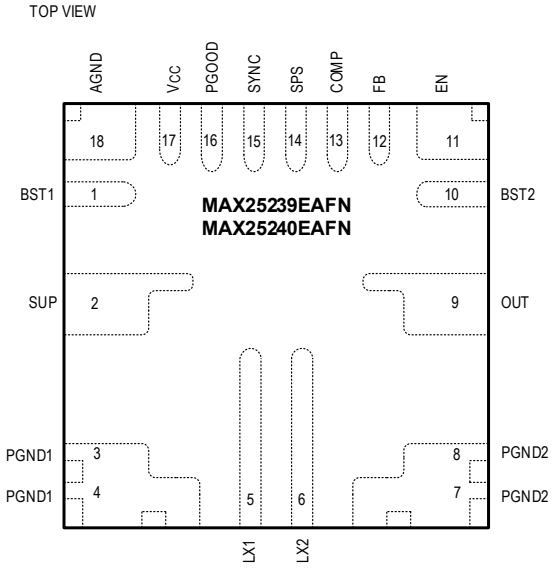
Pin Configurations

MAX25239AFF/MAX25240AFF



22-PIN FC2QFN
4.25mm x 4.25mm

MAX25239EAFN



18-PIN FC2QFN
5mm x 5mm

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Pin Descriptions

PIN		NAME	FUNCTION
MAX25239AFF/MAX25240AFF	MAX25239EAFN/MAX25240EAFN		
1	1	BST1	Bootstrap Capacitor Connection for Switching Node LX1. Connect a 0.1µF ceramic capacitor between LX1 and BST1.
2, 3	2	SUP	Power Supply of the Buck-Boost Converter and Internal V_{CC} LDO Regulator. Bypass SUP to PGND1 with a 4.7µF or larger ceramic capacitor.
4		NC	Not Connected
5, 6	3, 4	PGND1	Power Ground Connection for Buck Low-Side FET LS1. Connect PGND1 and PGND2 together to power ground.
7	5	LX1	Buck-Boost Converter Switching Node 1. Connect LX1 to one side of the power inductor.
8	6	LX2	Buck-Boost Converter Switching Node 2. Connect LX2 to the other side of the power inductor.
9, 10	7, 8	PGND2	Power Ground Connection for Boost Low-Side FET LS2. Connect PGND1 and PGND2 together to power ground.
11		NC	Not Connected
12, 13	9	OUT	Buck-Boost Converter Output
14	10	BST2	Bootstrap Capacitor Connection for Switching Node LX2. Connect a 0.1µF ceramic capacitor between LX2 and BST2.
15	11	EN	High-Voltage-Tolerant Enable Input. Drive EN high to enable buck-boost converter.
16	12	FB	Feedback Input. Connect FB to a resistor-divider between OUT and AGND to set the desired output voltage in the range of 3V to 20V. Connect FB to V_{CC} for the fixed output voltage option.
17	13	COMP	Error Amplifier Output. Connect an RC compensation network between COMP and AGND to stabilize the control loop.
18	14	SPS	Spread-Spectrum (SPS) Function Enable Input. Connect SPS high to enable SPS function and low to disable SPS function.
19	15	SYNC	External Clock Synchronization and Skip/PWM Mode Control Input. Connect SYNC to AGND to enable skip mode. Connect SYNC to V_{CC} to enable PWM mode. Connect SYNC to a valid external clock to synchronize the buck-boost converter switching frequency to external clock.
20	16	PGOOD	Open-Drain Power-Good Indicator. Pull up PGOOD with an external resistor to V_{CC} or a positive voltage lower than 5.5V to correctly indicate the OUT voltage status. PGOOD asserts low when the OUT voltage falls below 93% (typ) of its regulation voltage. PGOOD becomes high impedance when the OUT voltage rises above 94% (typ) of its regulation voltage. PGOOD is also low during soft-start and in shutdown.
21	17	V_{CC}	Internal 1.8V Regulator Output. Bypass V_{CC} to ground with a minimum 4.7µF ceramic capacitor.
22	18	AGND	Analog Ground. Connect AGND, PGND1, and PGND2 together at a single point in a star-ground connection.

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Detailed Description

The MAX25239/MAX25240 are small, synchronous buck-boost converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 6.0A with input voltages from +2.0V to +36V while using only 95µA quiescent current at no load. The MAX25239/MAX25240 provide an accurate output voltage of ±2% within the normal operation input range. Voltage quality can be monitored by observing the PGOOD signal.

The MAX25239/MAX25240 offer fixed output voltages and programmable output voltages in the range of 3V to 20V. Frequency is fixed with 200kHz, 400kHz, and 2.1MHz options. The 2.1MHz frequency allows for small external components and reduced output ripple, and guarantees no AM interference. The ICs automatically enter skip mode at light loads with a low quiescent current of 95µA at no load. They can operate with ±6% spread-spectrum frequency modulation designed to minimize EMI radiated emissions.

H-Bridge Operation

The MAX25239/MAX25240 H-bridge configuration is shown in the *Simplified Block Diagram*. The H-bridge consists of the four switches HS1, LS1, HS2, and LS2. Switches HS1 and LS1 are in series with the input voltage, and switches HS2 and LS2 are connected to the output. The inductor is connected between LX1 and LX2. There are three operation modes depending on the ratio of the input and output voltage: buck mode, boost mode, and buck-boost mode.

Buck Mode

When the input voltage is much higher than the output voltage, the MAX25239/MAX25240 operate in pure buck mode. In this mode, switch HS2 is always on and switch LS2 is always off, while switches HS1 and LS1 switch at the switching frequency. The ICs use an peak-current-mode control scheme to determine the ON pulse width for switches HS1 and LS1. Switches HS1 and LS1 will alternate, behaving like a synchronous buck converter.

Boost Mode

When the input voltage is much lower than the output voltage, the MAX25239/MAX25240 operate in pure boost mode. In this boost configuration, switch HS1 is always on and switch LS1 is always off, while switches HS2 and LS2 are operating at the switching frequency. The ICs use a peak-current-mode control scheme to determine the ON pulse width for switches HS2 and LS2. Switches HS2 and LS2 switch as a synchronous boost converter.

Buck-Boost Mode

With the input voltage close to the output voltage, the MAX25239/MAX25240 operate in buck-boost mode. During the buck-boost transition region, all four switches are turned on/off at the switching frequency as needed to maintain high efficiency and regulated output voltage in the transition region.

Operating Mode Transitions

Transitions between the boost, buck-boost, and buck operating modes in the MAX25239/MAX25240 are determined by duty-cycle limitations for each mode. The circuit is designed to switch between modes at thresholds that maintain good regulation accuracy.

The transition threshold between boost mode and buck-boost mode occurs at:

$V_{IN_TH} = (1 – k \times f_{SW})V_{OUT}$

where:

k = 87e-9s; internally preset minimum on-time value for boost mode

f_{SW} = Switching frequency

The transition between buck mode and buck-boost mode occurs at:

$V_{IN_TH} = V_{OUT}/D_{MAX}$

where:

D_{MAX} = Internally preset maximum duty factor

For the 400kHz trimmed parts, D_{MAX} = 0.89.

For the 2.1MHz trimmed parts, D_{MAX} =0.73.

There is no hysteresis at the transition thresholds.

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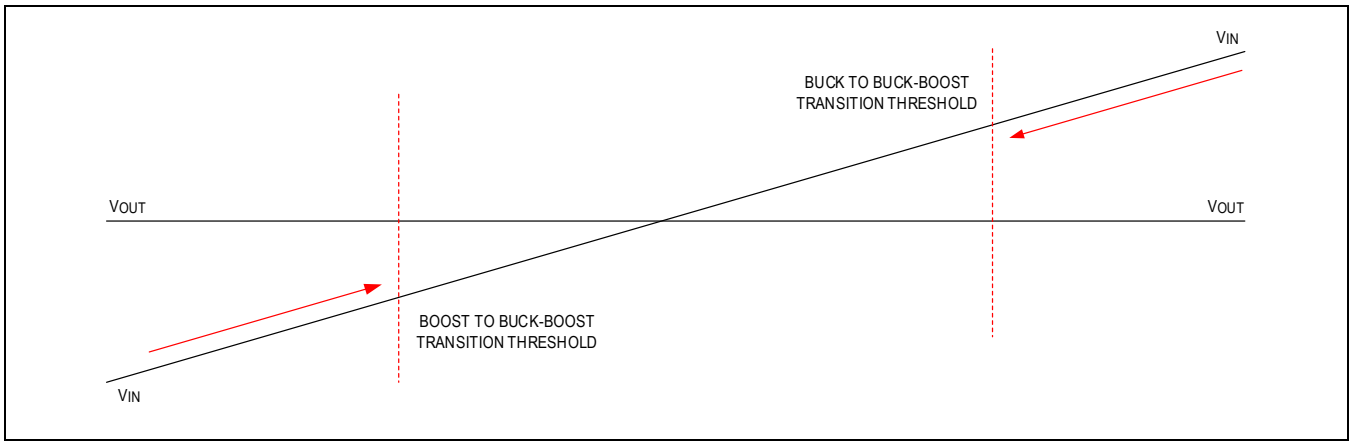


Figure 1. Input/Output Voltage at Buck-Boost Transition Boundary

For a MAX25239 that is configured for a 2.1MHz switching frequency with an adjustable output set to 15V, the boost to buck-boost threshold is approximately V_{IN} = 12.26V, and the buck to buck-boost threshold is approximately V_{IN} = 20.55V.

Linear Regulator Output (V_{CC})

The devices include a 1.8V linear regulator (V_{CC}) that provides power to the internal circuit blocks. Connect a 4.7µF (min) ceramic capacitor from V_{CC} to GND. During startup, the bias regulator draws power from the input and switches over to the output after the startup is complete. For output voltages less than 1.8V, the bias regulator is always supplied from the input.

Soft-Start

The MAX25239/MAX25240 include a 2.5ms soft-start time. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point. The soft-start ramp rate is set at 2.5ms.

Current-Limit/Hiccup Mode

The devices feature a current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short-circuit or overload condition is removed.

If the ICs reach the current limit with an output voltage below 50% of the target, hiccup mode is enabled and the output turns off for 5ms, then the IC attempts to power up through soft-start again.

Power-Good Output (PGOOD)

The devices feature an open-drain power-good indicator (PGOOD). PGOOD asserts low when the output voltage drops below the 93% (typ) falling threshold. PGOOD deasserts when the output voltage rises above the 94% (typ) rising threshold. Connect PGOOD to the output or external I/O voltage with a pull-up resistor.

Synchronization Input (SYNC)

The SYNC pin is a logic-level input used for operating mode selection and frequency control. Connecting SYNC to V_{CC} or to an external clock enables forced fixed-frequency (FPWM) operation. Connecting SYNC to GND enables automatic skip-mode operation for better light load efficiency. The external clock frequency at SYNC can be higher or lower than the internal clock by 20%. The devices synchronize to the external clock in two cycles. When the external clock signal at SYNC is absent for more than two clock cycles, the devices use the internal clock.

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System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with inputs from the automotive battery level down to 1.8V. EN turns on the internal linear (V_{CC}) regulator. Once V_{CC} is above the internal lockout threshold (V_{UVLO_VCC} = 1.7V, typ), the converter activates and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During shutdown, the V_{CC} regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5µA (typ). Drive EN high to bring the device out of shutdown.

Spread-Spectrum Option (SPS)

When the SPS pin is tied high, the operating frequency is varied ±6% centered on the switching frequency.

The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the external clock on the SYNC pin and pass any modulation (including spread spectrum) present driving the external clock.

Thermal Shutdown Protection

Thermal shutdown protects the device from excessive operating temperature. When the junction temperature exceeds +175°C, the sensor shuts down the converter, allowing the IC to cool. The sensor turns the IC on again after the junction temperature cools by 20°C. Thermal shutdown only disables the power switching, The V_{CC} regulator and IC logic remain active during thermal shutdown.

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Applications Information

Inductor Selection

Design of the inductor is a compromise between the size, efficiency, control, bandwidth, and stability of the converter. For a buck-boost application, selecting the right value of inductor becomes even more critical due to the presence of right-half-plane (RHP) zero in boost and buck-boost mode. A larger inductance value would reduce RMS current loss in MOSFETs, core, and winding losses in the inductor. On the other hand, it slows the control loop and reduces the frequency of the RHP zero, which can cause stability concerns.

Start the selection of the inductor based on the inductor peak-to-peak current ripple as a percentage of the maximum inductor current in buck and boost modes of operation using Equations 1, 2, and 3. Typically, 40% ripple of the maximum inductor current is a good compromise between speed and efficiency.

Equation 1:

$$L_{BUCK} = \frac{(V_{IN_MAX} - V_{OUT}) \times V_{OUT}}{f_{SW} \times \Delta I_{L_{P-P}} \times V_{IN_MAX}}$$

where:

V_{IN_MAX} = maximum input voltage

V_{OUT} = output voltage

ΔI_{LP-P} = peak-to-peak current ripple of the inductor

f_{SW} = switching frequency

Equation 2:

$$L_{BOOST} = \frac{(V_{OUT_MAX} - V_{IN}) \times V_{IN}}{f_{SW} \times \Delta I_{L_{P-P}} \times V_{OUT_MAX}}$$

where:

V_{IN} = input voltage

V_{OUT_MAX} = maximum output voltage

Select the larger of L_{BUCK} and L_{BOOST} as the final value of inductance L. Once the final value of inductance L is selected, calculate the actual peak inductor current using Equation 3 and choose an inductor with saturation current ≈20% more than the peak inductor current and the low DC resistance (DCR).

Equation 3:

$$I_{L_{PEAK}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN_MIN} \times \eta} + \frac{V_{IN_MIN} \times \left(1 - \frac{V_{IN_MIN}}{V_{OUT}}\right)}{L \times f_{SW} \times 2}$$

where:

V_{IN_MIN} = minimum input voltage

I_{OUT} = output current

η = power conversion efficiency

L = inductor value

Maximum Output Current

The MAX25239/MAX25240 sense the peak inductor current to limit the output current. The maximum output current is determined by the operating conditions and component selection that impact peak inductor current. At a heavy load and high output voltage, thermal limitations impact the output current capability. Use θ_{JA} to estimate the junction temperature at specific operating conditions to determine whether the device will trigger thermal shutdown.

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Input Capacitor

The input capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit switching. For operation in buck mode, the input capacitor sees high discontinuous input current. Both the equivalent series resistance (ESR) and capacitance of the input capacitors cause the peak-to-peak voltage ripple, as calculated in Equation 4.

Equation 4:

$$\triangle V_{IN} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT} \times ESR + \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT} \times V_{OUT}}{f_{SW} \times V_{IN} \times C_{IN}}$$

where:

ESR = equivalent series resistance of the input capacitor

I_{OUT} = output current

C_{IN} = capacitance of the input capacitor

With the given maximum input voltage ripple, the input capacitance is calculated as in Equation 5.

Equation 5:

$$C_{IN} = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT} \times V_{OUT}}{(V_{IN} \times \triangle V_{IN} - (V_{IN} - V_{OUT}) \times I_{OUT} \times ESR) \times f_{SW}}$$

The selected input capacitor should be designed to handle the input RMS current of the input capacitor calculated by Equation 6.

Equation 6:

$$I_{CIN_{RMS}} = \frac{I_{OUT} \text{ x } \sqrt{V_{OUT} \text{ x } (V_{IN} - V_{OUT})}}{V_{IN}}$$

where:

I_{CINRMS} = RMS current flowing through the input capacitor

The maximum input RMS current occurs at V_{IN} = 2 x V_{OUT} in Equation 7.

Equation 7:

$$I_{CIN_{RMS(MAX)}} = \frac{I_{OUT}}{2}$$

Select the input capacitors that can handle the given RMS current, as the RMS current flowing through the capacitor's ESR will produce power loss to make the temperature rise. Ceramic capacitors are recommended for their low ESR, ESL, small size, and high current ripple capability to bypass the pulsing ripple current, which helps reduce the peak-to-peak voltage ripple at the input voltage and electromagnetic interference (EMI).

Output Capacitor

In boost mode, the output capacitors see high discontinuous ripple current. Both equivalent series resistance (ESR) and capacitance of the output capacitors cause the voltage ripple, as calculated in Equation 8.

Equation 8:

$$\triangle V_{OUT} = \frac{V_{OUT} \times I_{OUT} \times ESR}{V_{IN} \times \eta} + \frac{I_{OUT} \times (1 - \frac{V_{IN}}{V_{OUT}})}{f_{SW} \times C_{OUT}}$$

where:

ESR = equivalent series resistance of the output capacitor

C_{OUT} = capacitance of the output capacitor

With the given maximum voltage ripple, the output capacitance is calculated as shown in Equation 9.

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Equation 9:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times V_{IN} \times I_{OUT} \times \eta}{(\triangle V_{OUT} \times V_{IN} \times \eta - V_{OUT} \times I_{OUT} \times ESR) \times V_{OUT} \times f_{SW}}$$

When the input voltage reaches the minimum value, and the output voltage reaches the maximum value, the output voltage is the largest.

Meanwhile the output capacitance is selected to satisfy the load transient requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitors, which causes an undershoot in the output voltage. Select a capacitor based on the maximum allowable undershoot on the output voltage. Typically, the worst-case response from a load transient is in boost mode. The output capacitance for the allowable undershoot is calculated under the load transient in boost mode, as in Equation 10.

Equation 10:

$$C_{OUT} = \frac{\triangle I_{OUT}}{2 \times \pi \times \triangle V_{OUT_{US}} \times f_C}$$

where:

f_C = crossover frequency

ΔI_{OUT} = transient load step

ΔV_{OUTUS} = maximum allowable undershoot

Select the larger output capacitance of Equation 9 and Equation 10 as the final value of the output capacitance C_{OUT} that can handle the given RMS current at the operating frequency. Ceramic capacitors are recommended for their low ESR, ESL, small size, and high current ripple capability to bypass the pulsing ripple current, which helps reduce the peak-to-peak voltage ripple at the output voltage and electromagnetic interference (EMI). The RMS ripple current of the output capacitors is calculated in Equation 11.

Equation 11:

$$I_{COUT_{RMS}} = I_{OUT} \times \sqrt{\frac{V_{OUT} - V_{IN}}{V_{IN}}}$$

Output Voltage Setting

Connect FB to V_{CC} to enable the fixed output voltage set by a preset internal resistive voltage-divider connected between the feedback pin (FB) and AGND. To externally adjust the output voltage between 3V and 20V, connect a resistive voltage-divider from the output (OUT) to FB to AGND, as shown in *Figure 2*. Calculate R_{FB1} and R_{FB2} using Equation 12.

Equation 12:

$$R_{FB1} = R_{FB2}[(\frac{V_{OUT}}{V_{FB}}) - 1]$$

where:

V_{FB} = 0.8V (typ)

R_{FB2} < 50kΩ, can be typically set to 10kΩ

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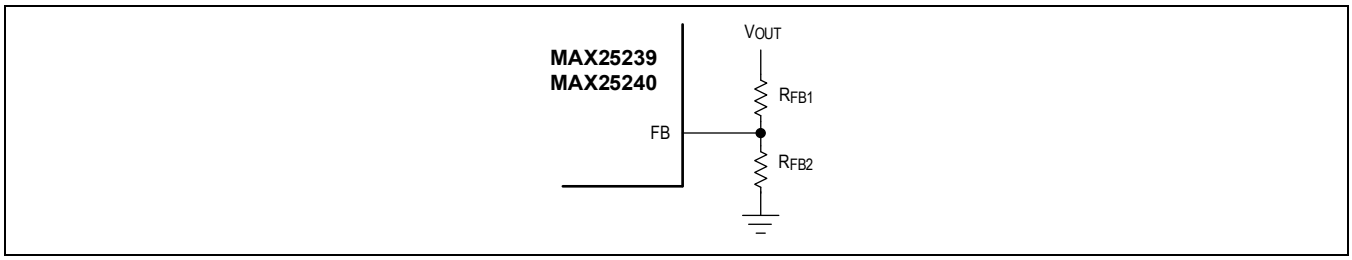


Figure 2. Output Voltage External Adjustment

Error Amplifier Compensation Design

The MAX25239/MAX25240 converters use an internal transconductance error amplifier, with its inverting input and output terminals available to the user for external frequency compensation (see *Figure 3*).

The controller uses a peak current-mode-controlled architecture that regulates the output voltage by forcing the required current through the external inductor. Current-mode control splits the double pole in the feedback loop caused by the inductor and output capacitor into two single poles. One of the poles is moved to a high frequency outside the typical bandwidth of the converter, making it a single-pole system. This makes compensation easy with just Type II required to compensate the loop. In boost mode, an extra right half-plane (RHP) zero is introduced by the power stage that adds extra phase delay in the control loop. To avoid any significant effect of the RHP zero on the converter stability, the compensation is designed such that the bandwidth is approximately 1/5 of the worst-case RHP zero frequency.

The design of external compensation requires some iterations to reach an optimized design. Care must be taken while designing the compensation for working in deep-boost mode and heavy load (V_{IN_MIN}), as the RHP zero frequency decreases.

A convenient way to design compensation for both buck and boost modes is to design the compensation at minimum input voltage and heavy load (deep-boost mode). At this operating point, RHP zero is at its lowest frequency. Design the compensation to achieve a bandwidth of 1/5 or lower of the RHP zero frequency to avoid significant effect of the RHP zero on the converter stability. The closed-loop gain of the converter would be a combination of the power-stage gain of the converter and error-amplifier gain, where the power stage's pole and zero are calculated in Equation 13.

Equation 13:

$$f_{PBOOST} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT}}$$

$$f_{ZESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

$$f_{ZRHP} = \frac{R_{LOAD} \times (1 - D)^2}{2 \times \pi \times L}$$

where the error amplifier's pole and zero are calculated in Equation 14:

Equation 14:

$$f_{P1EA} = \frac{1}{2 \times \pi \times (R_{EA} + R_C) \times C_C} \approx \frac{1}{2 \times \pi \times R_{EA} \times C_C}, \quad \text{if } R_{EA} \gg R_C$$

$$f_{P2EA} = \frac{1}{2 \times \pi \times R_C \times C_P}$$

$$f_{ZEA} = \frac{1}{2 \times \pi \times R_C \times C_C}$$

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where R_{EA} is the output impedance of the transconductance error amplifier with the value of approximately 5MΩ. ESR is the equivalent series resistance of the output capacitors. R_{LOAD} is the load resistance.

The target bandwidth for the closed-loop converter is selected to be 1/5 of the RHP zero. The zero of the error amplifier should be placed well below the bandwidth to give enough phase boost at the crossover frequency f_C. Typically, the zero of the transconductance error amplifier is placed close to the low-frequency pole f_{PBOOST} of the power stage. The second pole f_{P2EA} of the transconductance error amplifier is placed close to the RHP zero of the power stage. In such a case, the resistor R_C and capacitors C_C, C_P of the compensation network are calculated using Equation 15.

Equation 15:

$$R_C = \frac{2 \times \pi \times R_i \times C_{OUT} \times V_{OUT} \times f_C}{(1 - D) \times G_m \times V_{REF}}$$

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C}$$

$$C_P = \frac{1}{2 \times \pi \times R_C \times f_{ZRHP}}$$

where:

R_i = 50mΩ current-sensing resistor

G_M = 100µA/V gain of the transconductance error amplifier

f_C = Selected crossover frequency

V_{REF} = 0.8V reference of the feedback voltage

The internal compensation network is shown in *Figure 3*.

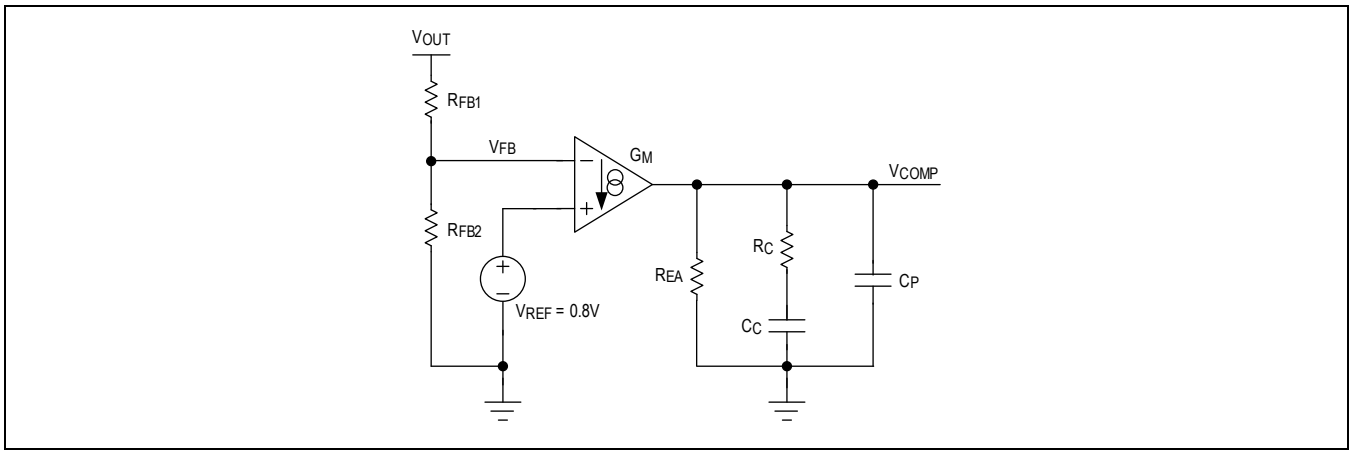


Figure 3. Compensation Network

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PCB Layout Guidelines

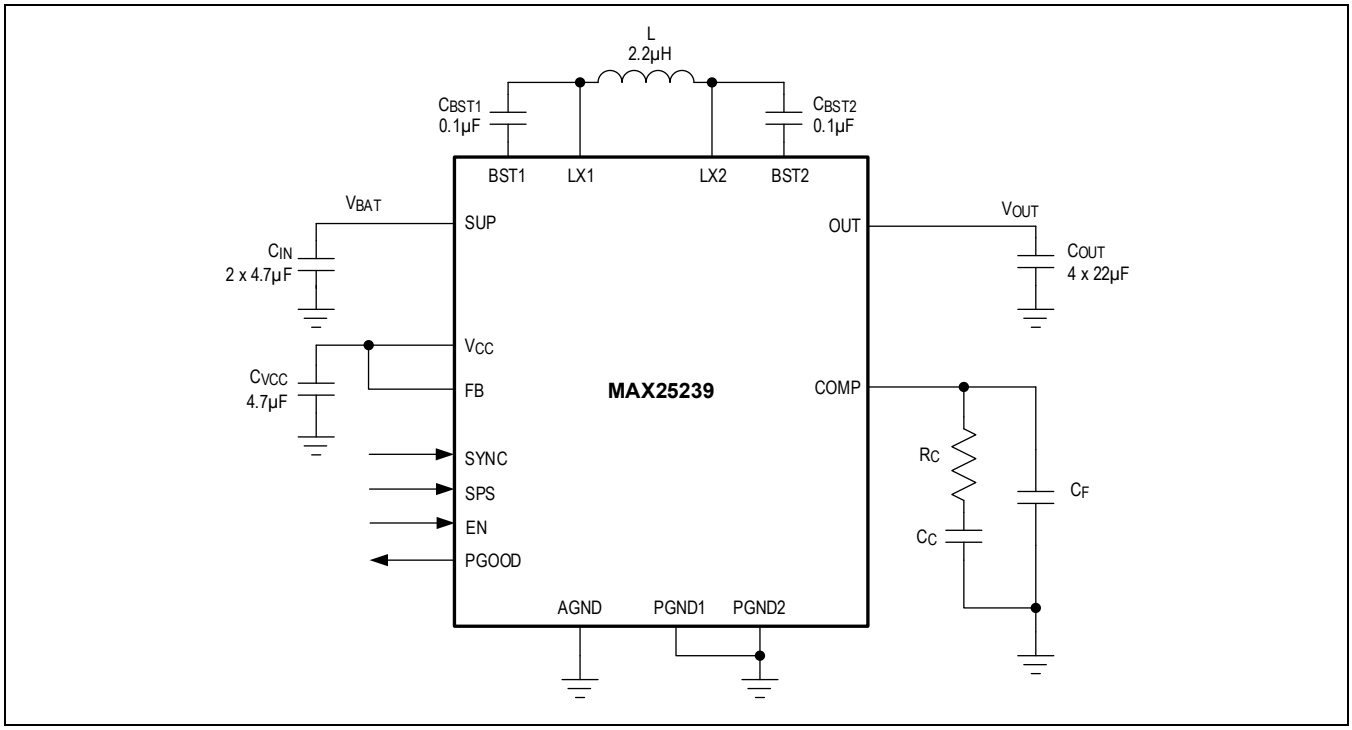
Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1. Place ceramic bypass capacitors close to the input and output pins to minimize high frequency current loops. This improves efficiency and helps minimize radiated emissions.
2. Place V_{CC} bypass capacitors close to the IC between the V_{CC} and AGND pins.
3. Orient the input and output capacitors to minimize the distance between their ground connections.
4. Isolate the power ground from the analog ground whenever possible. Connect the power ground to the analog ground with a star-ground connection at the AGND pin. This keeps the ground-current loops to a minimum. In cases where only one ground is used, adequate isolation between the analog return signals and high-power signals must be maintained.
5. Minimize trace inductance between the LX pins and BST capacitors, placing ceramic bootstrap capacitors as close as possible to the BST1 and BST2 pins.
6. Isolate the power components and high-current path from the sensitive analog circuitry in the compensation and feedback loops. This is essential to prevent noise coupling into the analog signals.
7. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path (composed of an input capacitor, high-side FET, inductor, and output capacitor) should be as short as possible.
8. Keep the power traces and load connections short and wide. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency and thermal dissipation.
9. The analog signal lines should be routed away from the high-frequency planes. This ensures the integrity of sensitive signals feeding back into the device.
10. Place compensation components as close to the COMP pin as possible.

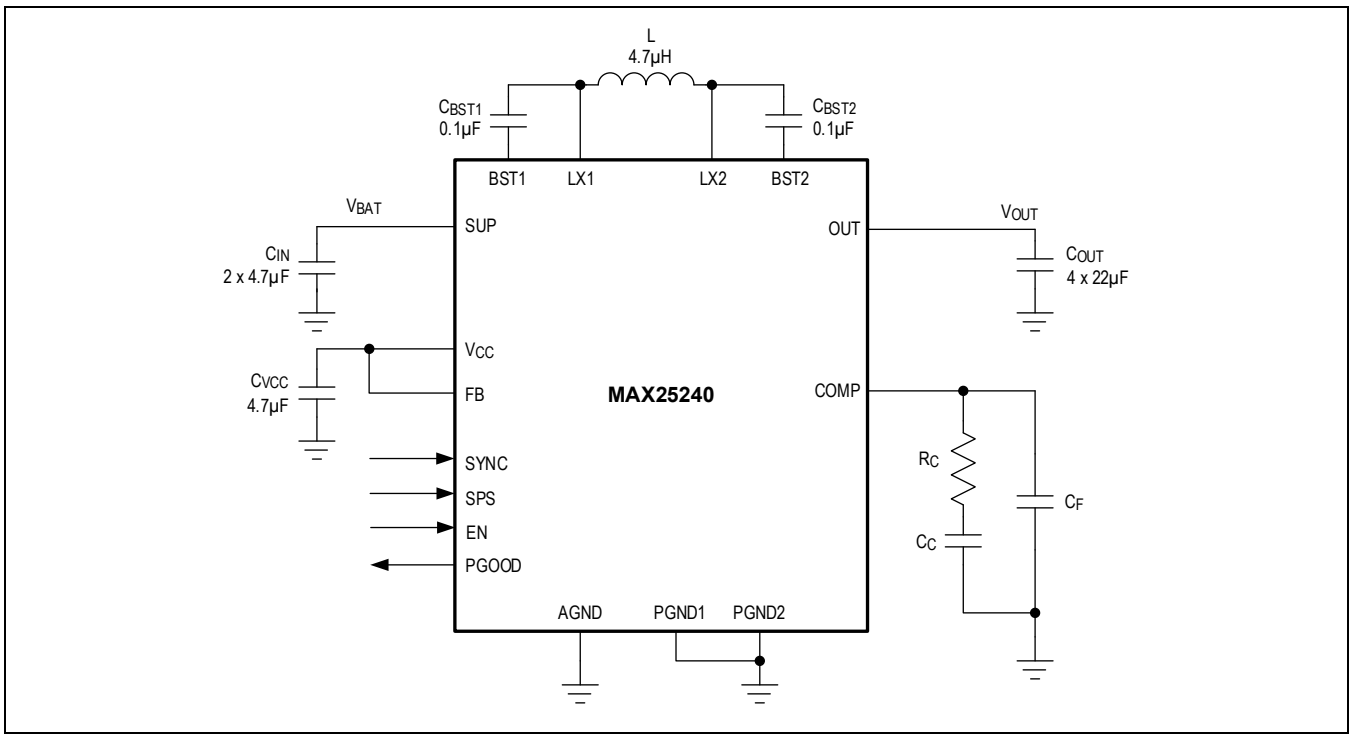
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Typical Application Circuits

2.1MHz Application Circuit: I_{LIM} = 8.2A, V_{OUT} = 5V



400kHz Application Circuit: I_{LIM} = 10A, V_{OUT} = 5V



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Ordering Information

PART NUMBER	CURRENT LIMIT I_{LIM} (A)	FIXED V_{OUT} OPTIONS (V)**	ADJ V_{OUT} (V)	SWITCHING FREQUENCY (kHz)
MAX25239AFFA/VY+	8.2	5	<6.5	2100
MAX25239AFFB/VY+	8.2	5	<6.5	400
MAX25239AFFD/VY+	8.2	10.5	>6.5	2100
MAX25239EAFNA/VY+	8.2	5	<6.5	2100
MAX25239AFFF/VY+	8.2	15	>6.5	400
MAX25239AFFI/VY+*	8.2	15	>6.5	2100
MAX25240AFFA/VY+	10	5	<6.5	2100
MAX25240AFFB/VY+	10	5	<6.5	400
MAX25240AFFD/VY+	10	10.5	>6.5	2100
MAX25240AFFF/VY+	8.2	11.5	>6.5	400
MAX25240AFFG/VY+^	12	10.5	>6.5	2100

/V denotes an automotive-qualified part.

+ denotes a lead(Pb)-free/RoHS-compliant package.

T denotes tape-and-reel.

^ 18V max operating V_{IN}, 5A max average I_{OUT}.

** Potential future product.*

*** Contact factory for options that include:*

- *Fixed V_{OUT} options from 3V to 15V*
- *SYNC input or output*
- *PGOOD assertion time delay options of 5ms and 10ms*

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/21	Initial release	—
1	1/22	Updated Ordering Information table	23
2	2/22	Updated Ordering Information table	23
3	2/22	Updated Ordering Information table	23
4	3/22	Updated Ordering Information table	23
5	4/22	Updated Ordering Information table	23
6	7/22	Updated Ordering Information table	23
7	9/22	Updated Electrical Characteristics and Ordering Information table	6, 23
8	12/22	Updated Ordering Information table	23
9	4/23	Updated Ordering Information table	23
10	6/23	Updated Package Information Thermal Parameters, Detailed Description, Applications Information, and Figure 4	5, 14, 18, 22
11	9/24	Updated General Description, Benefits and Features, Package Information, Pin Configurations, Pin Descriptions, Ordering Information table	1, 5, 6, 13, 14, 24
12	3/26	Updated Header, Updated Electrical Characteristics, Pin Configurations, Detailed Description, Ordering Information table	All, 6, 14, 15, 24
13	4/26	Updated Ordering Information table	24
14	7/26	Updated Header, Updated Electrical Characteristics, Pin Configurations, Detailed Description, Ordering Information table	All

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