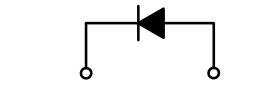
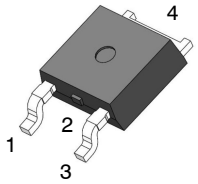
Silicon Carbide (SiC) Schottky Diode – EliteSiC, 6 A, 650 V, D2, DPAK

FFSD0665B



Schottky Diode



DPAK
CASE 369AS

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

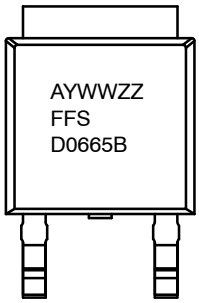
Features

- Max Junction Temperature 175°C
- Avalanche Rated 24.5 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

MARKING DIAGRAM



A	= Assembly Plant Code
YWW	= Date Code (Year & Week)
ZZ	= Lot Code
FFSD0665B	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Peak Repetitive Reverse Voltage		V_{RRM}	650	V
Single Pulse Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 9.9 A, L = 0.5 mH, V = 50 V)		E_{AS}	24.5	mJ
Continuous Rectified Forward Current	T_C < 154	I_F	6.0	A
	T_C < 135		9.1	
Non−Repetitive Peak Forward Surge Current	T_C = 25°C, t_P = 10 μs	I_{FM}	493	A
	T_C = 150°C, t_P = 10 μs		442	
Non−Repetitive Forward Surge Current (Half−Sine Pulse)	T_C = 25°C t_P = 8.3 ms	I_{FSM}	28	A
Power Dissipation	T_C = 25°C	P_{tot}	75	W
	T_C = 150°C		12.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.0	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ON CHARACTERISTICS						
V_F	Forward Voltage	I_F = 6.0 A, T_J = 25°C		1.38	1.7	V
		I_F = 6.0 A, T_J = 125°C		1.53	2.0	
		I_F = 6.0 A, T_J = 175°C		1.67	2.4	
I_R	Reverse Current	V_R = 650 V, T_J = 25°C		0.5	40	μA
		V_R = 650 V, T_J = 125°C		1.0	80	
		V_R = 650 V, T_J = 175°C		2.0	160	
CHARGES, CAPACITANCES & GATE RESISTANCE						
Q_C	Total Capacitive Charge	V_C = 400 V		16		nC
C_{tot}		V_R = 1 V, f = 100 kHz		259		pF
		V_R = 200 V, f = 100 kHz		29		
		V_R = 400 V, f = 100 kHz		22		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PART MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method†	Reel Size	Tape Width	Quantity
FFSD0665B	FFSD0665B	DPAK	Tape & Reel	330 mm	16 mm	2500 units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

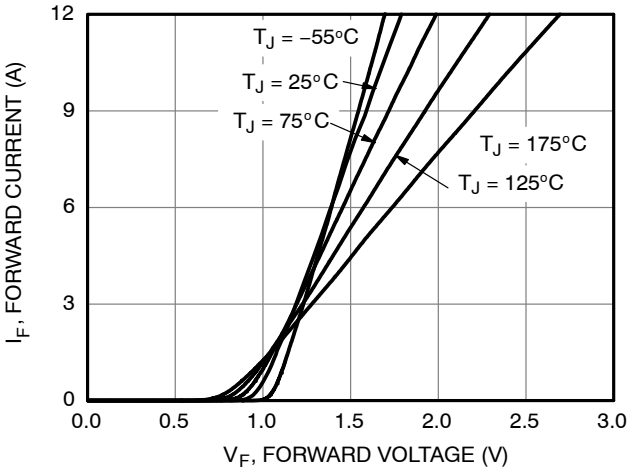


Figure 1. Forward Characteristics

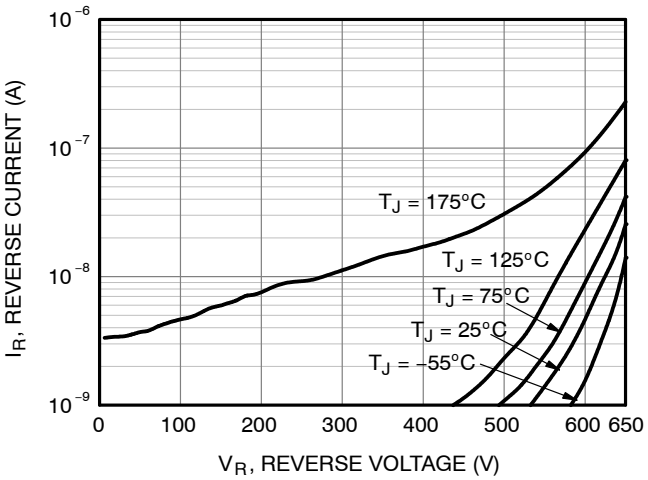


Figure 2. Reverse Characteristics

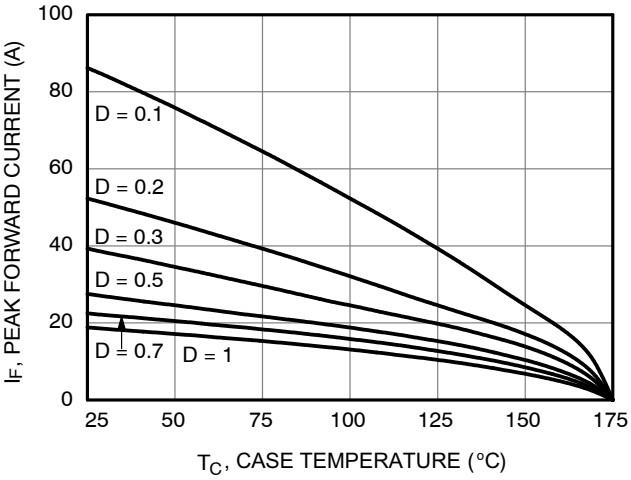


Figure 3. Current Derating

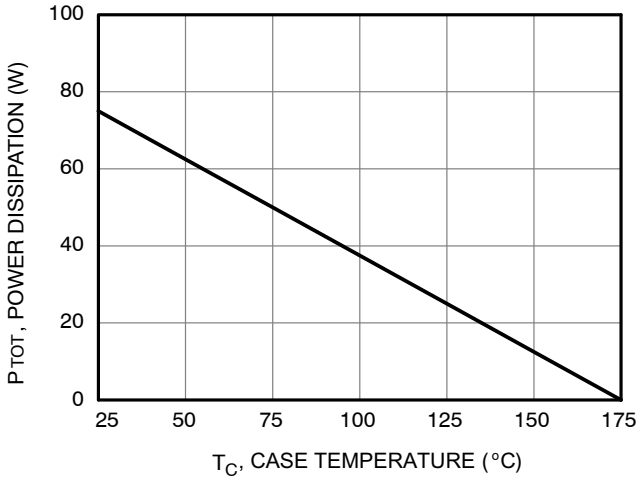


Figure 4. Power Derating

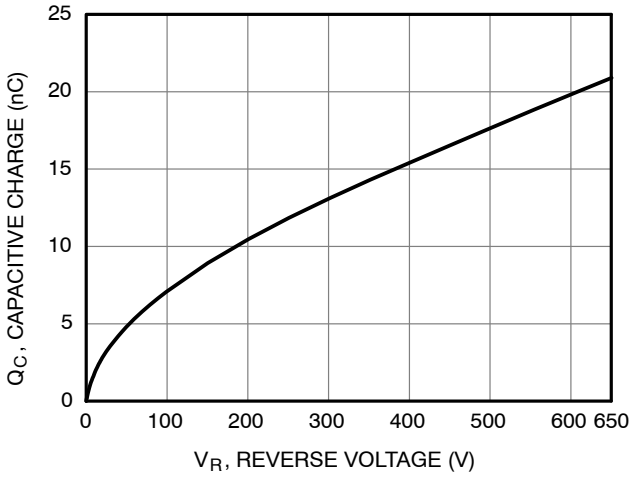


Figure 5. Capacitive Charge vs. Reverse Voltage

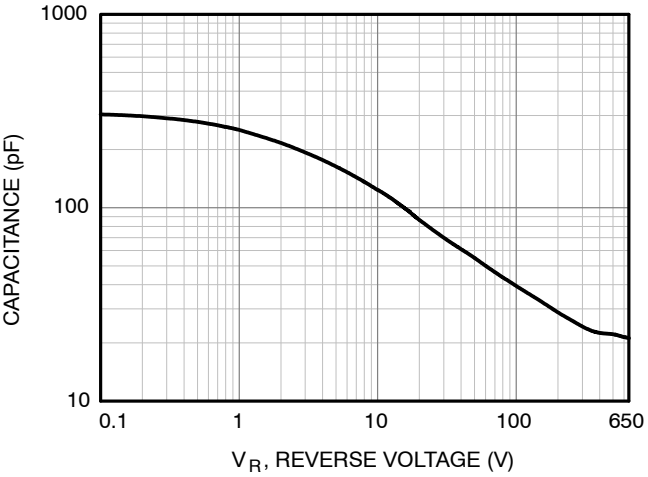


Figure 6. Capacitance vs. Reverse Voltage

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TYPICAL CHARACTERISTICS(CONTINUED)

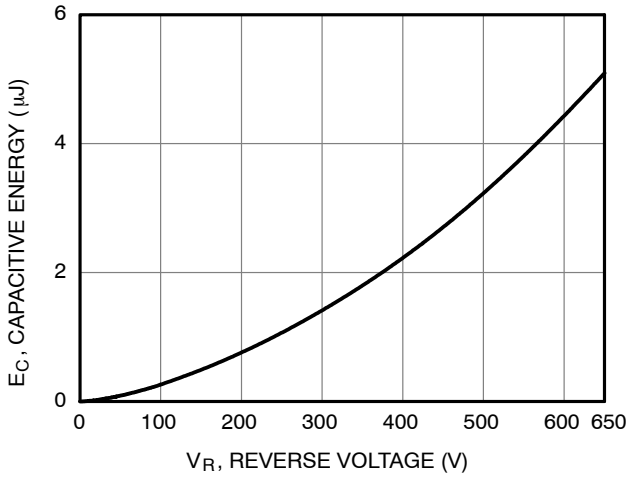


Figure 7. Capacitance Stored Energy

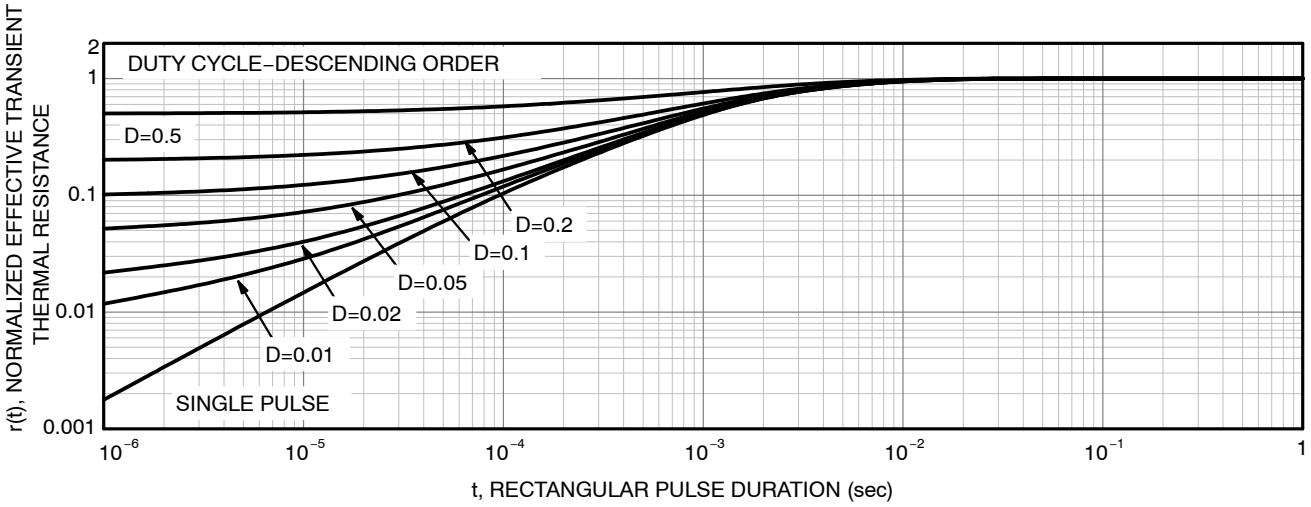
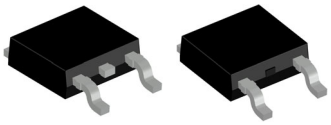


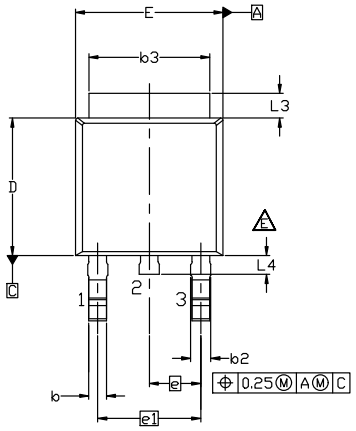
Figure 8. Junction−to−Case Transient Thermal Response

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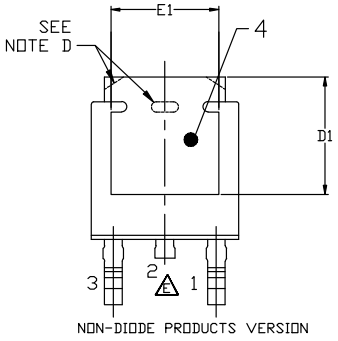


DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

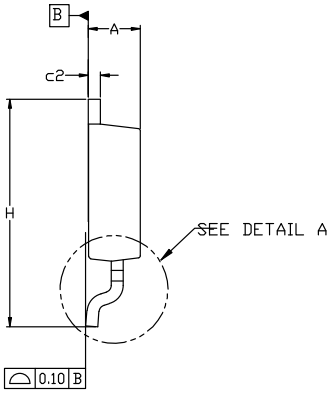
DATE 20 DEC 2023



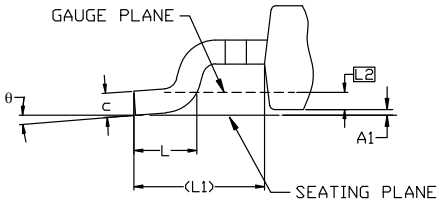
NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION

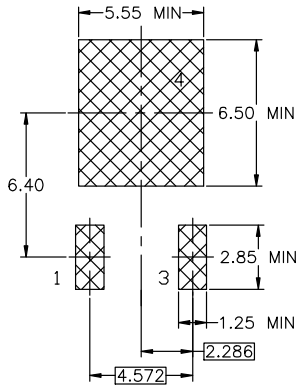


NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

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