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Continuity of ordering part numbers

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2-Mbit (128K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

- AEC-Q100 qualified
- High speed
  - t_{AA} = 10 ns; 12 ns
- Temperature range
  - Automotive-A: –40 °C to 85 °C
  - Automotive-E: –40 °C to 125 °C
- Embedded error-correcting code (ECC) for single-bit error correction[1, 2]
- Low active and standby current
  - Active current, I_{CC} = 40-mA typical (Automotive-E)
  - Standby current, I_{SB2} = 6-mA typical (Automotive-E)
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

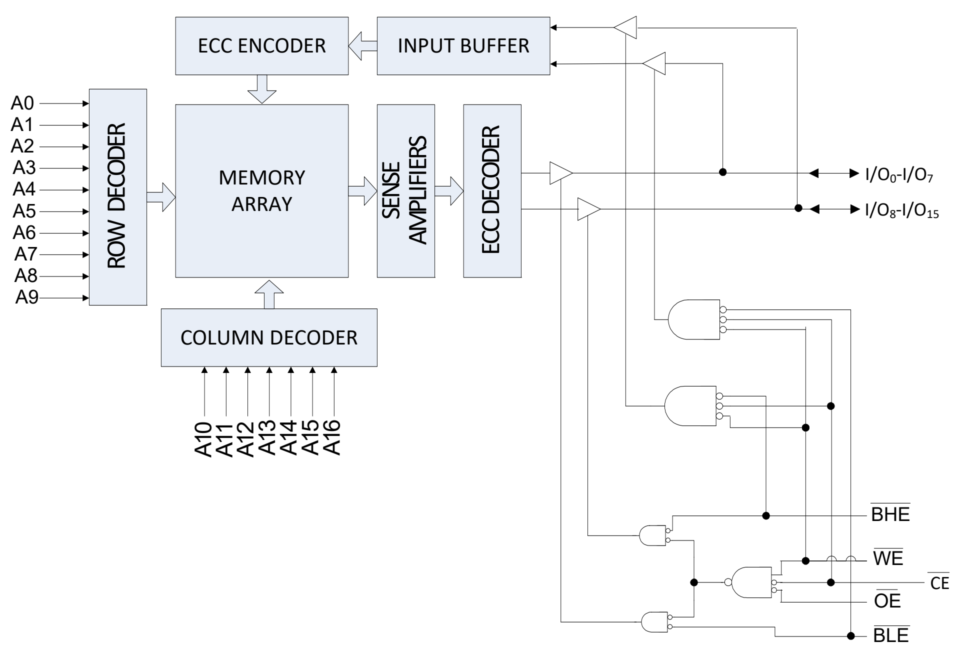
CY7C1011G is a high-performance CMOS fast static RAM automotive part with embedded ECC. This device has a single Chip Enable ($\overline{CE}$) input, and is accessed by asserting it LOW.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{16}) pins. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. You can access read data on the I/O lines (I/O_0 through I/O_{15}). To perform byte access, assert the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ LOW), or when the control signals are deasserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

Logic Block Diagram – CY7C1011G



Notes
1. This device does not support automatic write-back on error detection.
2. SER Rate < 0.1 FIT/Mb. Refer to AN88889 for details.

Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout[3]

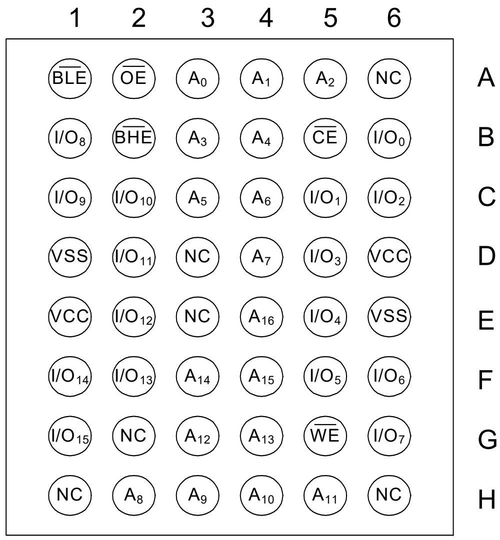
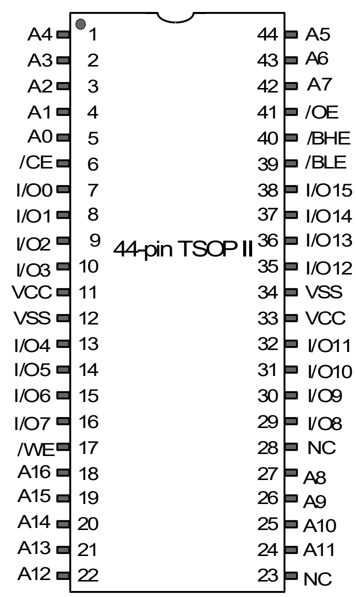


Figure 2. 44-pin TSOP II pinout [3]



Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
				Typ[4]	Max	Typ[4]	Max
CY7C1011G30	Automotive-E	2.2 V–3.6 V	10, 12	40	50	6	14
	Automotive-A		10	38	45	6	8

Notes
3. NC pins are not connected internally to the die.
4. Typical values are included for reference only and are not guaranteed or tested.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND[5] .... –0.5 V to V_{CC} + 0.3 V

DC voltage applied to outputs in HI-Z State[5] .... –0.3 V to V_{CC} + 0.3 V

DC input voltage[5] .... –0.3 V to V_{CC} + 0.3 V

Current into outputs (in low state) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V
Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions	10 ns (Automotive-A)			10 ns/ 12ns (Automotive-E)			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA	2	–	–	2	–	–	V
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.2	–	–	2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA	–	–	0.4	–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–	2	–	V_{CC} + 0.3[5]	2	–	V_{CC} + 0.3[5]	V
		2.7 V to 3.6 V	–	2	–	V_{CC} + 0.3[5]	2	–	V_{CC} + 0.3[5]	
V_{IL}	Input LOW voltage	2.2 V to 2.7 V	–	–0.3[5]	–	0.6	–0.3[5]	–	0.6	V
		2.7 V to 3.6 V	–	–0.3[5]	–	0.8	–0.3[5]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}	–1	–	+1	–5	–	+5	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	–	+1	–5	–	+5	µA
I_{CC}	Operating supply current		V_{CC} = 3.6 V, I_{OUT} = 0 mA, CMOS levels; f = f_{MAX} = $1/t_{RC}$	–	38	45	–	40	50	mA
I_{SB1}	Automatic CE power down current – TTL inputs		V_{CC} = 3.6 V, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	–	15	–	–	24	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		V_{CC} = 3.6 V, $\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0	–	6	8	–	6	14	mA

Note

5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

Capacitance

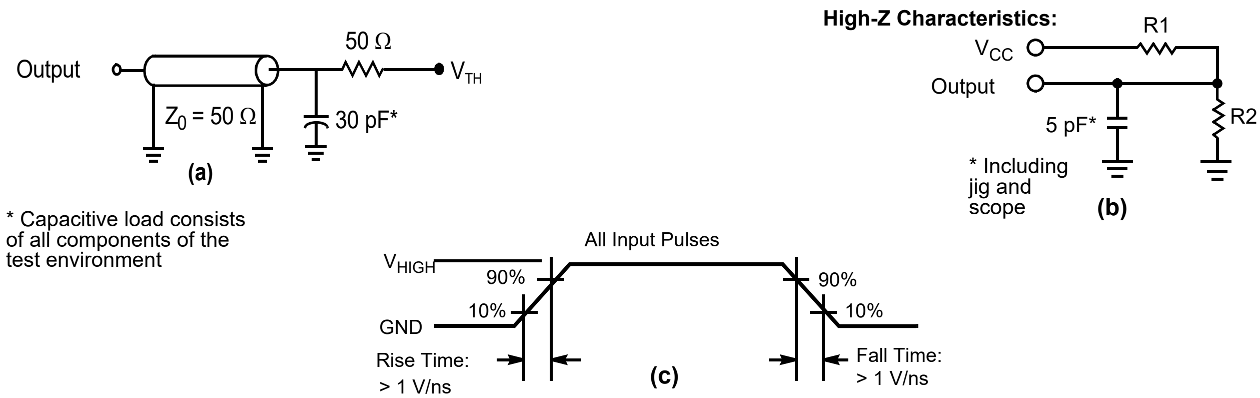
Parameter [6]	Description	Test Conditions	All Packages	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	48-ball VFBGA	44-pin TSOPII	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	30.68	66.82	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.83	15.97	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes
6. Tested initially and after any design or process change that may affect these parameters.
7. Full-device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ and a 100-µs wait time after V_{CC} stabilization.

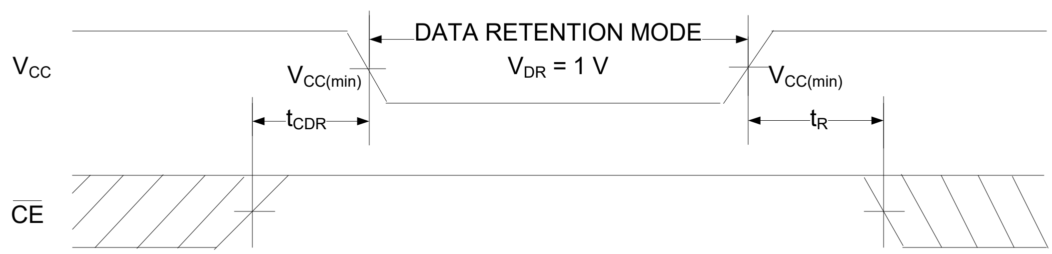
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Automotive-A		Automotive-E		Unit
			Min	Max	Min	Max	
V_{DR}	V_{CC} for data retention	–	1	–	1	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	8	–	14	mA
t_{CDR} [8]	Chip deselect to data retention time	–	0	–	0	–	ns
t_R [8, 9]	Operation recovery time	$V_{CC} \geq 2.2$ V, t_{AA} = 10ns	10	–	10	–	ns
		$V_{CC} \geq 2.2$ V, t_{AA} = 12ns	–	–	12	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [9]



Notes
8. These parameters are guaranteed by design.
9. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

AC Switching Characteristics

Over the Operating Range

Parameter [10]	Description	10 ns (Automotive-A/ Automotive-E)		12 ns (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	12	–	ns
t_{AA}	Address to data	–	10	–	12	ns
t_{OHA}	Data	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data [11]	–	10	–	12	ns
t_{DOE}	$\overline{OE}$ LOW to data	–	4.5	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to low impedance [11, 12]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z [11, 12]	–	5	–	6	ns
t_{LZCE}	$\overline{CE}$ LOW to low impedance [11, 11, 12]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to HI-Z [11, 11, 12]	–	5	–	6	ns
t_{PU}	$\overline{CE}$ LOW to power up [11, 12]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down [11, 12]	–	10	–	12	ns
t_{DBE}	Byte enable to data valid	–	4.5	–	7	ns
t_{LZBE}	Byte enable to low impedance[12]	0	–	0	–	ns
t_{HZBE}	Byte disable to HI-Z[12]	–	6	–	6	ns
Write Cycle [13, 14]						
t_{WC}	Write cycle time	10	–	12	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [11]	7	–	8	–	ns
t_{AW}	Address setup to write end	7	–	8	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	8	–	ns
t_{SD}	Data setup to write end	5	–	6	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low impedance [11, 12]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z [11, 12]	–	5	–	6	ns
t_{BW}	Byte Enable to write end	7	–	8	–	ns

Notes

10. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 5, unless specified otherwise.
11. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady state voltage.
12. These parameters are guaranteed by design and are not tested.
13. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
14. The minimum write cycle pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1011G (Address Transition Controlled) [15, 16]

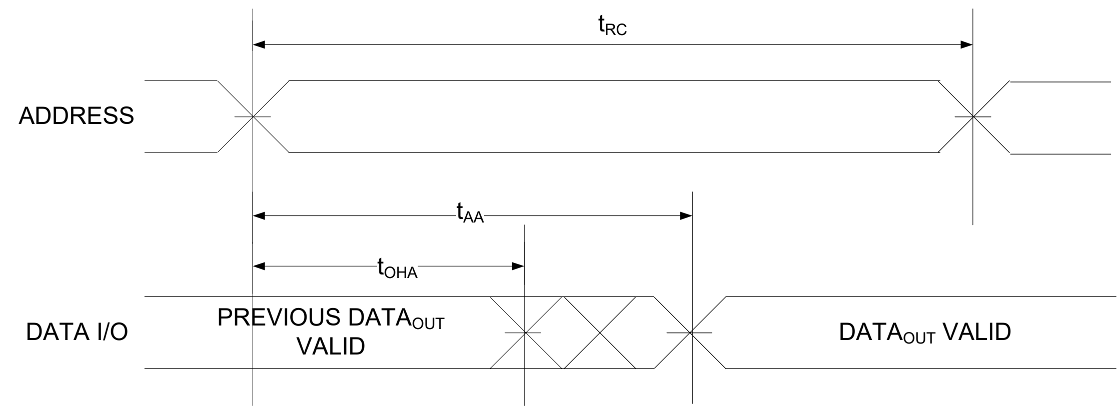
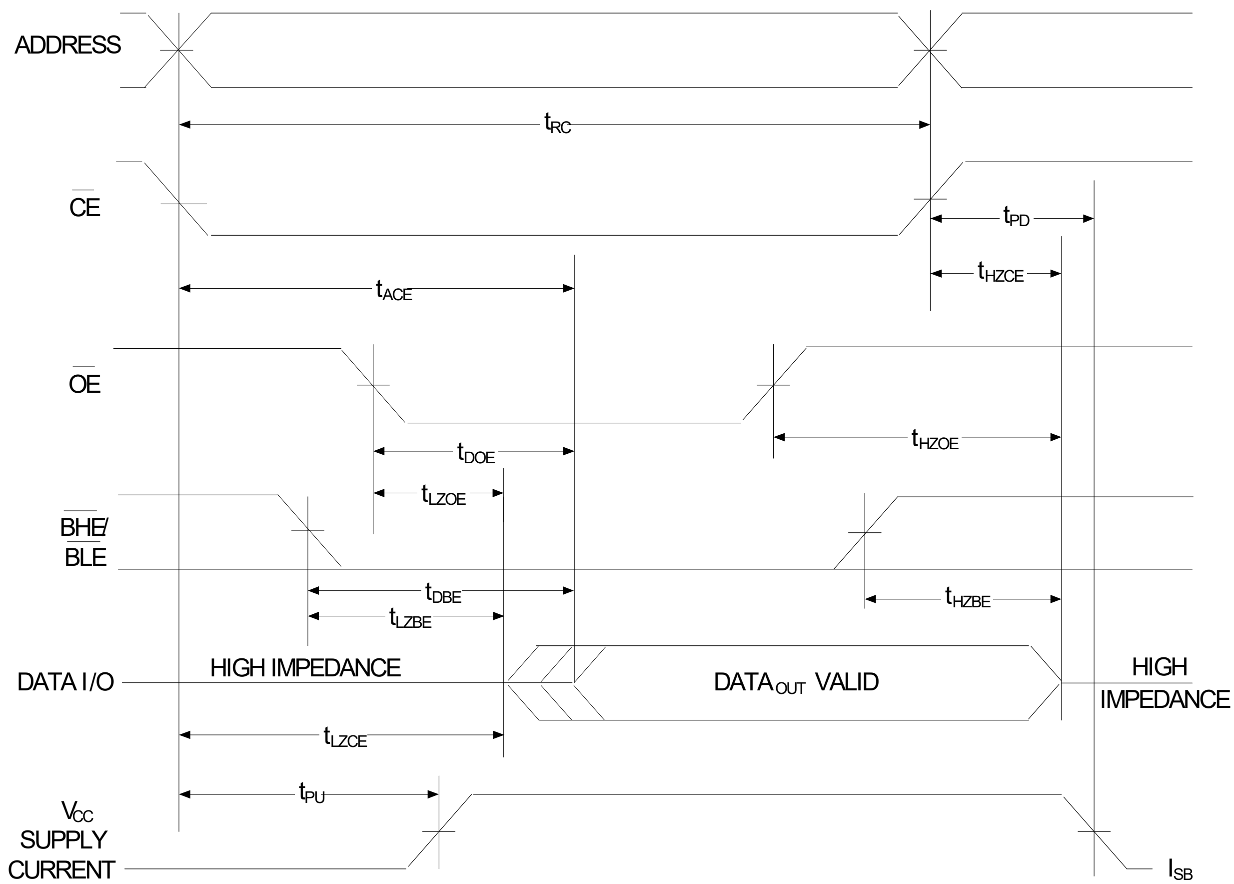


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [16]



Notes

15. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
16. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18, 19]

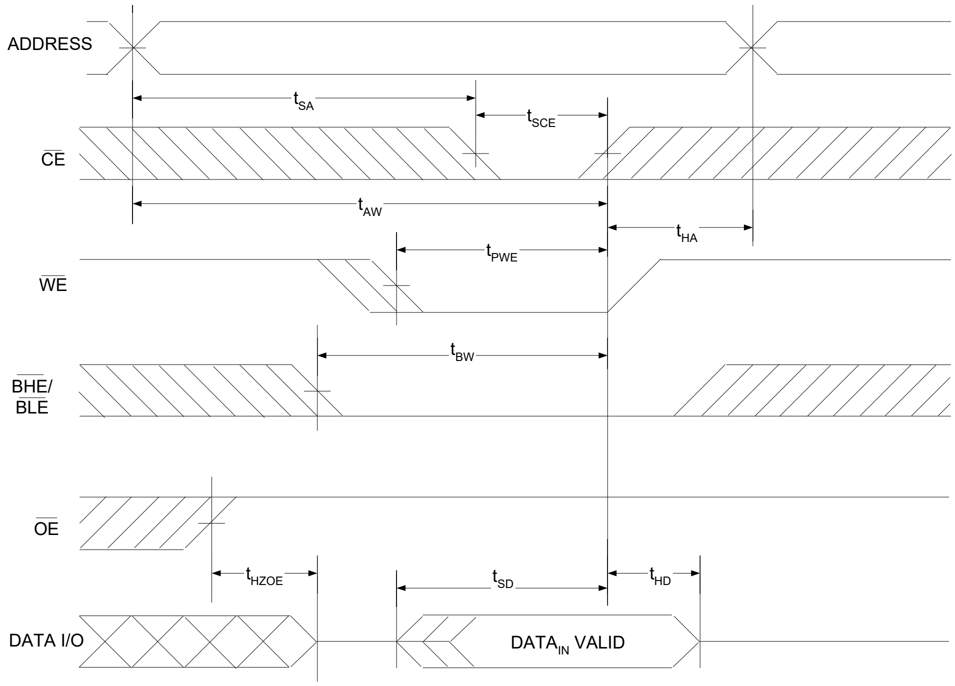
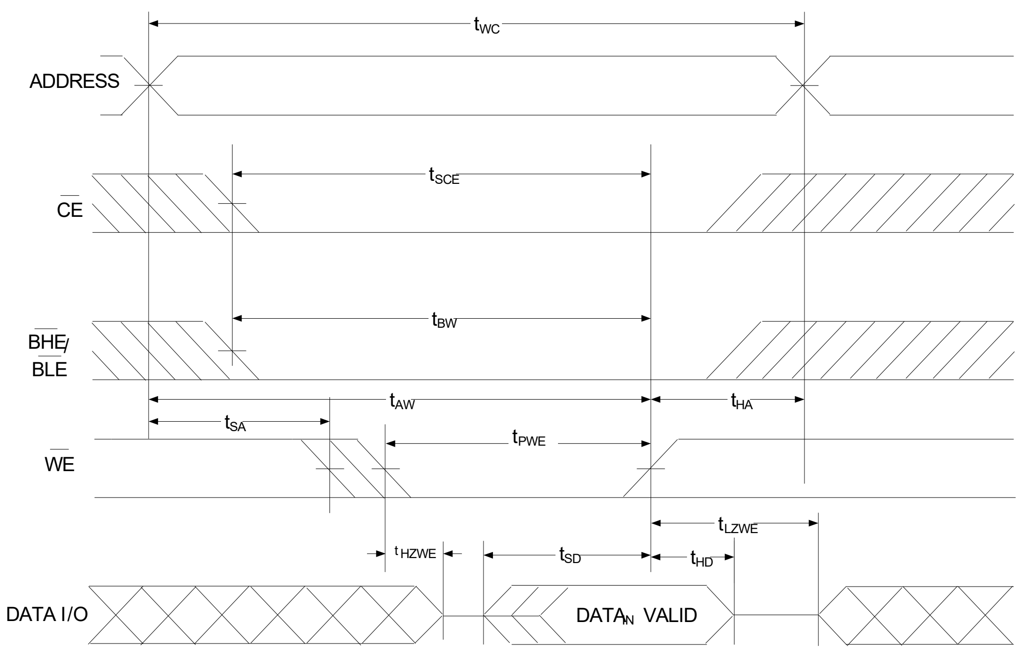


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17, 18, 19, 20]



Notes

17. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
18. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
20. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [21, 22]

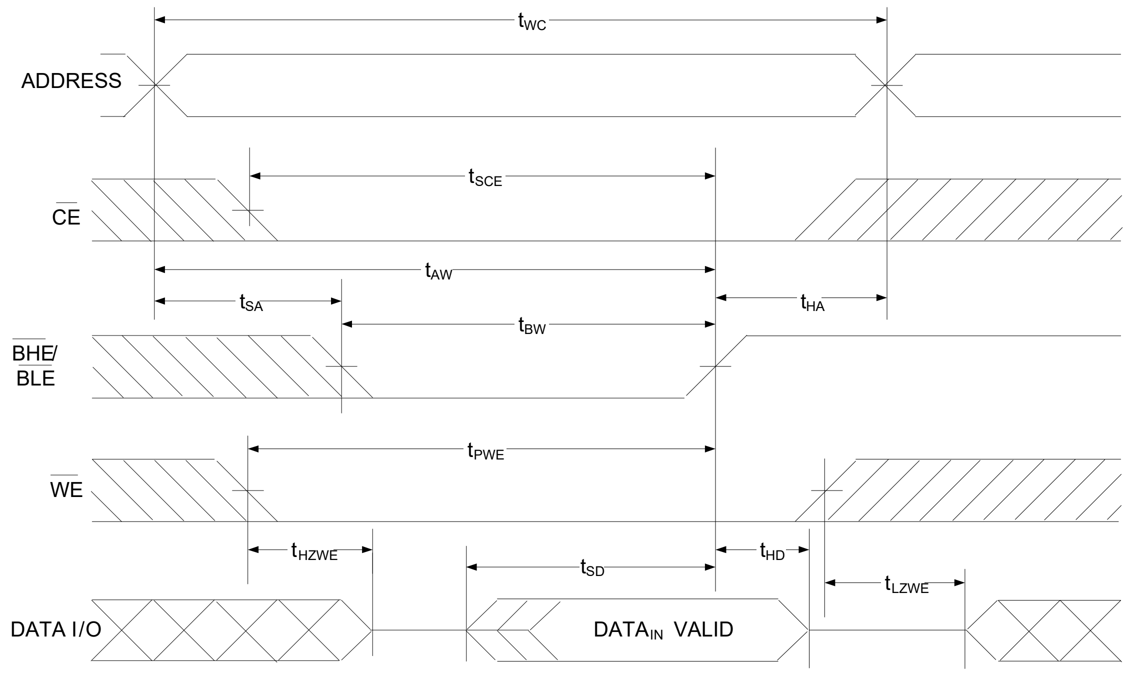
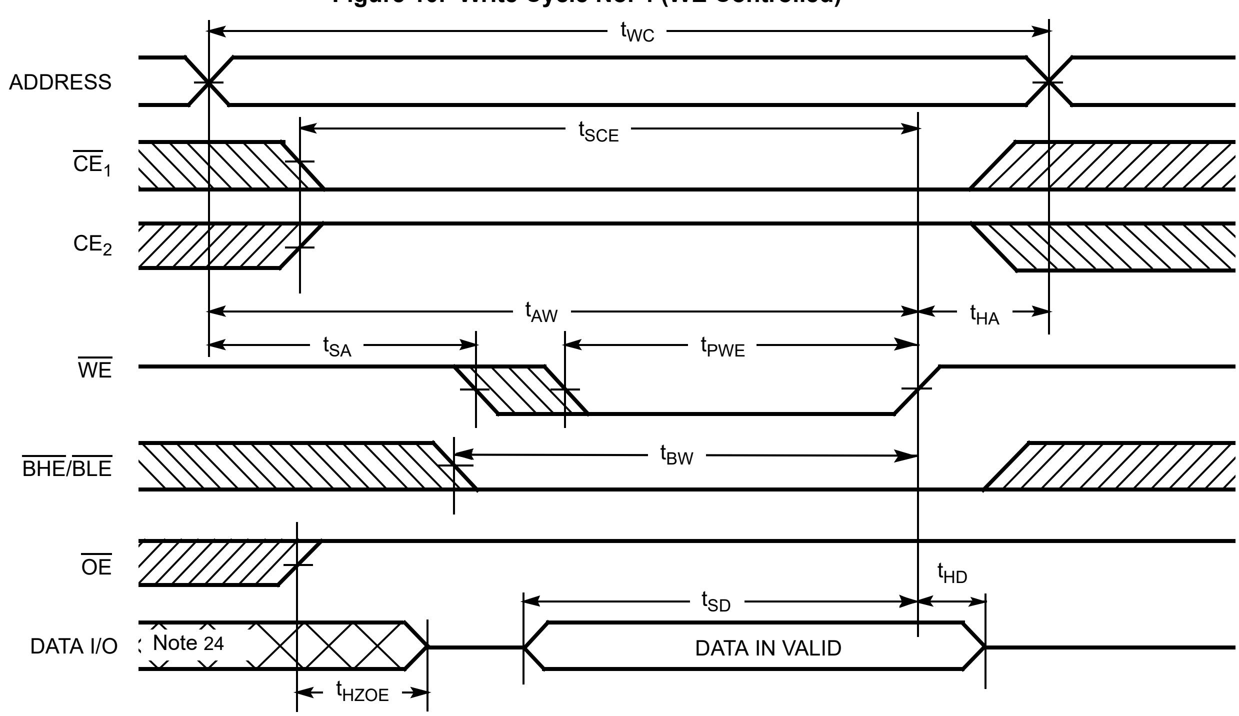


Figure 10. Write Cycle No. 4 ($\overline{WE}$ Controlled) [21, 22, 23]



Notes

21. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
24. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	HI-Z	HI-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Voltage Range	Package Diagram	Package Type (All Pb-free)	Operating Range
10	CY7C1011G30-10ZSXA	2.2 V–3.6 V	51-85087	44-pin TSOP II	Automotive-A
	CY7C1011G30-10ZSXAT	2.2 V–3.6 V	51-85087	44-pin TSOP II, Tape & Reel	Automotive-A
	CY7C1011G30-10BAJXE	2.2 V–3.6 V	001-85259	48-ball VFBGA	Automotive-E
	CY7C1011G30-10BAJXET	2.2 V–3.6 V	001-85259	48-ball VFBGA, Tape & Reel	Automotive-E
12	CY7C1011G30-12ZSXE	2.2 V–3.6 V	51-85087	44-pin TSOP II	Automotive-E
	CY7C1011G30-12ZSXET	2.2 V–3.6 V	51-85087	44-pin TSOP II, Tape & Reel	Automotive-E

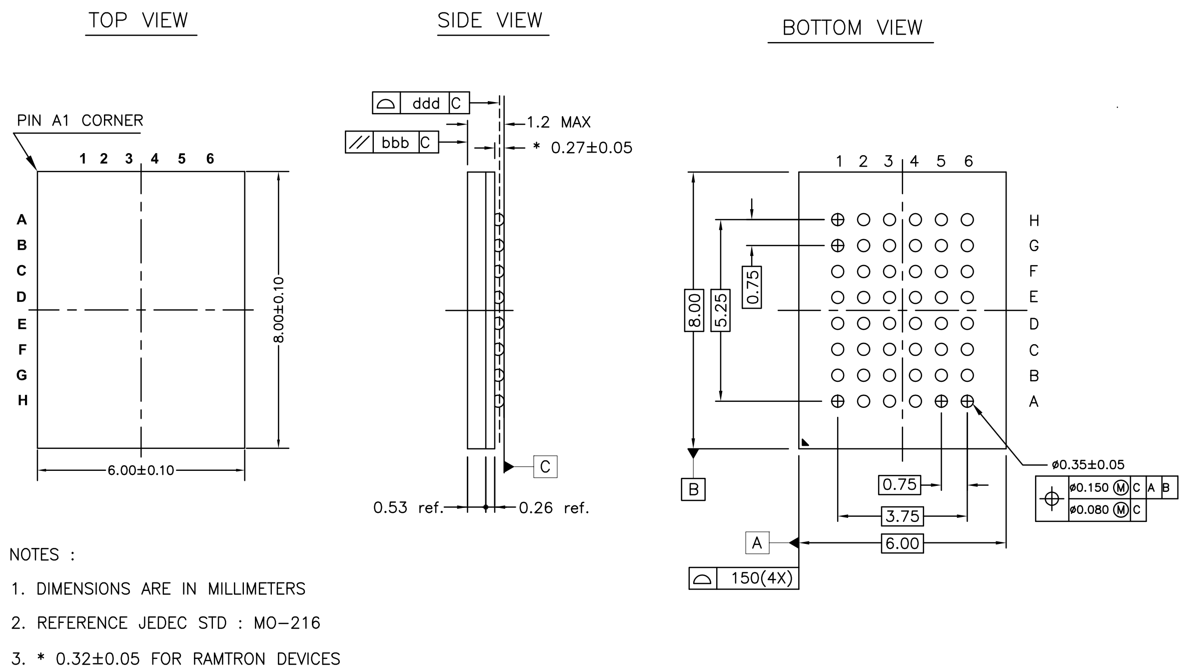
Ordering Code Definitions

CY 7 C 1 04 1 G 30 - XX XX J X X X

- X = blank or T
  blank = Bulk; T = Tape and Reel
- Temperature Range: X = A or E
  A = Automotive-A; E = Automotive-E
- Pb-free
- J = JEDEC Compliant (only for BGA package)
- Package Type: XX = BA or ZS
  BA = 48-ball VFBGA; ZS = 44-pin TSOP II
- Speed: XX = 10 ns or 12 ns
- Voltage Range: 30 = 2.2 V–3.6 V
- Process Technology: Revision Code “G” = 65 nm Technology
- Data Width: 1 = × 16-bits
- Density: 04 = 4-Mbit
- Family Code: 1 = Fast Asynchronous SRAM family
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

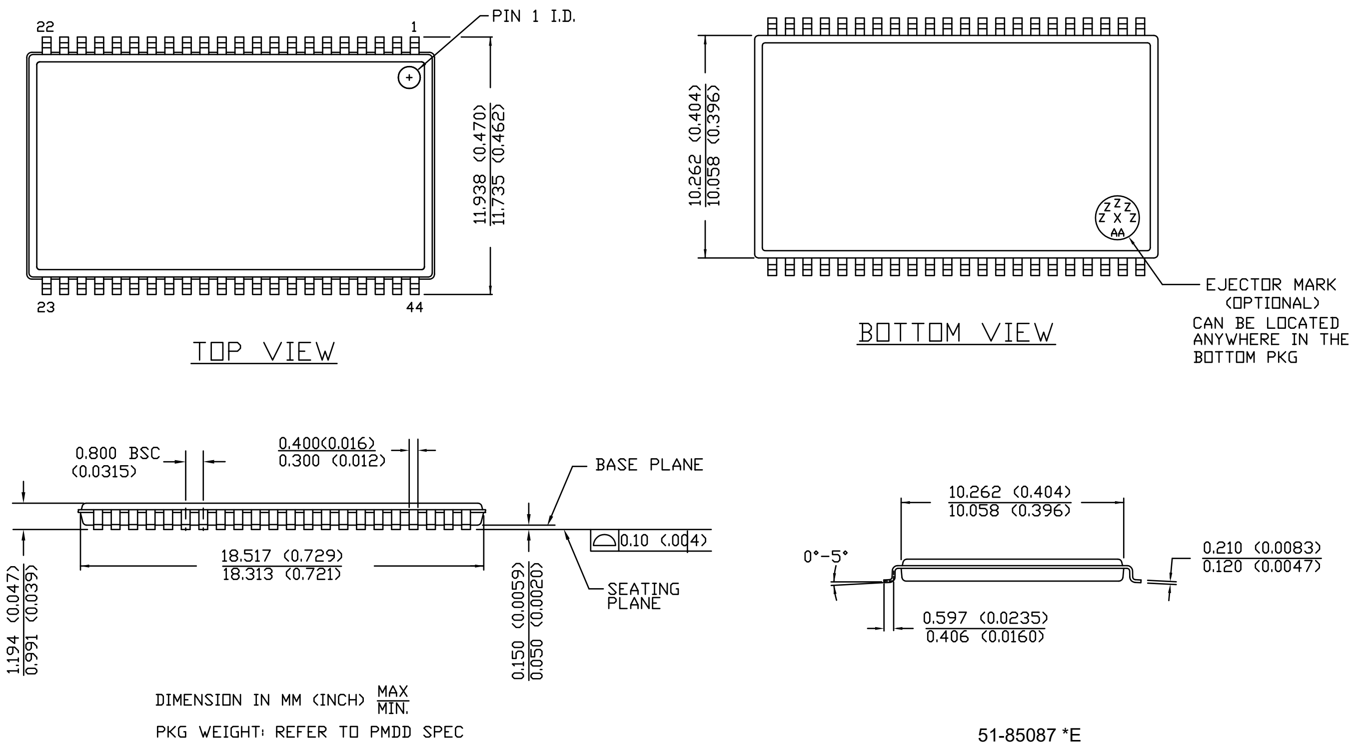
Figure 11. 48-ball VFBGA ((6 × 8 × 1.2 mm) 0.35 mm Ball Diameter) Package Outline, 001-85259



001-85259 *A

Package Diagrams (continued)

Figure 12. 44-pin TSOP II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1011G Automotive, 2-Mbit (128K words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95423				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A	4998910	NILE	11/02/2015	Changed status from Preliminary to Final.
*B	5024020	NILE	11/23/2015	Updated Ordering Information: Updated part numbers.
*C	5692050	NILE	04/27/2017	Added 12 ns speed bin related information in all instances across the document. Updated Features: Added “AEC-Q100 qualified”. Updated DC Electrical Characteristics: Removed details of V_{OH} parameter corresponding to “2.7 V to 3.6 V”. Added details of V_{OH} parameter corresponding to “2.7 V to 3.0 V” and “3.0 V to 3.6 V”. Updated Note 5 (Replaced “2 ns” with “20 ns”). Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*D	5725360	NILE	05/03/2017	Updated Ordering Information: Updated part numbers.
*E	6142440	NILE	04/17/2018	Updated Features: Added Note 2 and referred the same note in “Embedded error-correcting code (ECC) for single-bit error correction”.
*F	6560693	NILE	04/29/2019	Updated to new template.

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