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**P-Channel 1.5 V Specified PowerTrench® Thin WL-CSP MOSFET**  
**-20 V, -2.6 A, 140 mΩ**
**Features**

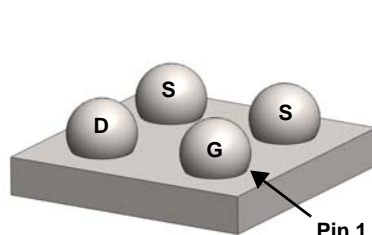
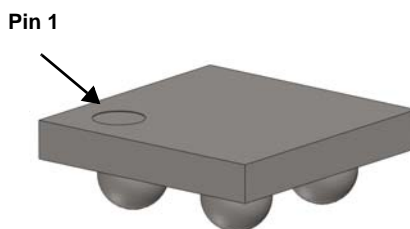
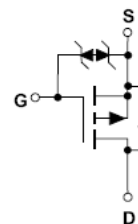
- Max  $r_{DS(on)}$  = 140 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -2$  A
- Max  $r_{DS(on)}$  = 182 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -1.5$  A
- Max  $r_{DS(on)}$  = 231 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -1$  A
- Max  $r_{DS(on)}$  = 315 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -1$  A
- Occupies only 0.64 mm<sup>2</sup> of PCB area. Less than 16% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.4 mm height when mounted to PCB
- HBM ESD protection level > 2 kV (Note3)
- RoHS Compliant


**General Description**

Designed on Fairchild's advanced 1.5 V PowerTrench® process with state of the art "fine pitch" Thin WLCSP packaging process, the FDZ661PZ minimizes both PCB space and  $r_{DS(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile (0.4 mm) and small (0.8x0.8 mm<sup>2</sup>) packaging, low gate charge, and low  $r_{DS(on)}$ .

**Applications**

- Battery management
- Load switch
- Battery protection


**BOTTOM**

**TOP**

**WL-CSP 0.8X0.8 Thin**
**MOSFET Maximum Ratings**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	-2.6	A
	-Pulsed	-10	
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	1.3	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	0.4	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

**Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	93	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	311	

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
EH	FDZ661PZ	WL-CSP 0.8X0.8 Thin	7 "	8 mm	5000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\ \text{V}$ , $V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\ \text{V}$ , $V_{DS} = 0\ \text{V}$			$\pm 6$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\ \mu\text{A}$	-0.3	-0.7	-1.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		2.5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\ \text{V}$ , $I_D = -2\ \text{A}$		108	140	m $\Omega$
		$V_{GS} = -2.5\ \text{V}$ , $I_D = -1.5\ \text{A}$		129	182	
		$V_{GS} = -1.8\ \text{V}$ , $I_D = -1\ \text{A}$		159	231	
		$V_{GS} = -1.5\ \text{V}$ , $I_D = -1\ \text{A}$		201	315	
		$V_{GS} = -4.5\ \text{V}$ , $I_D = -2\ \text{A}$ , $T_J = 125^\circ\text{C}$		143	204	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\ \text{V}$ , $I_D = -2\ \text{A}$		7.8		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$		416	555	pF
$C_{oss}$	Output Capacitance			61	80	pF
$C_{rss}$	Reverse Transfer Capacitance			53	70	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\ \text{V}$ , $I_D = -2.5\ \text{A}$ , $V_{GS} = -4.5\ \text{V}$ , $R_{GEN} = 6\ \Omega$		4.9	10	ns
$t_r$	Rise Time			6.3	13	ns
$t_{d(off)}$	Turn-Off Delay Time			68	108	ns
$t_f$	Fall Time			33	52	ns
$Q_g$	Total Gate Charge	$V_{GS} = -4.5\ \text{V}$ , $V_{DD} = -10\ \text{V}$ , $I_D = -2.5\ \text{A}$		6.3	8.8	nC
$Q_{gs}$	Gate to Source Charge			0.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.7		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = -1.4\ \text{A}$ (Note 2)		-0.9	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -2.5\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$		29	46	ns
$Q_{rr}$	Reverse Recovery Charge			10	18	nC

**Notes:**

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 93  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 311  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

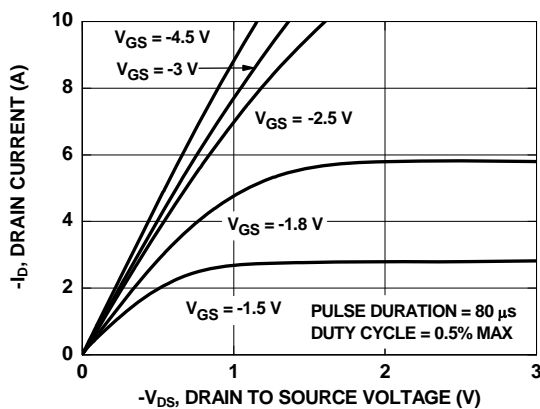


Figure 1. On-Region Characteristics

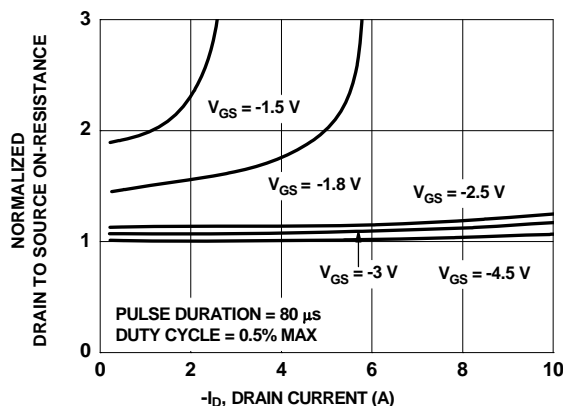


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

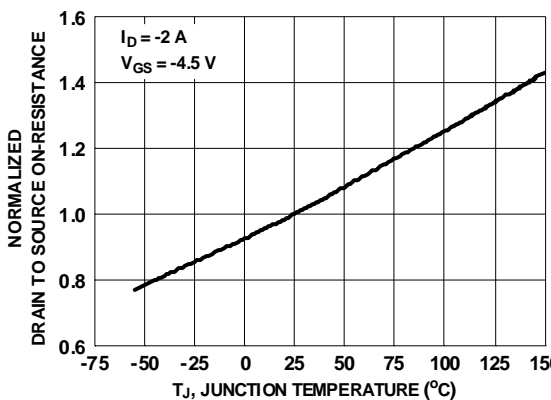


Figure 3. Normalized On-Resistance vs Junction Temperature

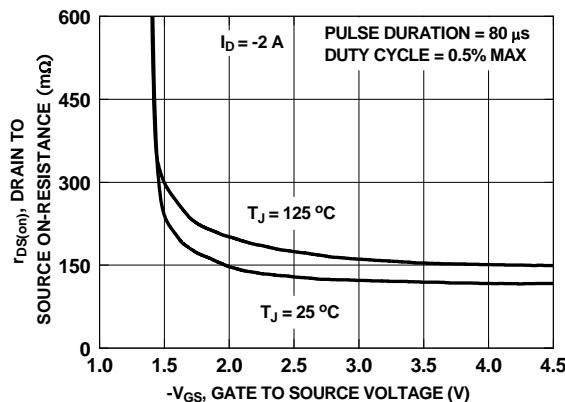


Figure 4. On-Resistance vs Gate to Source Voltage

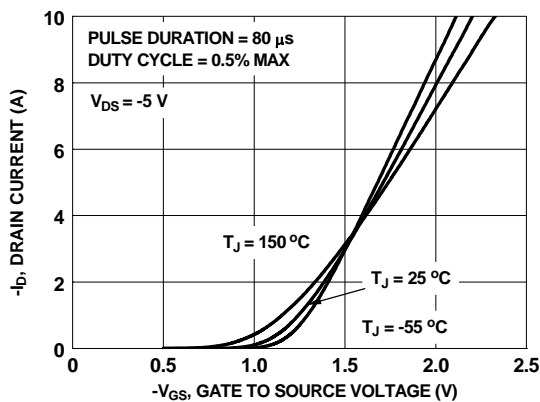


Figure 5. Transfer Characteristics

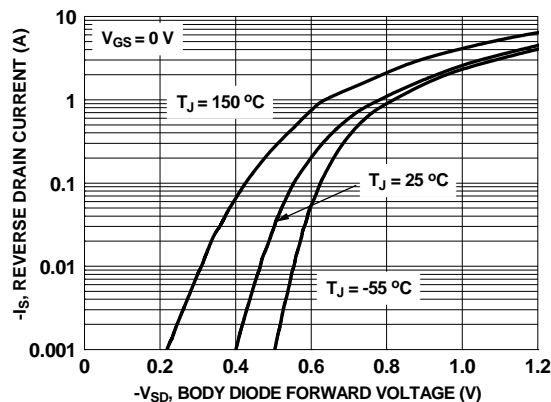


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

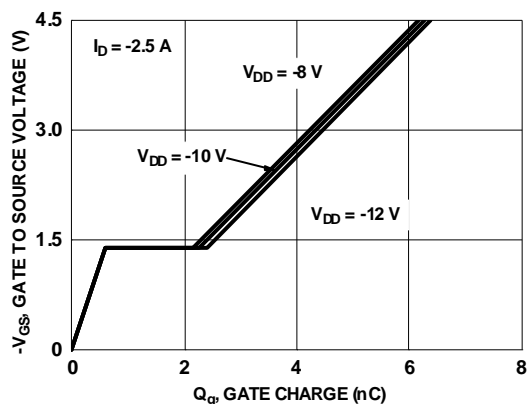


Figure 7. Gate Charge Characteristics

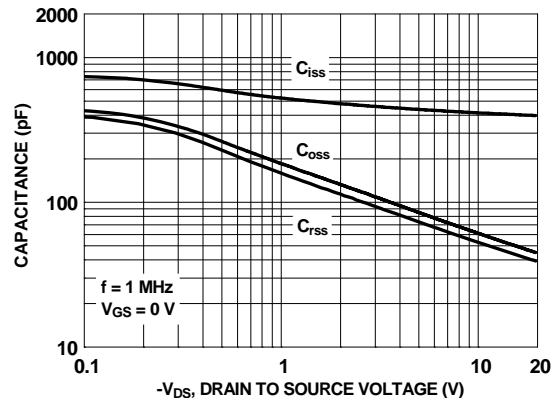


Figure 8. Capacitance vs Drain to Source Voltage

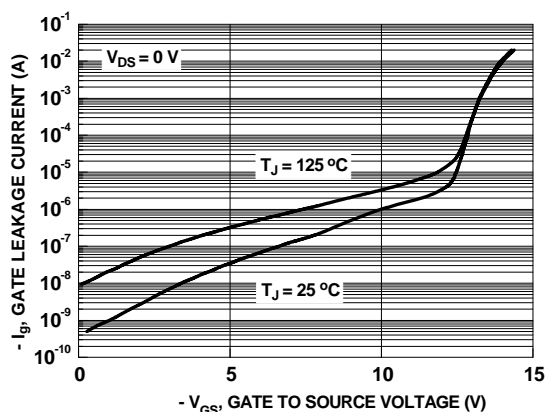


Figure 9. Gate Leakage Current vs Gate to Source Voltage

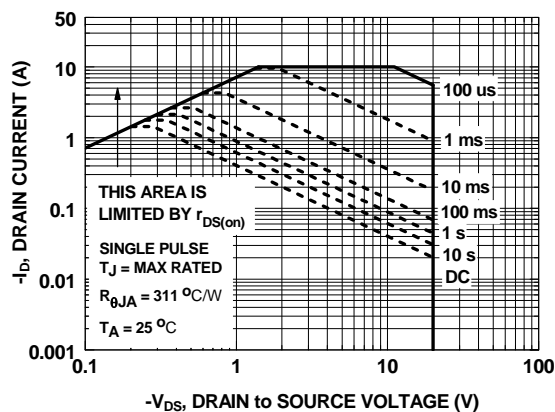


Figure 10. Forward Bias Safe Operating Area

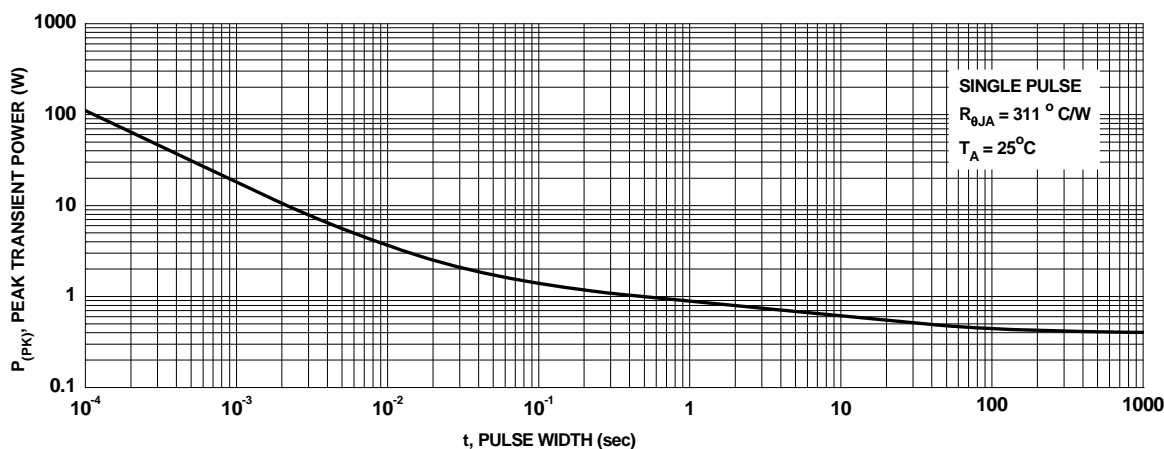
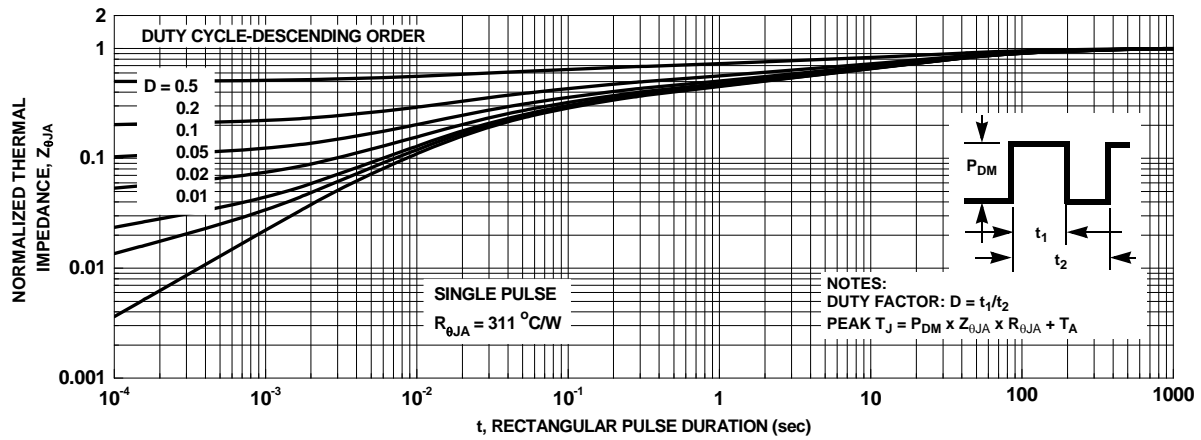


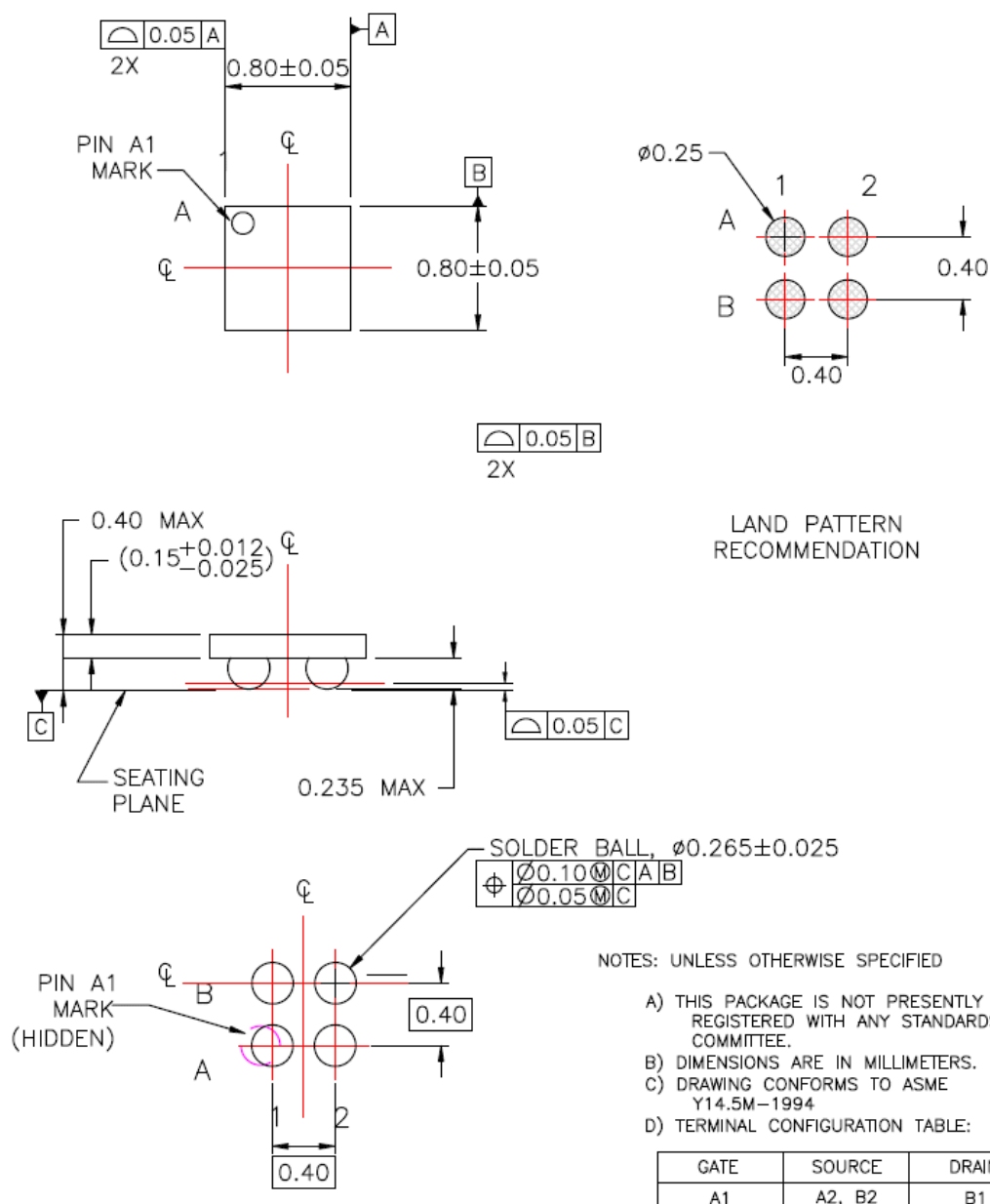
Figure 11. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout







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