

PTMC210124MD

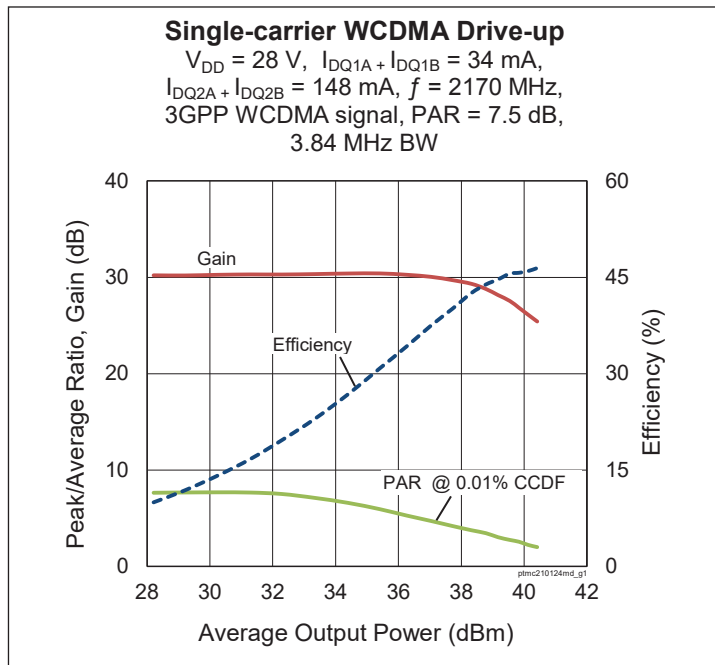
Wideband LDMOS Two-stage Integrated Power Amplifier 12 W, 28 V, 1805 – 2200 MHz

Description

The PTMC210124MD is a wideband, two-stage, LDMOS integrated power amplifier. It incorporates internal matching for operation from 1805 MHz to 2200 MHz, and dual independent outputs with 6 W of output power each. It is available in a 14-lead plastic overmold package with gull wing leads.



PTMC210124MD
Package PG-HB1DSO-14-1
(formed leads)



Features

- On-chip matching for broadband operation
- Typical CW performance, 2170 MHz, 28 V, combined outputs
 - Output power at $P_{1dB} = 12\text{ W}$
 - Gain = 30.5 dB
 - Efficiency = 51.9%
- Capable of handling 10:1 VSWR @ 28 V, 12 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 0B (per ANSI/ESDA/JEDEC JS-001)
- Integrated temperature compensation
- Pb-free and RoHS-compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed production test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1A} = I_{DQ1B} = 17\text{ mA}$, $I_{DQ2A} = I_{DQ2B} = 73\text{ mA}$, $P_{OUT} = 1.38\text{ W avg}$, $f = 2170\text{ MHz}$, 3GPP WCDMA signal, channel bandwidth = 3.84 MHz, peak/average = 7.5 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	29	30.5	—	dB
Drain Efficiency	η_D	15	16.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-49.5	-47	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Stage 1	Conditions	Symbol	Min	Typ	Max	Unit
Drain Leakage Current	$V_{DS} = 28\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	—	—	0.1	μA
	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1	μA
Gate Leakage Current	$V_{GS} = 1\text{ V}, V_{DS} = 0\text{ V}$	I_{GSS}	—	—	0.1	μA
On-state Resistance	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	10	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}, I_{DQ1A} = I_{DQ1B} = 17\text{ mA}$	V_{GS1}	—	2.7	—	V
Fixture Operating Gate Voltage	$V_{DS} = 28\text{ V}, I_{DQ1A} = I_{DQ1B} = 17\text{ mA}$	V_{GS1}	—	4.9	—	V

Stage 2	Conditions	Symbol	Min	Typ	Max	Unit
Drain Leakage Current	$V_{DS} = 28\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	—	—	0.1	μA
	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1	μA
Gate Leakage Current	$V_{GS} = 1\text{ V}, V_{DS} = 0\text{ V}$	I_{GSS}	—	—	0.1	μA
On-state Resistance	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	1.9	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}, I_{DQ2A} = I_{DQ2B} = 73\text{ mA}$	V_{GS2}	—	2.7	—	V
Fixture Opererating Gate Voltage	$V_{DS} = 28\text{ V}, I_{DQ2A} = I_{DQ2B} = 73\text{ mA}$	V_{GS2}	—	4.9	—	V

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	−6 to +10	V
Junction Temperature	T_J	225	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−65 to +150	$^{\circ}\text{C}$
Operating Voltage	V_{DD}	0 to 32	V

Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Stage 1	$R_{\theta JC}$	4.8	$^{\circ}\text{C/W}$
Thermal Resistance Stage 2	$R_{\theta JC}$	1.9	$^{\circ}\text{C/W}$



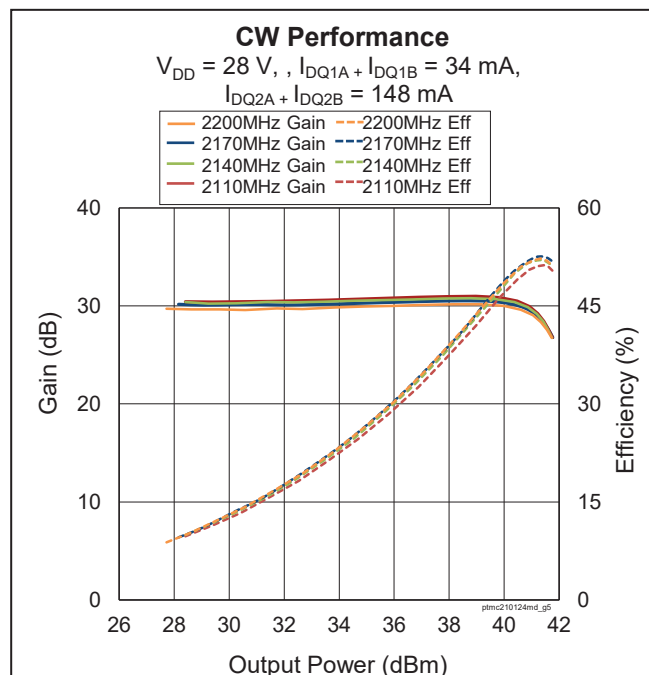
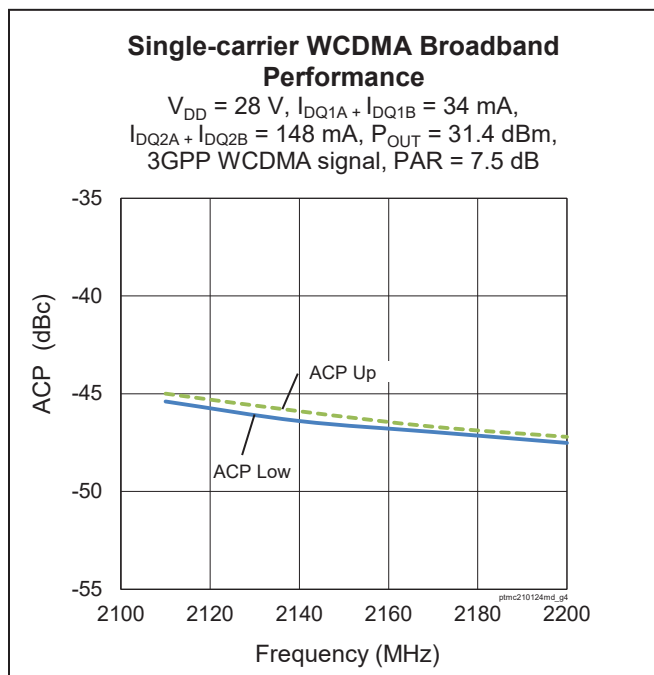
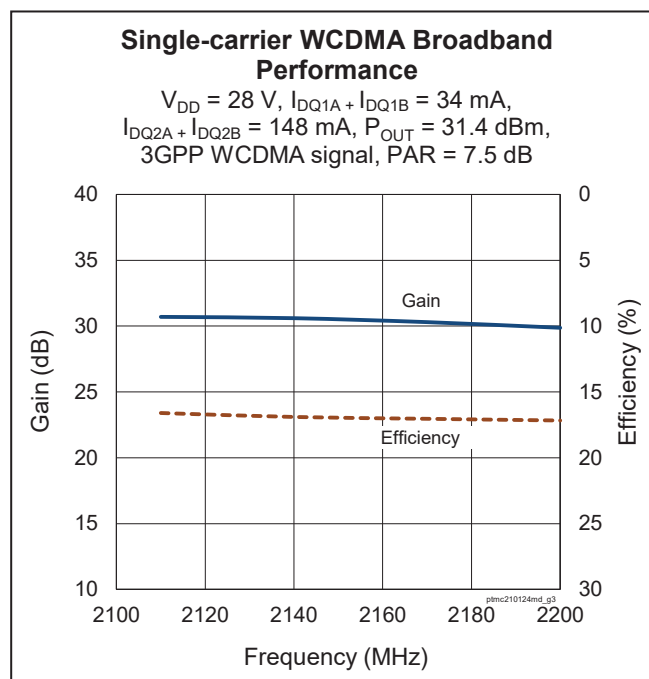
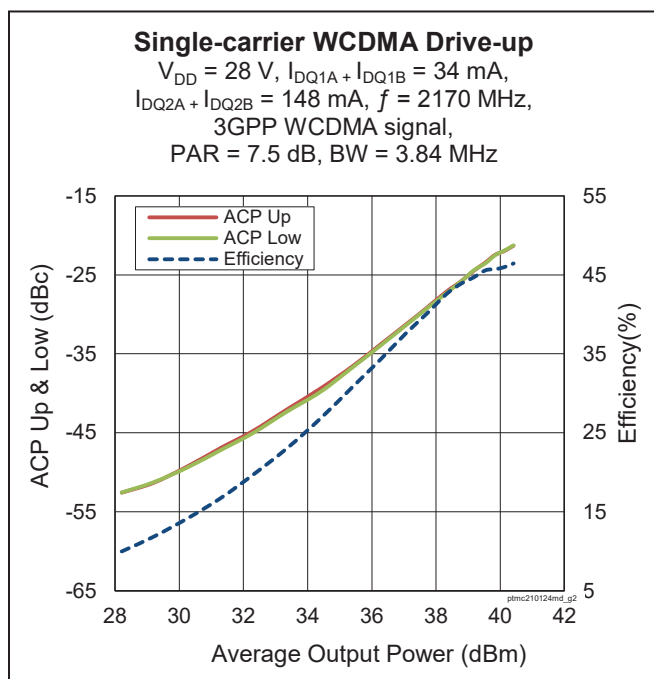
Moisture Sensitivity Level

Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

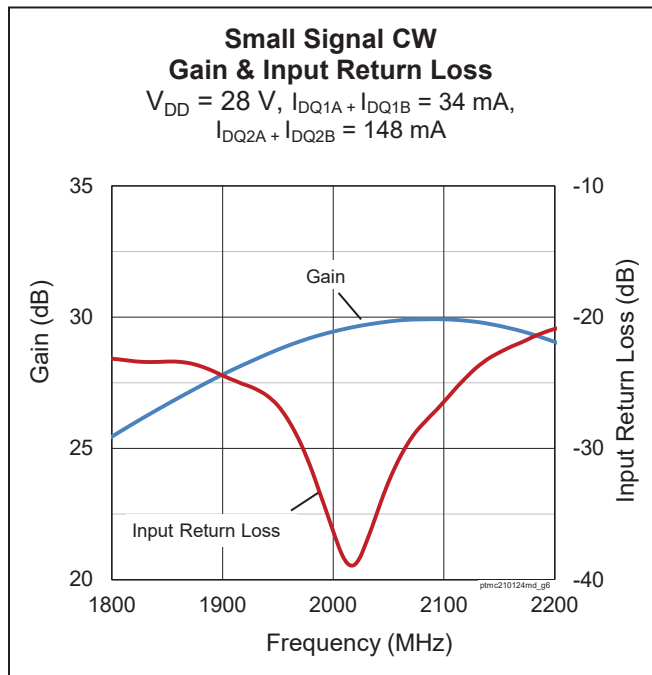
Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTMC210124MD V1 R5	PTMC210124MD-V1-R5	PG-HB1DSO-14-1	Tape & Reel, 500 pcs

Typical Performance (data taken in production test fixture)



Typical Performance (cont.)

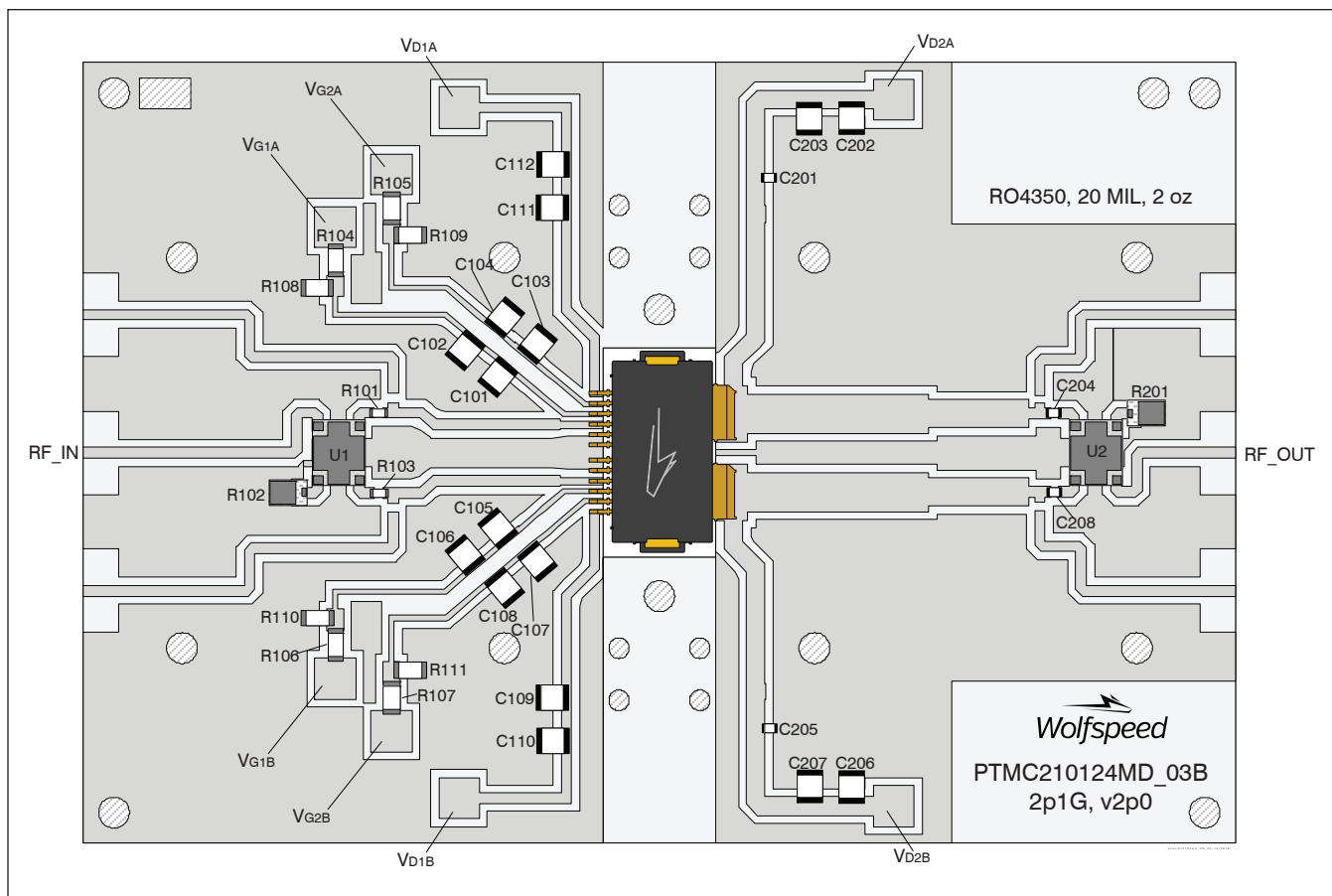


Load Pull Performance

CW signal: $V_{DD} = 28\text{ V}$, $I_{DQ1A} = I_{DQ1B} = 17\text{ mA}$, $I_{DQ2A} = I_{DQ2B} = 74\text{ mA}$

Freq [MHz]	Z_s [Ω]	P_{1dB}									
		Max Output Power					Max PAE				
		Z_L [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	PAE [%]	Z_L [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	PAE [%]
1805	49.8+j2.25	28.5+j0.97	29.2	39.5	9.0	53.4	36.1+j19.6	30.6	38.4	6.9	58.8
1960	49.9-j0.12	24.0+j4.31	30.1	39.4	8.6	53.4	21.8+j16.3	31.3	38.5	7.1	58.4
2180	48.5-j1.88	19.5+j3.58	29.0	39.5	8.9	51.5	12.0+j13.7	30.7	38.0	6.3	58.4
2200	49.3+j1.0	18.7+j4.81	29.0	39.5	8.9	53.6	12.3+j12.4	30.3	38.3	6.7	59.1

Reference Circuit, 2110 – 2200 MHz



Reference circuit assembly diagram (not to scale)

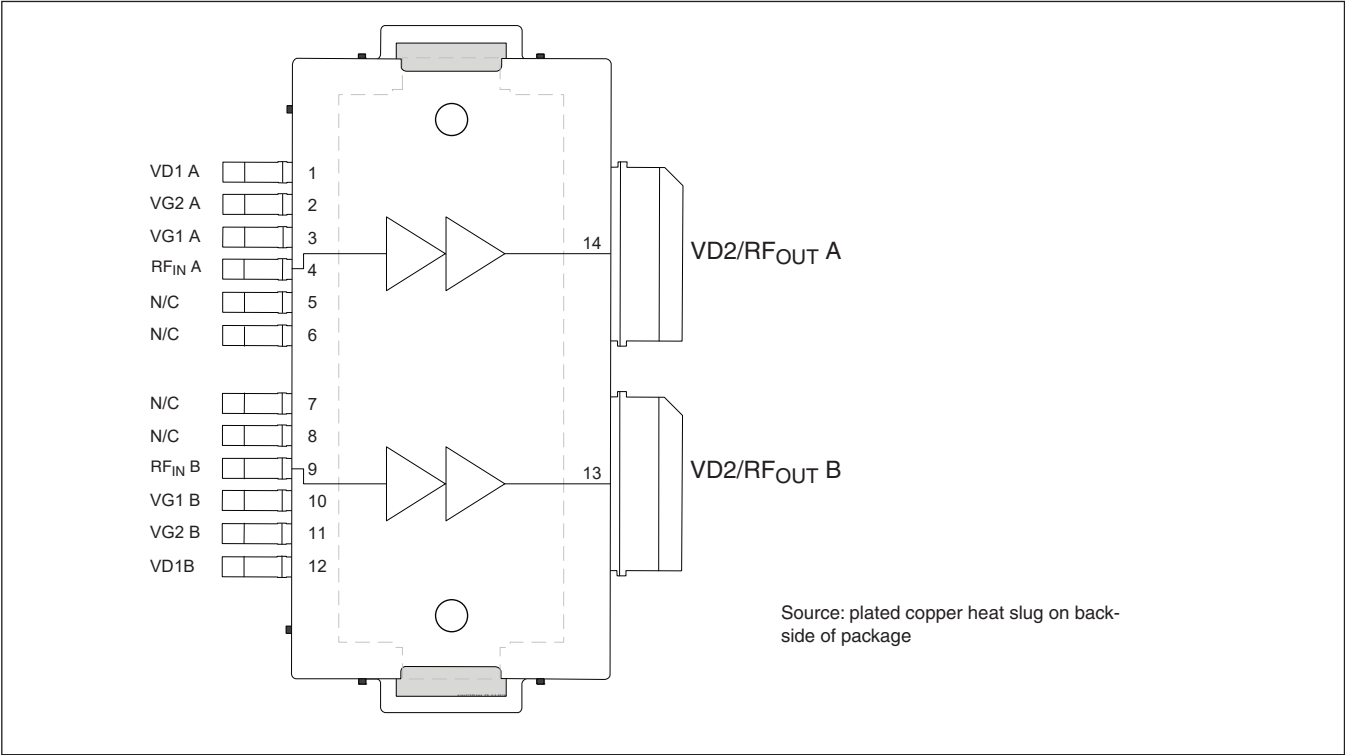
Reference Circuit Assembly

DUT	PTMC210124MD V1
Test Fixture Part No.	LTN/PTMC210124MD V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$, $f = 2110\text{--}2200$ MHz
Find Gerber files for this test fixture on the Wolfspeed Web site at www.wolfspeed.com/RF	

Components Information

Component	Description	Manufacturer	P/N
C101, C103, C105, C107, C109, C111, C203, C207	Capacitor, 4.7 μF	Murata Electronics North America	GRM32ER71H475KA88L
C102, C104, C106, C108, C110, C112, C202, C206	Capacitor, 10 μF	Taiyo Yuden	UMK325C7106MM-T
C201, C204, C205, C208	Capacitor, 10 pF	ATC	ATC800A100JT250T
R101, R103	Resistor, 0.0 ohms	Panasonic Electronic Components	ERJ-3GEY0R00V
R102, R201	Resistor, 50 ohms	Anaren	C8A50Z4A
R104, R105, R106, R107	Resistor, 1K ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
R108, R109, R110, R111	Resistor, 4.3K ohms	Panasonic Electronic Components	ERJ-8GEYJ432V
U1, U2	Hybrid coupler	Anaren	X3C21P1-03S

Pinout Diagram (top view)



Package Outline Specifications

Package PG-HB1DSO-14-1 (formed leads)

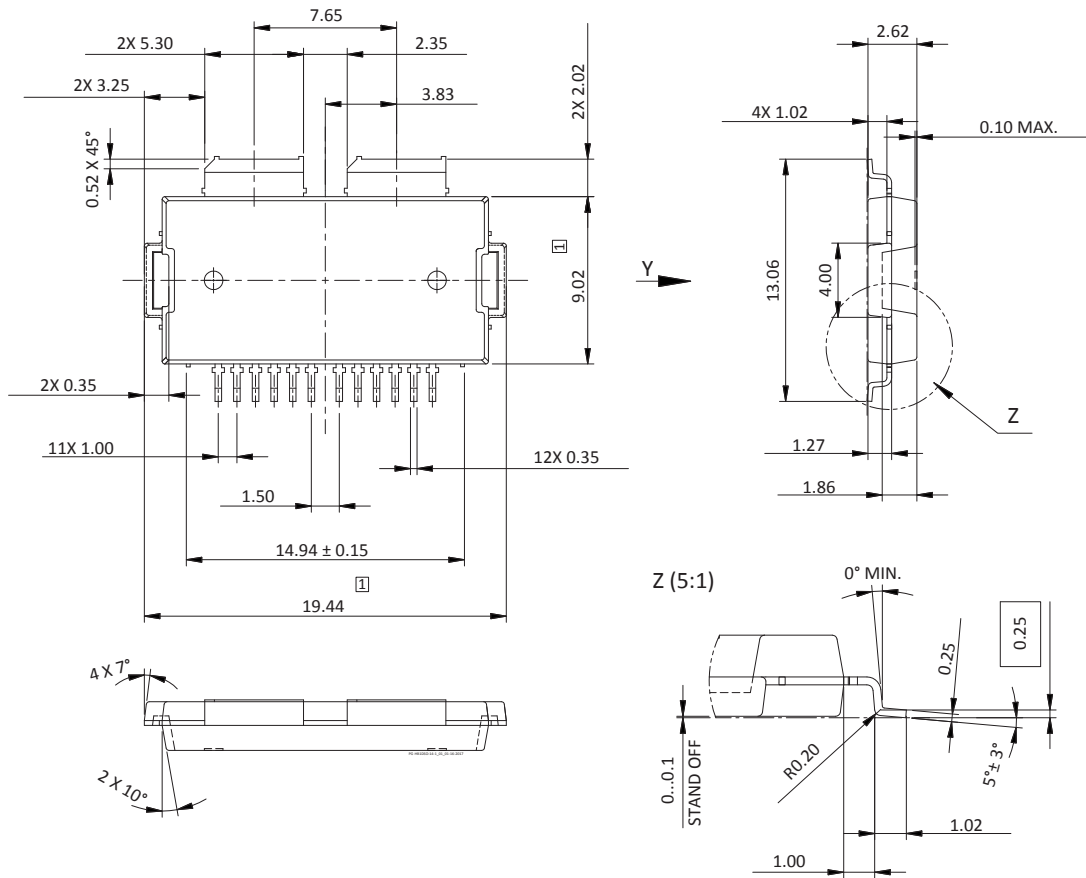


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.30 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
- 6 All tolerances ± 0.1 mm unless specified otherwise.
7. All metal surfaces pre-plated, except area of cut.
8. Lead thickness: 0.25 mm.
9. Gold plating thickness: 0.25 micron max.

Package Outline Specifications

Package PG-HB1DSO-14-1
(formed leads, bottom view)

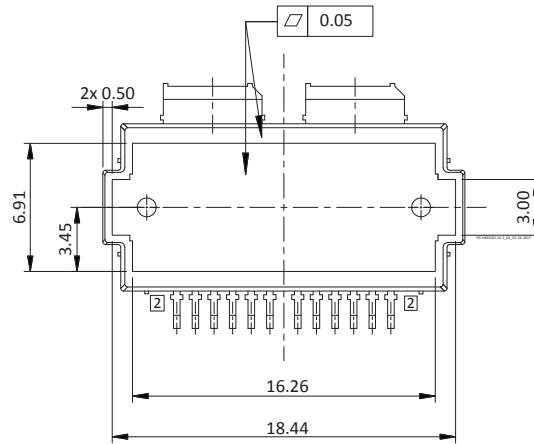


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Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2016-08-18	Advance	All	Target specifications for proposed product
02	2017-12-14	Production	All	Data Sheet reflects released product specification
03	2018-05-19	Production	All	Converted to Wolfspeed Data Sheet

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Notes

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