16V, 12A Switching Buck Regulator Module

MCPF1412M06

Description

The MCPF1412M06 is an easy-to-use, fully integrated and highly efficient Point-Of-Load (POL) 12A voltage regulator module. The on-chip Pulse-Width Modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment. This unique and optimized solution has yielded the highest density, full-featured 12A POL currently available.

The user can program aspects of the MCPF1412M06's operation using I^2C and PMBus™ protocols. The built-in protection features include soft start protection, overvoltage protection, thermally compensated overcurrent protection with hiccup mode, and thermal shutdown with auto-recovery.

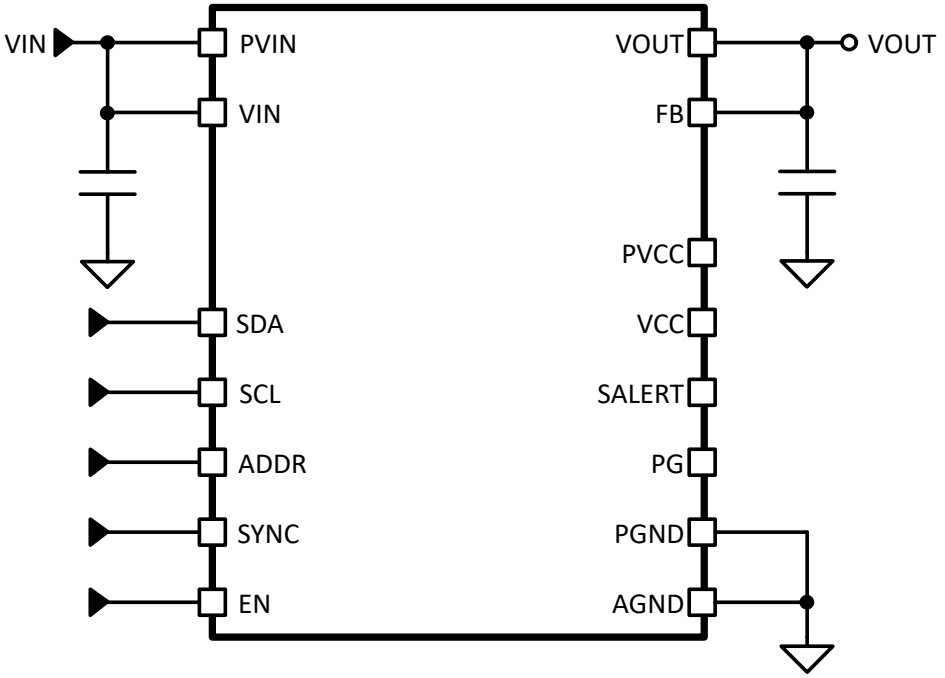
Features

- POL Module with Output Inductor Included
- Small Size: 5.8 mm x 4.9 mm x 1.6 mm
- Continuous 12A Load Capability
- Wide Input Voltage Range: 4.5-16V
- Adjustable Output Voltage: 0.6-1.8V
- No External Compensation Required
- Programmable Operation Using I^2C and PMBus™
- Enable Input, Programmable Undervoltage Lock-Out (UVLO) Circuit
- Power-Good Indicator
- Built-in Protection Features
- Operating Temperature from -40°C to +125°C
- Lead-Free and Halogen-Free
- Compliant with EU REACH and RoHS

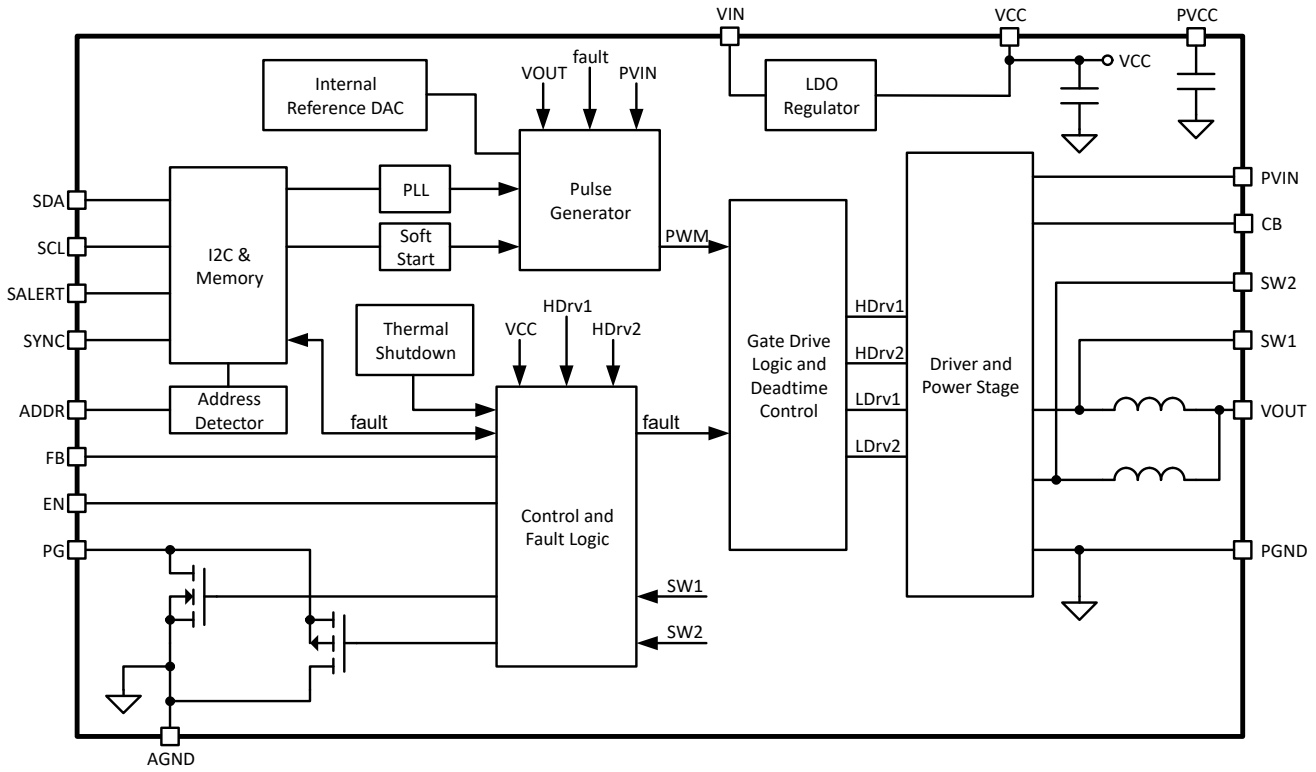
Applications

- Servers, Workstations and Cloud Computing
- Routers, Switches and Telecom Equipment
- Base Stations, Data Center Power Solutions
- High Power Density POL Conversion

Typical Application



Block Diagram

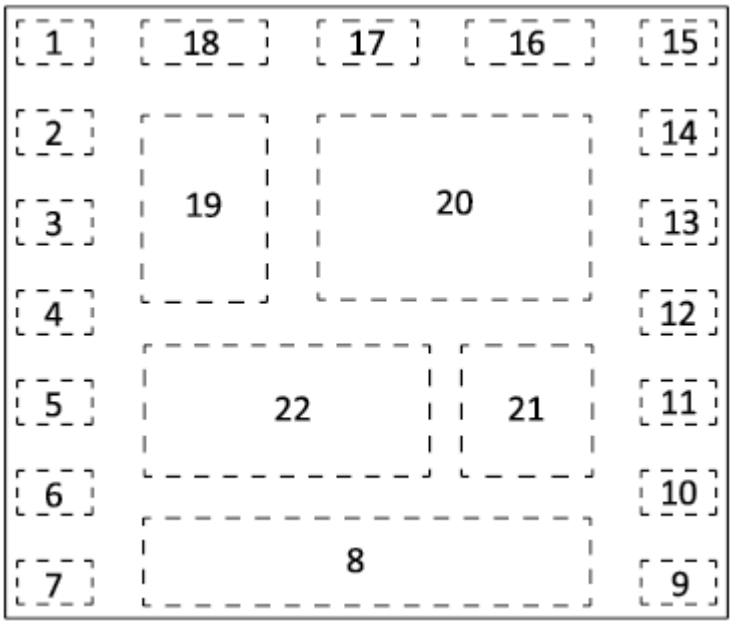


1. Pin Configuration

Pin Number	Name	Description
1	SW2	Test Pin
2	VIN	Input voltage and input to the LDO regulator.
3	EN	Enable pin. Turns the MCPF1412M06 ON and OFF. A resistor divider can be used on this pin to create an external UVLO condition.
4	PVCC	Input supply for the driver circuits. Connect to VCC.
5	VCC	Supply voltage. This is used as either a bypass capacitor connection for the internal LDO or as a connection point for an external bias voltage.
6	FB	Feedback voltage to the device. Connect the tap of a voltage divider across the output voltage to this pin to set the output voltage value.
7, 22	AGND	Signal level ground for the converter and the internal control circuitry. Connect this to the ground plane of the application.
8	VOUT	Output voltage of the regulator. Connect output filter capacitors and a 100Ω resistor from this pin to PGND.
9	PG	Power Good status indicator. An open drain FET pulls this pin down when Power Good is not asserted. Connect 49.9 kΩ from this pin to VCC or an external 5V rail.
10	ADDR	Address pin. Connect a resistor from this pin to AGND to set the I^2C address of the part.
11	SYNC	Synchronization input to synchronize the switching to an external source. Connect to AGND if not used.
12	SDA	I^2C/PMBus data I/O pin. Pull this pin up to the bus voltage with 4.99 kΩ or connect to AGND if not used.
13	SCL	I^2C/PMBus clock pin. Pull this pin up to the bus voltage with 4.99 kΩ or connect to AGND if not used.
14	SALERT	SMBAlert# line. Pull this up to bus voltage with a 4.99 kΩ resistor.
15	SW1	Optional connection for a capacitor to CB. A 0.1 to 1 µF, 16V or higher rated MLCC capacitor is recommended.
16, 20, 21	PGND	Power Ground. This is a separate ground connection for the internal power devices. Connect to the application power ground plane.
17	CB	An optional capacitor can be connected from this pin to SW1.
18, 19	PVIN	Power input terminal for the power switching stage.

1.1. Package

Figure 1-1. Pin Configuration 20-Lead 5.8 mm x 4.9 mm LGA (Top View)



2. Functional Description

2.1. Overview

The MCPF1412M06 is a user-friendly, fully integrated, and highly efficient DC/DC regulator. Its operation, including output voltage and system optimization parameters, can be programmed via the I²C/PMBus™ protocol. It employs a proprietary modulator to ensure rapid transient response. The modulator features internal compensation, making it suitable for a wide range of applications with various types of output capacitors, without encountering loop stability issues.

The MCPF1412M06 is a versatile device that offers significant flexibility for configuration and system monitoring through the I²C/PMBus™ interface. Additionally, it supports standalone operation without a digital interface, allowing designers to easily configure output voltages using simple resistor divider adjustments and monitor the system via the Power Good output.

2.2. Operation and Topology

The MCPF1412M06 employs an interleaved buck converter design, which minimizes voltage stress on internal power components, leading to a more compact size but with switching losses similar to those of a conventional interleaved buck converter with the same rating. Additionally, it features an inherent current-sharing mechanism between the two phases.

2.3. Bias Voltage

The MCPF1412M06 features an integrated Low Drop-Out (LDO) regulator that supplies the DC bias voltage for its internal circuitry, typically outputting 5.2V. For single-rail operation with internal bias, connect the VIN pin to the PVIN pin (see Figure 2-1). When using an external bias voltage, connect the VIN pin to the VCC pin to bypass the internal LDO regulator (see Figure 2-2). A separate pin (PVCC) is provided for driver bias and should be connected to VCC in the application circuit. The supply voltage, whether internal or external, increases with VIN and does not require enabling via the EN pin. Therefore, I²C/PMBus™ communication can commence once the following conditions are met:

- The VCC_UVLO start threshold is surpassed
- Memory contents are loaded
- Initialization is complete
- The address offset is read

Attention: During initialization, a small leakage current (approximately 3.4 µA) may flow from the device to the output, potentially pre-biasing the output voltage in applications with prolonged VIN/VCC rise times. To mitigate this, connect a small load capable of sinking 3.4 µA in such applications.

The I²C bus can be pulled up to either VCC or a system I²C bus voltage. The MCPF1412M06 allows for two I²C bus voltage ranges, selectable via the user register bit Bus_voltage_sel, as shown below:

Register	Bits	Name/ Description
0x7A	[2]	Bus_voltage_sel 0: 1.8-2.5V, 1: 3.3-5V

Figure 2-1. Single Supply Configuration: Internal LDO Regulator and Adjustable PVIN Undervoltage Lockout (UVLO)

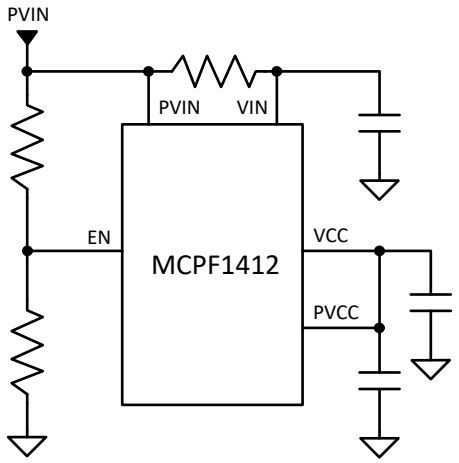
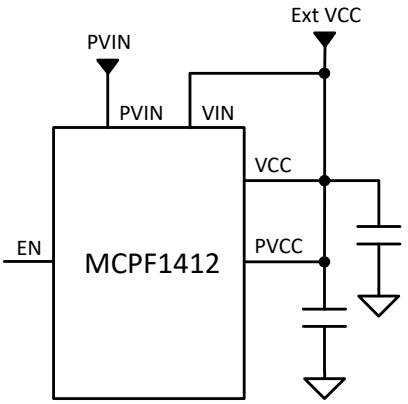


Figure 2-2. Setup for Using an External Bias Voltage



2.4. I²C Base Address and Offsets

The MCPF1412M06 features user-configurable registers to set its I²C and PMBus™ base addresses. By default, the I²C base address is 0x08, and the PMBus™ base address is 0x70. An offset ranging from 0 to 15 is determined by connecting the ADDR pin to the AGND pin, either directly or via a resistor. At startup, an address detector measures the resistance of this connection to set the offset, which is then added to the base I²C address to establish the address for I²C communication with the MCPF1412M06. The same offset is added to the base PMBus™ address to set the PMBus™ communication address.

To select offsets from 0 to 15, connect the pins as follows:

- 0 – 0Ω (short ADDR to AGND)
- +1 – 1.13 kΩ
- +2 – 1.87 kΩ
- +3 – 2.61 kΩ
- +4 – 3.4 kΩ
- +5 – 4.12 kΩ
- +6 – 4.87 kΩ
- +7 – 5.62 kΩ
- +8 – 6.34 kΩ

- +9 – 7.15 kΩ
- +10 – 7.87 kΩ
- +11 – 8.66 kΩ
- +12 – 9.31 kΩ
- +13 – 10.2 kΩ
- +14 – 11 kΩ
- +15 – 12.1 kΩ

Note: Avoid using the 7-bit address 0x0C, as it corresponds to the Alert Response Address in the SMBus™ protocol.

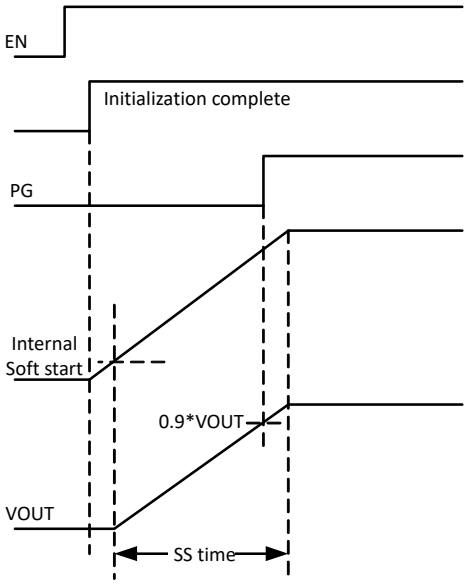
2.5. Soft Start and Target Output Voltage

The MCPF1412M06 features an internal digital soft start circuit designed to manage the output voltage rise-time and limit current surges during start-up. When VCC surpasses its start threshold ($VCC\_UVLO_{(START)}$), the MCPF1412M06 exits reset mode, initiating the loading of non-volatile memory contents into working registers and calculating the address offset as previously described. After initialization, the internal soft start ramps up towards the set reference voltage at a rate specified by the TON_RISE registers (associated with the TON_RISE command), provided the following conditions are met:

1. A valid enable signal is detected, as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PVIN, and PVIN UVLO threshold corresponding to the VIN_ON registers.
2. The internal pre-charge circuit ensures balanced PVIN/2 voltages across all FETs when the device begins switching.

During initial start-up, the MCPF1412M06 operates with minimal high-drive (HDrv) pulses until the output voltage increases (refer to Switching frequency and minimum values for ON-time, OFF-time). The ON time is increased until VOUT reaches the target value set by the VOUT_COMMAND registers. For optimal start-up performance, it is recommended to use a 100Ω resistor connected in parallel with the output capacitors (C_{OUT}). A minimum wait time of 600Ω × C_{OUT} is advised between successive power or Enable cycling operations. For instance, with a 100Ω resistor across four 47 µF output capacitors, a new Enable assertion should not occur until at least 78 ms (allowing the reduction of capacitance at a bias of 1V - see Design Example) after disabling the MCPF1412M06.

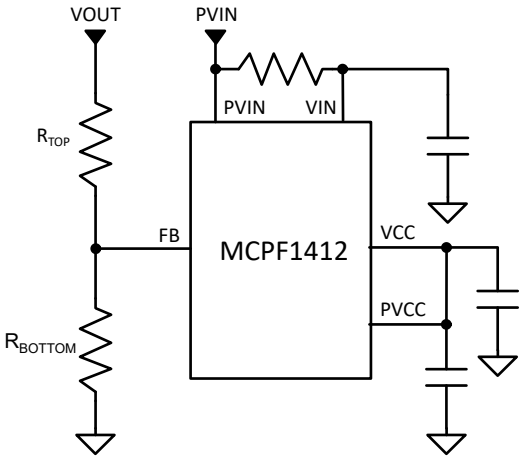
Figure 2-3. Soft Start Operation



Overcurrent Protection (OCP) and Overvoltage Protection (OVP) are active during soft start to safeguard the MCPF1412M06 from short circuits and excessive voltages.

A resistor divider can be utilized with a standard MCPF1412M06 device to set the desired output voltage (Figure 2-4). This provides system designers with the flexibility to configure all power rails in the system across the entire output voltage range (0.6–1.8V) using a single component.

Figure 2-4. Resistor Divider to Set Output Voltage



The following equation describes the appropriate resistor divider selection to set the output voltage using an MCPF1412M06 programmed to 0.6V:

$$R_{BOTTOM} = \frac{R_{TOP}}{1.7975 \times VOUT - 1.0639 - 0.00894 \times R_{TOP}}$$

Where:

R_{TOP} and R_{BOTTOM} are in kΩ.

It is recommended that system designers place a capacitor (C_{FF} in Figure 5-1) of 47 pF to 470 pF in parallel with R_{TOP}. 4.12 kΩ is suggested as a value for R_{TOP}. The recommended value for R_{BOTTOM}

depends on the output voltage, as shown in the table below. Designers should validate these values in their specific applications.

VOUT (V)	R_{BOTTOM} (kΩ)
0.72	21
0.85	9.76
0.9	8.06
0.95	6.81
1	5.9
1.05	5.23
1.1	4.75
1.2	3.92
1.5	2.55
1.8	1.91

Alternatively, the output voltage can be set using I²C/PMBus™ commands (see PMBus Commands) or the corresponding user registers, instead of an external resistor divider. The table below lists VOUT_COMMAND codes to set the specified voltages. The MCPF1412M06 supports this command with a resolution of 1/256V.

VOUT (V)	VOUT_COMMAND	VOUT (V)	VOUT_COMMAND
0.65	00A7	1.20	0134
0.70	00B4	1.25	0140
0.72	00B9	1.30	014E
0.75	00C0	1.35	015A
0.78	00C8	1.40	0167
0.80	00CD	1.45	0174
0.85	00DA	1.50	0180
0.88	00E2	1.55	018D
0.90	00E7	1.60	019A
0.95	00F4	1.65	01A7
1.00	0100	1.70	01B4
1.05	010D	1.75	01C0
1.10	011A	1.80	01CD
1.15	0127		

2.6. Shutdown Mechanisms

The MCPF1412M06 features two shutdown mechanisms:

1. **Hard Shutdown or Load-Dependent Decay**:

   A valid hard-disable is detected based on the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PVIN, and PVIN UVLO threshold corresponding to the VIN_ON registers. Both drivers are immediately turned OFF, and the soft start is pulled down instantly.

2. **Soft-Stop or Controlled Ramp Down**:

   A valid soft-OFF request is detected based on the Enable pin, Operation register, and ON_OFF_CONFIG register. After a delay defined by the TOFF_DELAY registers, the SS signal gradually decreases to 0 over a period specified by the TOFF_FALL registers. The drivers are disabled only when the SS signal reaches 0, causing the output voltage to follow the SS signal down to 0.

By default, the device is set for hard shutdown. Shutdown using PVIN is always a hard shutdown.

2.7. Switching Frequency, Minimum ON and OFF Time, PVIN

The switching frequency of the MCPF1412M06 is influenced by the output voltage and can operate in one of two modes:

- Mode A: Pseudo constant-frequency COT mode (default)
- Mode B: PLL-modulated COT mode

For the default output voltage of 0.6V, the switching frequency is typically 470 kHz, and the device functions in Mode A. In this mode, if the output voltage is adjusted using an external resistor divider, the switching frequency automatically adapts to the correct value:

$$F_{SW} = 470\ \mathrm{kHz} \times \frac{VOUT}{0.6}$$

When the output voltage is configured via the VOUT_COMMAND user registers instead of an external resistor divider, Mode B should be selected. To implement this, the user must enable the Phase-Locked Loop (PLL), which is disabled by default, and toggle the Enable pin. This action automatically sets the switching frequency to the factory-programmed values listed in the table below. The PLL adjusts the ON-time to ensure a constant switching frequency regardless of the load.

VOUT Range (V)	F_{SW} (MHz)
< 0.65	0.5
0.65 to 1.1	1.00
1.1 to 1.32	1.25
1.32 to 1.8	1.5

With either approach, system designers do not need to worry about selecting the switching frequency. When the input voltage is significantly higher than the target output voltage, the high side MOSFETs are switched ON for shorter durations. The shortest reliable ON-time is defined by the minimum ON-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very low, the MCPF1412M06 operates with the minimum ON-time.

The maximum conversion ratio is influenced by two factors:

1. When the input voltage is low, relative to the target output voltage, the Control MOSFET is switched ON for longer durations. The shortest OFF-time is defined by the minimum OFF-time ($T_{OFF(MIN)}$). During this period, the Synchronous MOSFET remains ON, and its current is monitored for overcurrent protection. This determines the minimum input voltage that can still allow the device to regulate its output at the target voltage.
2. To maintain balanced switching amplitudes in both phases, this topology requires no overlap between the high sides of the two phases, unlike a conventional buck topology. This imposes theoretical maximums of 50% on the duty cycle of each phase and 25% on the conversion ratio. In practice, considering circuit delays and dead-times, the conversion ratio should not exceed 16% at full load.

The maximum conversion ratio is influenced by both system efficiency and load transient requirements. It is recommended that system designers validate these values in their specific applications.

2.8. Enable Pin (EN)

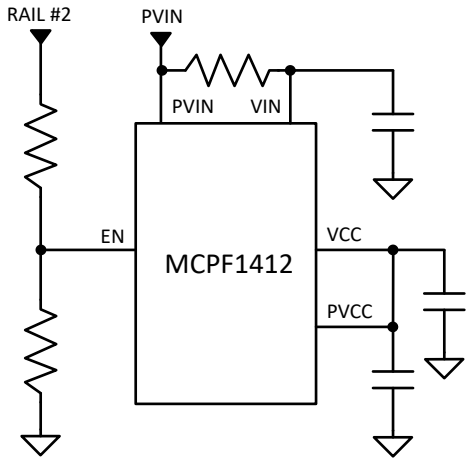
The Enable (EN) pin serves multiple purposes:

- By default, according to the ON_OFF_CONFIG command, it controls the power state of the MCPF1412M06. It features a precise threshold monitored by the UVLO circuit. If left unconnected, an internal 1 MΩ resistor pulls it down to prevent accidental activation of the MCPF1412M06.
- It can be utilized to establish a precise input voltage UVLO. The EN pin's input is derived from the PVIN voltage through a set of resistive dividers (Figure 2-1). Users can adjust the UVLO threshold

voltage by selecting different resistor ratios, allowing for finer control over the PVIN UVLO voltage levels than the VIN_ON/VIN_OFF commands provide.

- It can also be used to monitor other power rails for specific power sequencing schemes (Figure 2-5).

Figure 2-5. EN Pin Used to Monitor a Second Rail for Startup



2.9. Overcurrent Protection (OCP)

Overcurrent Protection (OCP) is achieved by monitoring the voltage across the channel RDS(ON) of the Synchronous MOSFET. When this surpasses the OCP threshold, a fault condition is triggered.

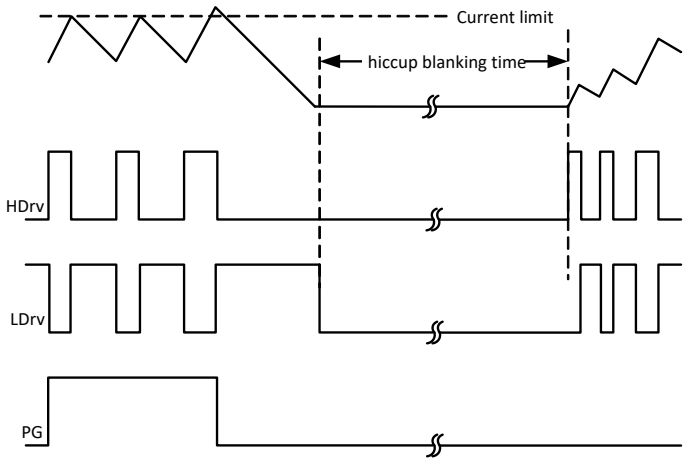
This approach offers several advantages:

- Ensures precise overcurrent protection without compromising converter efficiency (the current sensing is lossless)
- Lowers costs by eliminating the need for a current-sense resistor
- Minimizes layout-related noise issues

The OCP threshold is set by the IOUT_OC_FAULT_LIMIT command (or corresponding user registers) and can be programmed in 0.5A increments, up to a maximum of 16A. The recommended minimum overcurrent threshold is 10A. The OCP threshold is internally compensated to remain nearly constant across different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET stays ON until the current drops to 0, after which the MCPF1412M06 enters hiccup. Both the Control MOSFET and the Synchronous MOSFET remain OFF during the hiccup-blanking period. After this period, the MCPF1412M06 attempts to restart. If an overcurrent fault is still present, the previous actions are repeated. The MCPF1412M06 stays in hiccup mode until the overcurrent fault is resolved. The MCPF1412M06 can also be reprogrammed to enter a latched shutdown mode upon detecting an overcurrent fault.

Figure 2-6. Overcurrent Protection and Hiccup Operation



2.10. Overvoltage Protection (OVP)

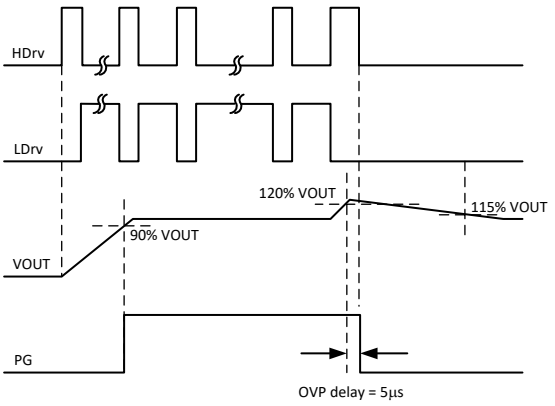
Overvoltage Protection (OVP) is achieved by monitoring the voltage at the FB pin. If the FB pin voltage surpasses the output OVP threshold for more than the output OVP delay (typically 5 µs), a fault condition is triggered.

The OVP threshold is determined by the VOUT_OV_FAULT_LIMIT command (or the corresponding user registers). This command enables the overvoltage level to be set relative to the output voltage, with a resolution of 1/256V. Internally, these values are rounded to one of four settings, as indicated in the table below.

VOUT_OV_FAULT_LIMIT (% of VOUT_COMMAND)	Actual V_{OUT} OV Threshold (% of VOUT_COMMAND)
100 to 105.4	105
105.4 to 110.1	110
110.1 to 114.8	115
less than 100 or more than 114.8	120 (Default)

The default setting is 120%. All MOSFETs are immediately switched OFF, and the PG pin is pulled low. The MOSFETs stay latched off until reset by cycling either VCC or EN. Figure 2-7 illustrates a timing diagram for overvoltage protection.

Figure 2-7. OVP Operation for Latched OVP



The MCPF1412M06 issues warnings for output overvoltage and undervoltage, and provides protection against output undervoltage faults. These functions are controlled by three commands (or their corresponding user registers):

- VOUT_OV_WARN_LIMIT
- VOUT_UV_WARN_LIMIT
- VOUT_UV_FAULT_LIMIT

The threshold mechanism for these warnings differs from the overvoltage protection mechanism: the warnings use a digital comparison of the digitized and processed VOUT telemetry against the thresholds, while the overvoltage protection uses an all-analog signal path and an internal high-speed comparator.

2.11. Overtemperature Protection (OTP)

The MCPF1412M06 includes an internal temperature sensing feature. The Overtemperature Protection (OTP) threshold is determined by a fixed internal threshold, set at 145°C. This threshold is monitored by an internal analog comparison. If the temperature exceeds this limit, the device halts switching and turns OFF all MOSFETs until the temperature falls below the threshold, at which point it automatically restarts.

2.12. Power Good (PG)

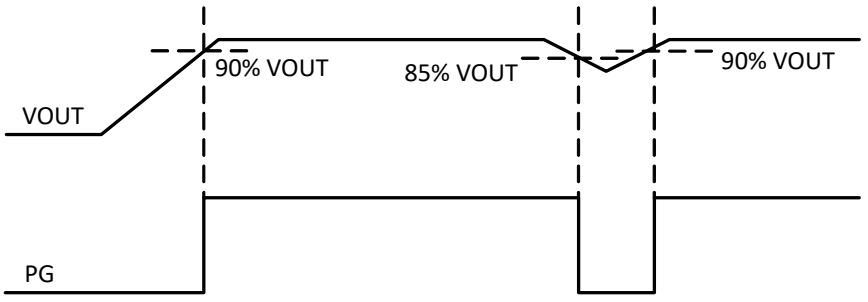
Power Good (PG) behavior is defined through the PGControl register bits and the POWER_GOOD_ON command. When the PGControl bit is enabled, the PMBus™ command can set the upper Power Good threshold relative to the output voltage with a resolution of 1/256V. Internally, these values are rounded to one of four settings, as illustrated in the table below.

POWER_GOOD_ON (% of VOUT_COMMAND)	Actual Threshold (% of VOUT_COMMAND)
Above 96.1 or below 79.6	80
Above 79.6 to 85.1	85
Above 85.1 to 89.8	90 (default)
Above 89.8 to 96.1	95

The default setting is 90%, meaning the PG signal will be activated when the voltage at the FB pin surpasses 90% of the VOUT_COMMAND setting (default 0.6V). A 5% hysteresis is applied, creating a lower threshold. If the voltage at the FB pin falls below this lower threshold, the PG signal will be deactivated.

Figure 2-8 illustrates the case where the PGControl bit is set to 1.

Figure 2-8. PG Operation With PGControl Bit Set to 1

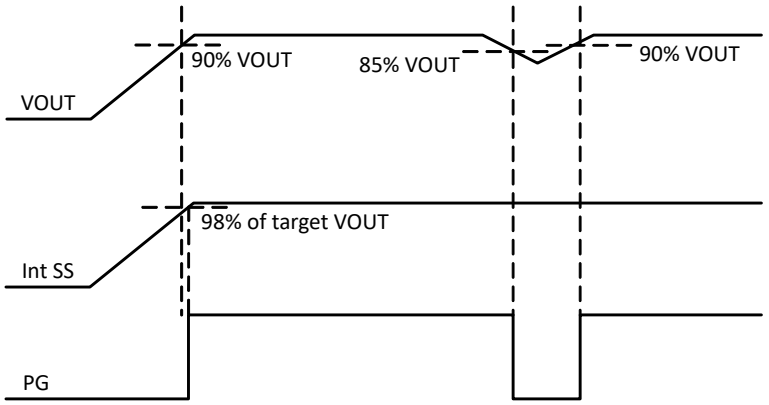


The behavior remains consistent during start-up and normal operation. The PG signal is asserted when:

- Both EN and VCC exceed their thresholds
- No faults are present (including overcurrent, overvoltage, and overtemperature)
- VOUT is within the target range (monitored continuously to ensure FB is above the PG threshold)

With the PGControl bit set to '0' the operation is as shown in Figure 2-9.

Figure 2-9. PG Operation With PGControl Bit Set to '0'



During normal operation, the PG signal functions identically to when the PGControl bit is set to '1'. However, at start-up, the PG signal is asserted once FB is within 2% of the target output voltage, rather than when FB surpasses the upper PG threshold. The MCPF1412M06 also includes an additional PMOS in parallel with the NMOS, internally connected to the PG pin (see Block Diagram). This PMOS ensures that the PG signal remains at a logic low level, even if VCC is low and the PG pin is pulled up to an external voltage other than VCC.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

PVIN, VIN, EN to PGND, CB to SW1	-0.3V to 18V
VCC to PGND	-0.3V to 6V
SW1, SW2	-0.3V to 15V
FB, SYNC, ADDR, SCL, SDA, SALERT, to AGND	-0.3V to VCC
PG to AGND	-0.3V to VCC
PGND to AGND	-0.3V to 0.3V
ESD HBM JESD22-A114	Class 1C
Maximum Junction Temperature (T_J)	-40°C to 150°C
Storage Temperature (T_S)	-55°C to 150°C
Moisture Sensitivity Rating (JEDEC, J-STD-020D)	MSL 3

Note: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2. Recommended Operating Ratings(1)

Input Voltage Range with External VCC(2)(4), PVIN	6*VOUT to 16V
Input Voltage Range with Internal LDO(3)(4) , PVIN	6*VOUT to 16V
Bias Input voltage Range(3), VIN	4.5V to 16V
Supply Voltage Range(5), VCC	4.5V to 5.5V
Output Voltage Range, VOUT	0.6V to 1.8V
Continuous Output Current Range, I_O	0A to 12A
Operating Junction Temperature Range, T_J	-40°C to 125°C

Notes:

1. The device is not guaranteed to operate outside its operating ratings.
2. VIN is connected to VCC to bypass the internal Low Drop-Out (LDO) regulator.
3. VIN is connected to PVIN (for single-rail applications with PVIN = VIN = 4.5V – 16V).
4. Maximum switch node voltage should not exceed 15V.
5. Must not exceed 6V.

3.3. DC/AC Characteristics

Electrical Characteristics: 6*V_{OUT} < PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T_A < 125°C unless specified otherwise, Typicals at T_A = 25°C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input Current						
VIN Supply Current (Standby)	$I_{IN(STANDBY)}$		7	8	mA	Enable low
VIN Supply Current (Dynamic)	$I_{IN(DYN)}$		16	18	mA	Enable High, F_{SW} = 470 kHz
Soft Start						
Soft Start Rate(1)	SS_{RATE}	0.17	0.28	0.37	V/ms	Default VOUT = 0.6V, T_{ON_RISE} = 2 ms
Output Voltage						

DC/AC Characteristics (continued)

Electrical Characteristics: 6*V_{OUT} < PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T_A < 125°C unless specified otherwise, Typicals at T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage Range	VOUT (default)		0.6		V	
	Range	0.6		1.8	V	
	Resolution		5		mV	
Accuracy			+/-0.75		%	T_J = 25°C, V_{OUT} = 0.6V
		-1		+1	%	-40°C < T_J < 125°C(2)
On-Time Timer Control						
On Time	T_{ON}	185	211	235	ns	PV_{IN} = 12V, V_{OUT} = 0.6V, F_{SW} = 470 kHz
Minimum On Time(1)	$T_{ON(MIN)}$		50		ns	
Internal Low Drop Out Regulator (LDO						
Regulator Output Voltage	VCC	4.89	5.2	5.4	V	5.5 < V_{IN} < 16V, 0-40 mA
		4.19	4.26		V	4.5 < V_{IN} < 5.5V, 0-40 mA
Load Regulation	V_{LD}			0.19	V	0-40 mA
Thermal Shutdown						
Thermal Shutdown(1)			145		C	
Hysteresis(1)			25		C	
Undervoltage Lock Out						
V_{CC} Start Threshold	$VCC\_UVLO_{(START)}$	4.0	4.2	4.4	V	VCC rising
V_{CC} Stop Threshold	$VCC\_UVLO_{(STOP)}$	3.6	3.8	4.1	V	VCC falling
Enable Threshold	$En_{(HIGH)}$	1.05	1.20	1.34	V	EN rising
	$En_{(LOW)}$	0.92	1.00	1.11	V	EN falling
Input Impedance	R_{EN}	500	1000	1500	kΩ	
Current Limit						
Current Limit Threshold	I_{OC} (default)	14.5	16	17.5	A	T_J = 25°C
	I_{OC} (range)	10		16	A	
Hiccup Blanking Time	$T_{BLK(HICCUP)}$		20		ms	
Over Voltage Protection (OVP)						
OVP Threshold(1)	V_{OVP} (default)	115	120	125	%	
	V_{OVP} (range)	105		120	%	
	V_{OVP} (resolution)		5		%	
OVP Delay	T_{OVPDEL}		5		µs	
Power Good						
Upper Threshold	$V_{PG(UPPER)}$ (default)	85	90	95	%	V_{OUT} rising
Hysteresis	$V_{PG(LOWER)}$		7		%	V_{OUT} falling
Sink Current	I_{PG}		9		mA	V_{PG} = 0.5V, EN = 2V
Telemetry						
Input Voltage Reporting Accuracy	PV_{IN}_report_err	-2		+2	%	PVIN = 12V, -40°C < TJ < 125°C
		-5		+5	%	5V < PVIN < 16V, -40°C < TJ < 125°C
Output Voltage Reporting Accuracy	V_{OUT}_report_err	-18		+18	mV	VOUT = VFB = 0.6V, -40°C < TJ < 125°C
Temperature Reporting Accuracy(1)	T_report_err	-20		+20	°C	-40°C < TJ < 125°C

DC/AC Characteristics (continued)

Electrical Characteristics: $6*V_{OUT} < PV_{IN} < 16V$, $4.5V < V_{IN} < 16V$, $0°C < T_A < 125°C$ unless specified otherwise, Typicals at $T_A = 25°C$						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**

Notes:

1. Characterized parameter, not production tested.
2. Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment.

Electrical Characteristics: $6*V_{OUT} < PV_{IN} < 16V$, $4.5V < V_{IN} < 16V$, $0°C < T_A < 125°C$ unless specified otherwise, Typicals at $T_A = 25°C$							
Parameter(1 – all parameters)	**Symbol**	**Fast-mode**		**Fast-mode Plus**		**Unit**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**		
I²C Parameters							
I²C Bus Voltage	V_{BUS}	1.8	5.5	1.8	5.5	V	
Vin Low	V_{IL}	-0.5	$0.3*V_{BUS}$	-0.5	$0.3*V_{BUS}$	V	
Vin High	V_{IH}	$0.7*V_{BUS}$		$0.7*V_{BUS}$		V	
Input Hysteresis	V_{HYS}	$0.05*V_{BUS}$		$0.05*V_{BUS}$		V	
Low Level Output Voltage 1		0	0.4	0	0.4	V	3 mA sink current, $V_{CC} > 2V$
Low Level Output Voltage 2	V_{OL2}	0	$0.2* V_{BUS}$	0	$0.2* V_{BUS}$		2 mA sink current, $V_{CC} < 2V$
Low level sink Current	I_{OL}	3		3		mA	$V_{OL} = 0.4V$
		6		6		mA	$V_{OL} = 0.6V$
Output Fall Time	T_{OF}	$20*(V_{BUS}/5.5)$	250	$20*(V_{BUS}/5.5)$	125	ns	
Max Noise Spike Width	T_{SP}	0	50	0	50	ns	
Input Current	I_{IN}	-10	10	-10	10	mA	
Input Capacitance	C_I	-	10	-	10	pF	
SCL Frequency	F_{SCL}	0	400	0	1000	kHz	
Repeated Start Hold Time	$T_{HD;STA}$	0.6	-	0.26	-	µs	
SCL Low Time	T_{LOW}	1.3	-	0.5	-	µs	
SCL High Time	T_{HIGH}	0.6	-	0.26	-	µs	
Repeated Start Setup Time	$T_{SU;STA}$	0.6	-	0.26	-	µs	
Data Hold Time	$T_{HD;DAT}$	0	-	0	-	µs	
Data Setup Time	$T_{SU;DAT}$	100	-	50	-	ns	
SDA, SCL Rise Time	T_R	20	300	-	120	ns	
SDA, SCL Fall Time	T_F	$20*(V_{DD}/5)$	300	$20*(V_{BUS}/5)$	120	ns	
STOP setup Time	$T_{SU;STO}$	0.6	-	0.26	-	µs	
Bus Free Time between STOP and START	T_{BUF}	1.3	-	0.5	-	µs	
Bus Capacitive Load	C_{BUS}	-	400	-	550	pF	
Data Valid Time	$T_{VD;DAT}$	-	0.9	-	0.45	µs	
Data Valid ACK Time	$T_{VD;ACK}$	-	0.9	-	0.45	µs	
Noise Margin at LOW Level	V_{NL}	$0.1*V_{DD}$	-	$0.1*V_{DD}$	-	V	
Noise Margin at HIGH Level	V_{NH}	$0.2*V_{DD}$	-	$0.2*V_{DD}$	-	V	

DC/AC Characteristics (continued)

Electrical Characteristics: 6*V_{OUT} < PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T_A < 125°C unless specified otherwise, Typicals at T_A = 25°C							
Parameter(1 – all parameters)	**Symbol**	**Fast-mode**		**Fast-mode Plus**		**Unit**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**		
SDA Timeout	T_{TO}	200		200		µs	

Note:

1. Characterized parameter, not production tested.

Table 3-1. Package Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	—	20.5	—	°C/W	JEDEC JESD 51-2A
Junction to PCB Thermal Resistance	$R_{\theta J\text{-}PCB}$	—	5.5	—	°C/W	JEDEC JESD 51-8

4. Typical Performance Curves

The graphs and tables provided in this section are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Important: Unless otherwise stated, test conditions are 12V input, 1.2V output, mode A operation, using a voltage divider to set the output voltage.

Figure 4-1. Load Regulation vs. Temperature

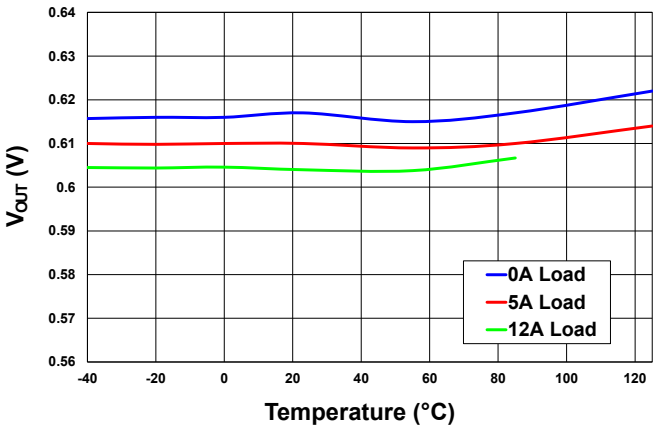


Figure 4-2. Enable Start Threshold vs. Temperature

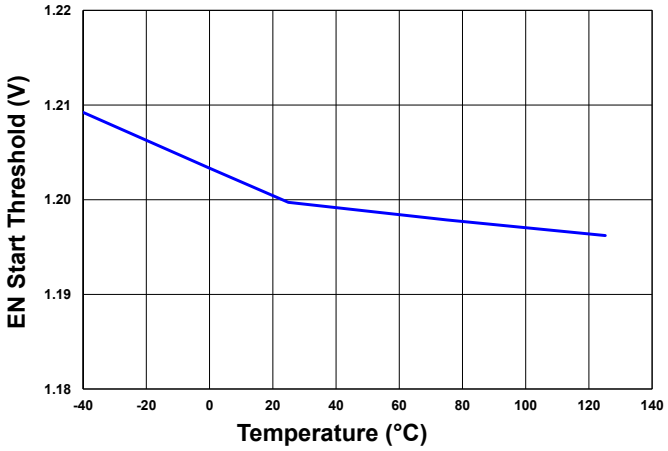


Figure 4-3. Enable Stop Threshold vs. Temperature

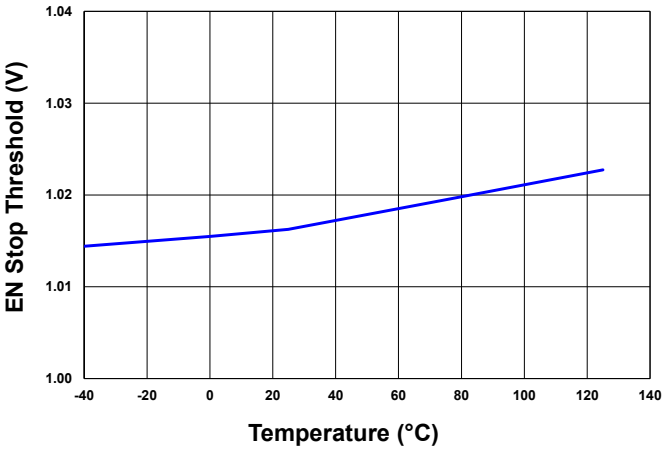


Figure 4-4. VCC Start Threshold vs. Temperature

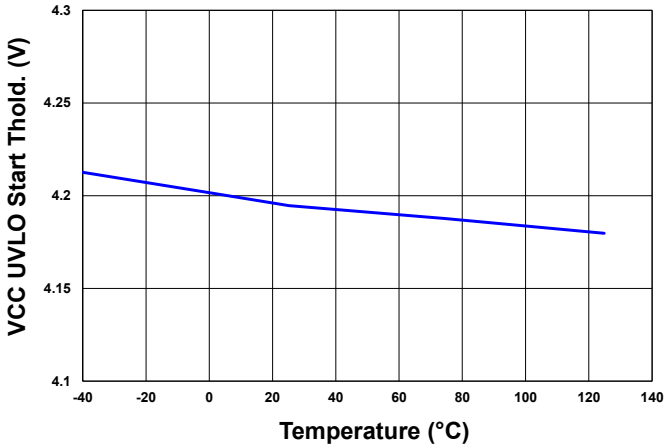


Figure 4-5. VCC Stop Threshold vs. Temperature

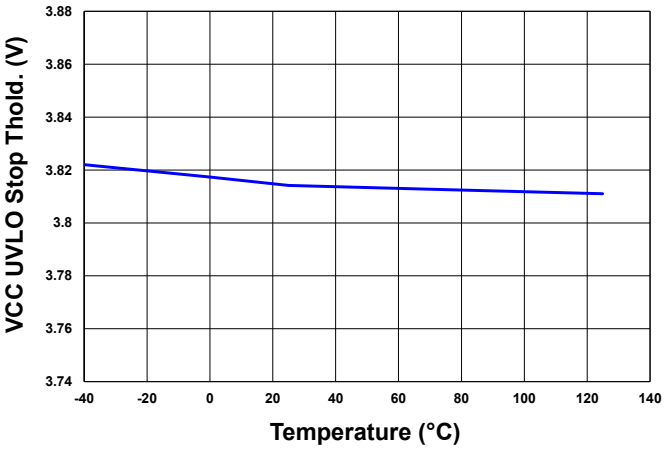


Figure 4-6. ON Time vs. Temperature

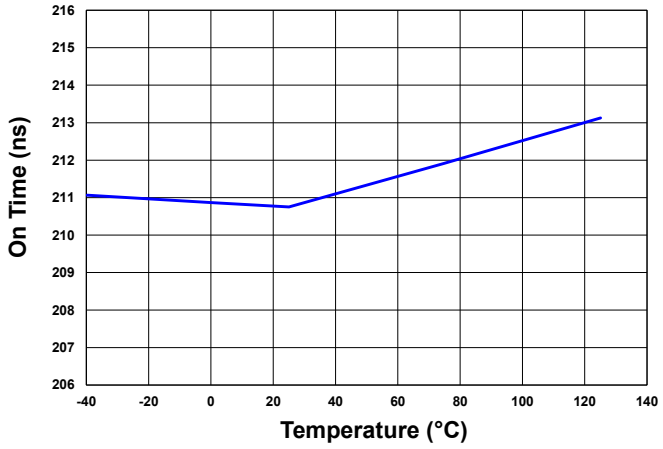


Figure 4-7. OFF Time vs. Temperature

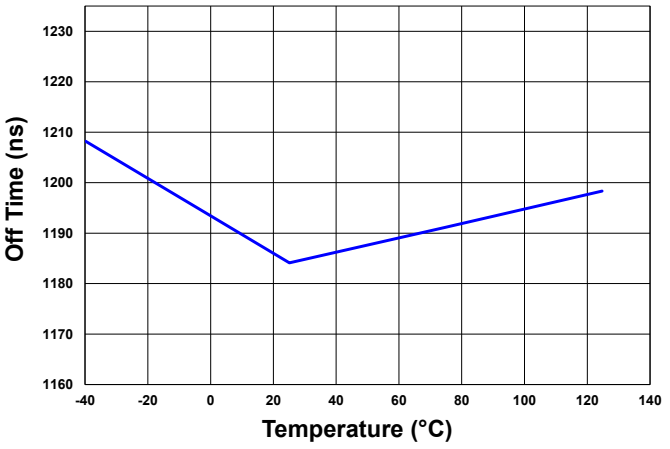


Figure 4-8. Soft Start Rate vs. Temperature

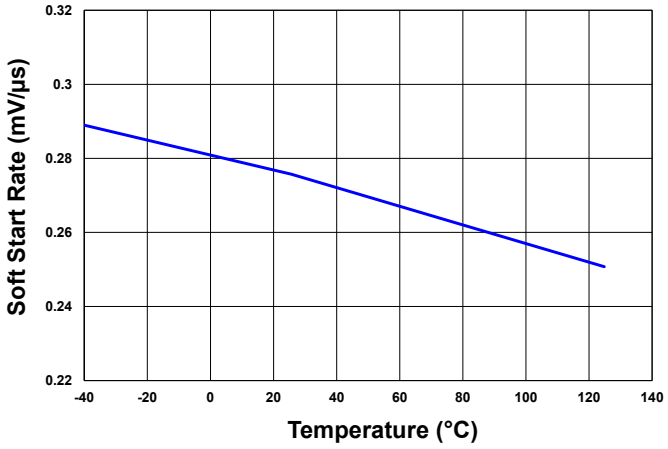


Figure 4-9. Dynamic Input Current vs. Temperature

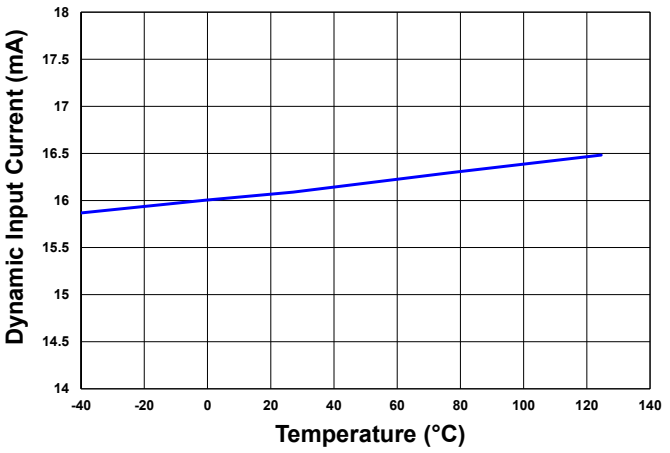


Figure 4-10. Typical Efficiency (PVIN = 12V, V_{OUT} = 1.0V)

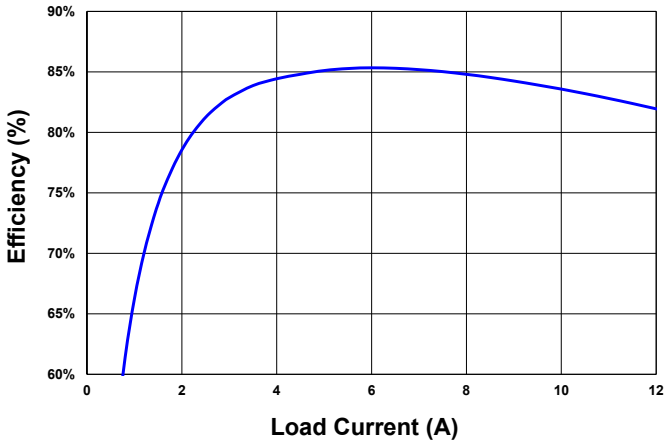


Figure 4-11. Typical Power Loss (PVIN = 12V, V_{OUT} = 1.0V)

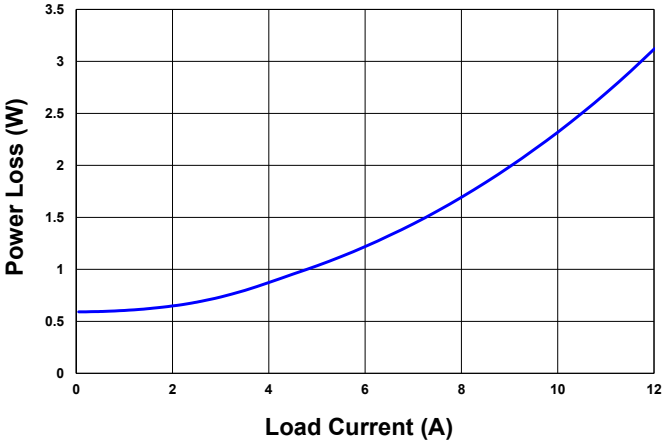


Figure 4-12. Typical Load Regulation (PVIN = 12V, V_{OUT} = 1.0V, I_{OUT} = 0-12A, Room Temeperature, No Air Flow, All Loses Included)

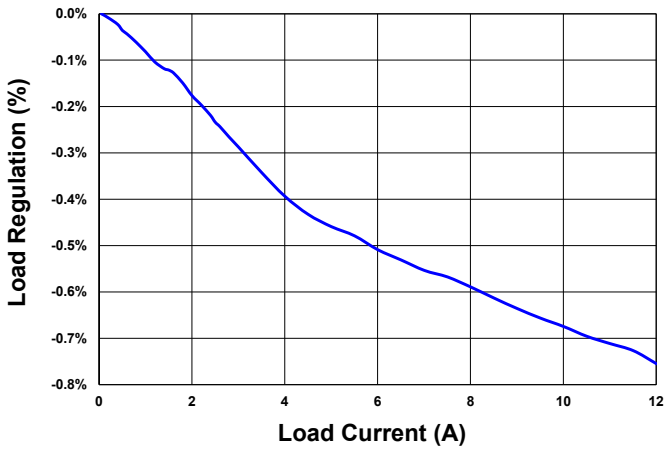


Figure 4-13. Typical Efficiency (PVIN = 12V, V_{OUT} = 1.8V, External VCC Source Applied)

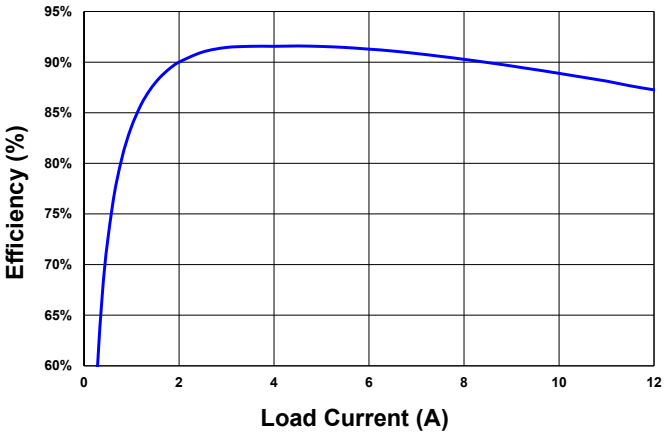


Figure 4-14. Typical Power Loss (PVIN = 12V, V_{OUT} = 1.8V, External VCC Source Applied)

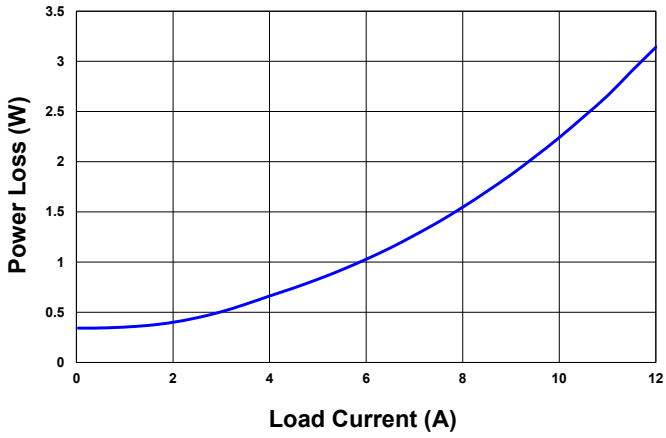


Figure 4-15. Typical Load Regulation (PVIN = 12V, V_{OUT} = 1.8V, External VCC Source Applied)

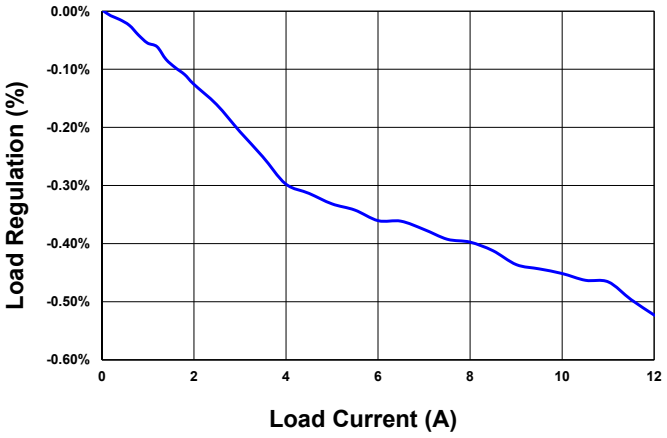


Figure 4-16. Startup (No Load)

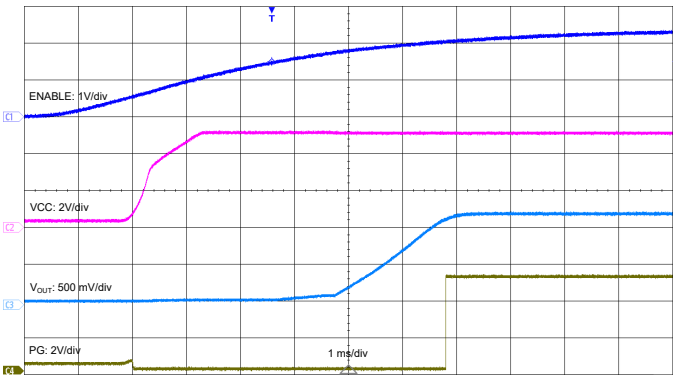


Figure 4-17. Startup (12A Load)

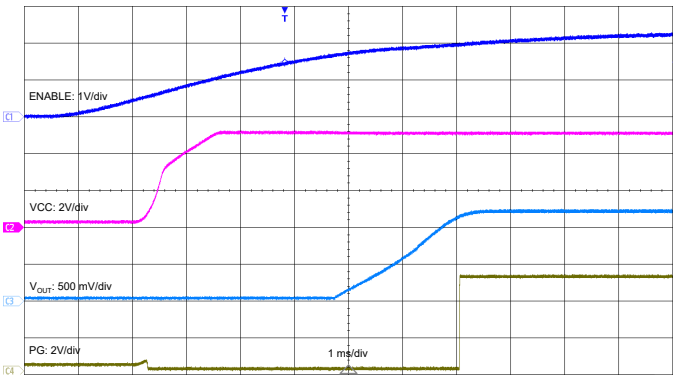


Figure 4-18. Shutdown via EN De-assertion (No Load)

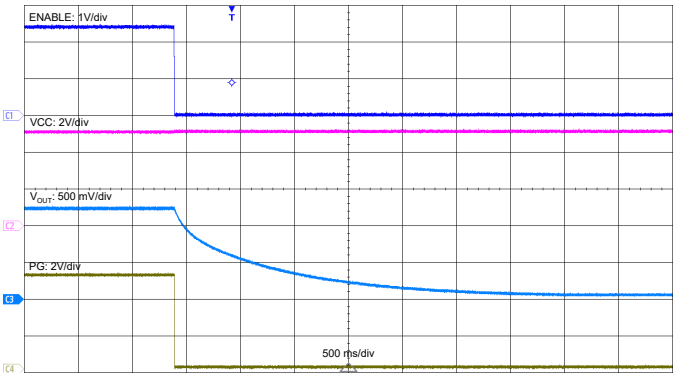


Figure 4-19. Shutdown via EN De-assertion (12A Load)

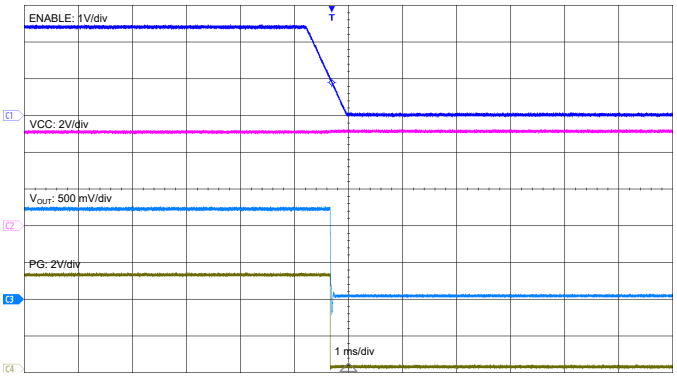


Figure 4-20. Switching Waveforms (No Load)

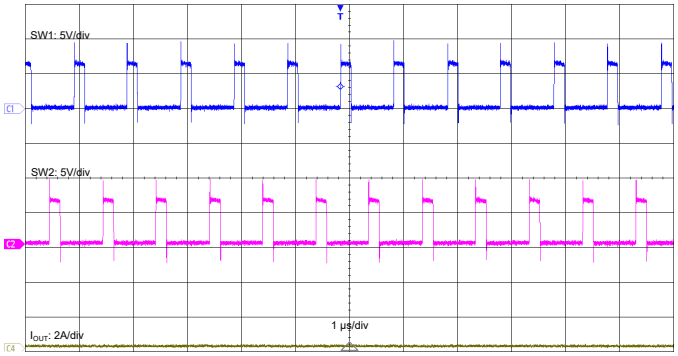


Figure 4-21. Switching Waveforms (12A Load)

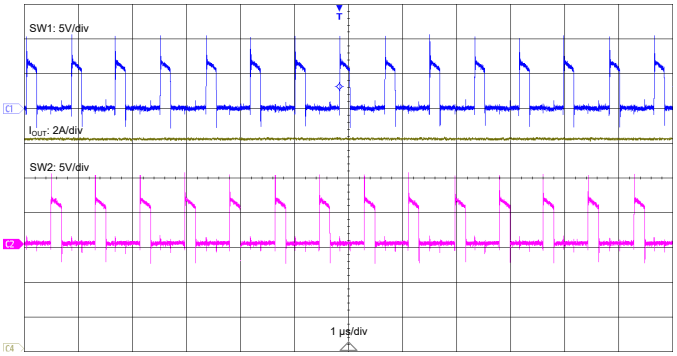


Figure 4-22. V_{OUT} Ripple - Persistent

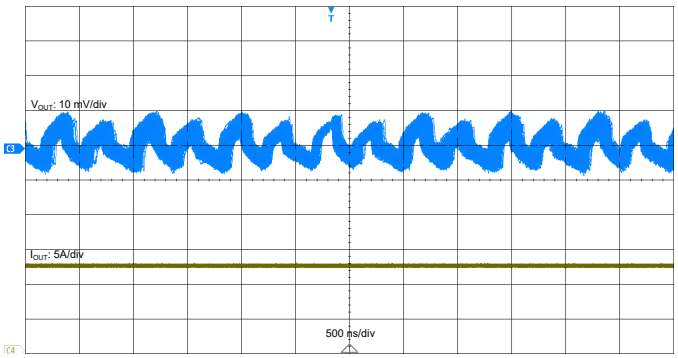


Figure 4-23. V_{OUT} Ripple

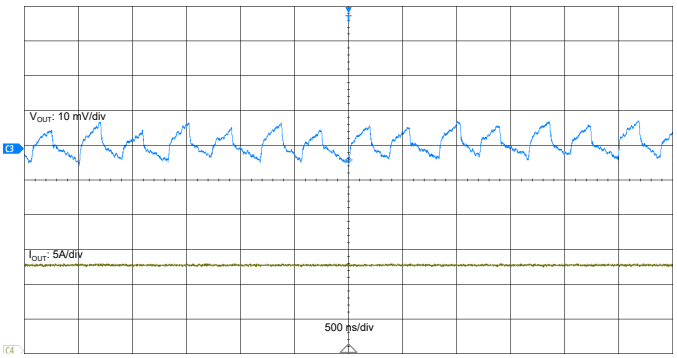


Figure 4-24. Transient Response - Persistent

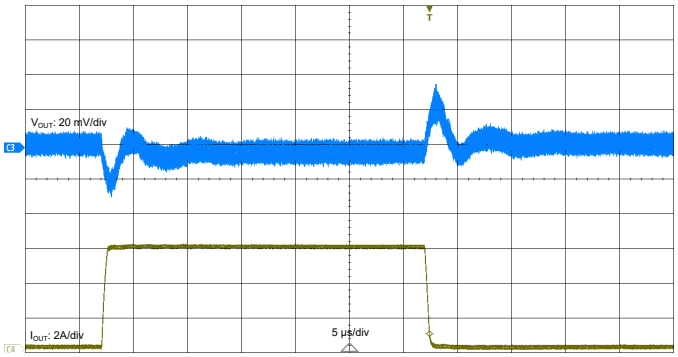
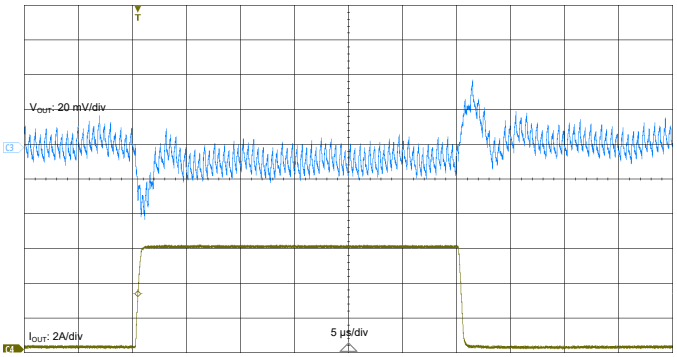


Figure 4-25. Transient Response



5. Design Example

For this example, the specifications are:

- $PV_{IN} = V_{IN}$ = 12V
- V_{OUT} = 1.0V
- I_{OUT} = 12A
- F_{SW} = 800 kHz
- C_{OUT} = 4 x 47 µF
- C_{IN} = 3 × 22 µF
- Ripple Voltage = ±1% × V_{OUT}
- $\Delta V_{OUT(MAX)}$ = ±3% × V_{OUT} (for 50% load transient @ 40 A/µs)

Input Capacitor

The input capacitor chosen for this design must:

- Accommodate the peak and RMS input currents required by the MCPF1412M06
- Possess low equivalent series resistance (ESR) and inductance (ESL) to minimize input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal for this purpose. Typically, in an 0805 case size, they can handle 2A RMS current with less than a 5°C temperature rise. For the MCPF1412M06 converter topology operating at duty cycle D and output current I_{OUT}, the RMS value of the input current is:

$$I_{RMS} = 0.5 \times I_{OUT} \times \sqrt{D \times (1 - D)}$$

In this application I_{OUT} is 12A and D is 2 × VOUT/VIN (aggregate duty for a 2 phase converter) or 0.167. Thus, the input capacitor I_{RMS} is 2.23A, and we can choose three 22 µF 25V ceramic capacitors for the input capacitors (C2012X5R1E226M125AC from TDK). If the MCPF1412M06 is not positioned near the 12V power supply, an additional bulk capacitor (68–330 µF) may be used alongside the ceramic capacitors.

For VIN, which serves as the input to the LDO, it is recommended to place a 1 µF capacitor very close to the pin. The VIN pin should be connected to PVIN via a 2.7Ω resistor and a 1 µF capacitor at the PVIN pin, to help filter noise on PVIN.

Output Voltage and Output Capacitor

The MCPF1412M06 is factory-calibrated to deliver a 0.6V output in a closed-loop configuration. When opting for a resistor divider instead of using I²C/PMBus™, as illustrated in the application example, resistor values should be selected based on the guidelines provided in Section 2.5. Consequently, R_{TOP} is set to 4.12 kΩ, R_{BOTTOM} to 5.9 kΩ, and C_{FF} to 220 pF. The design necessitates minimal output capacitance to achieve the desired output voltage ripple and maximum output voltage deviation during load transients. For the MCPF1412M06, the minimum number of output capacitors needed to meet the target peak-to-peak VOUT ripple is:

$$N_{MIN} = 5.8 \times \frac{\frac{(1-D)}{8 \times C \times F_{SW}} + ESR \times (1 - D) + \frac{ESL \times F_{SW} \times \left(1 - D^2\right)}{D}}{\Delta VOUT_{ripple(p-p)}}$$

Where:

- N_{MIN} is the minimum number of output capacitors required
- C is the equivalent capacitance of each capacitor
- F_{SW} is the switching frequency

- ESR is the equivalent series resistance of each output capacitor
- ELS is the equivalent series inductance of each capacitor
- $\Delta VOUT_{ripple(p-p)}$ is the maximum peak to peak output ripple allowed

This design uses the TDK C2012X5R0J476M125AC, a 47 µF MLCC with an 0805 case size and a 6.3V rating. Considering DC bias and AC ripple derating at 1.0V, its equivalent capacitance is 33 µF. The equivalent series resistance (ESR) is 3 mΩ, and the equivalent series inductance (ESL) is 0.44 nH. Using these parameters in the equation results in:

$N_{MIN} = 2.27$

To achieve the maximum voltage deviation ΔV_{Omax} during a ΔI_O load transient, the minimum number of output capacitors needed is:

$$N_{MIN} = \frac{0.196 \times \Delta I^2}{4 \times \Delta V_{Omax} \times F_{SW} \times C}$$

Where:

- ΔI is the load step
- ΔV_{Omax} is the maximum voltage deviation allowed
- F_{SW} is the switching frequency
- C is the capacitance of each capacitor

Using a capacitance of 33 µF, it is determined that a minimum of 2.22 output capacitors are needed. For our design, which is intended for space-constrained applications, we have chosen to use four C2012X5R0J476M125AC capacitors.

It is important to note that the calculation for the minimum number of output capacitors under a load transient is based on several assumptions:

- No Equivalent Series Resistance (ESR) or Equivalent Series Inductance (ESL) – (a)
- The converter can instantly saturate its duty cycle – (b)
- No latency – (c)
- Step load with an infinite slew rate – (d)

Assumptions (a), (b), and (c) are optimistic, while assumption (d) is conservative. Therefore, in practical applications, additional capacitance may be necessary to meet transient requirements, and this should be carefully evaluated by the system designer.

Even without a specified target VOUT ripple or maximum voltage deviation under load transient, a minimum of one 22 µF capacitor is necessary to ensure stable operation without excessive jitter. Up to eight 47 µF capacitors can be used in the design. If additional capacitance is needed, it is advisable to use a high-value capacitor with a relatively high ESR (>3 mΩ).

VCC and PVCC Capacitors

The MCPF1412M06 incorporates on-package capacitors for both VCC and PVCC to ensure efficient high-frequency bypassing. However, for applications utilizing an external VCC supply, it is advisable for system designers to place 2.2 µF/0603/X7R/10V capacitors on the application board as close as possible to the VCC and PVCC pins (see Figure 5-1).

Figure 5-1. Application Circuit Design for PV_{IN} = 12V, V_{OUT} = 1.0V and I_{OUT} = 12A

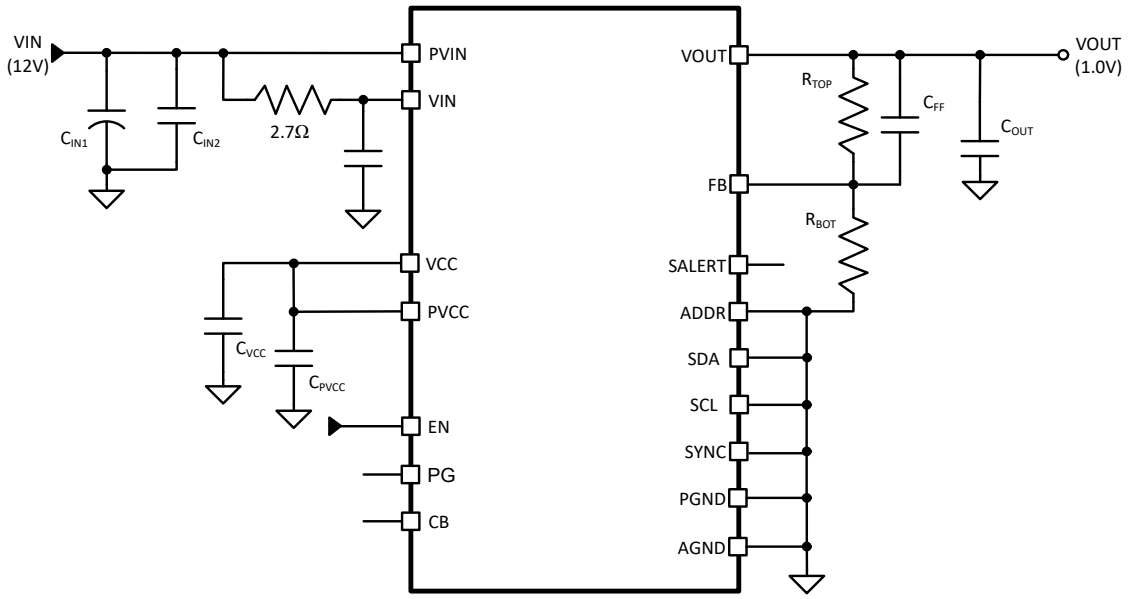


Table 5-1. Application Circuit Design Components

C_{IN1}	68 µF, 25V (optional)
C_{IN2}	2 x 22 µF, 16V, 0805, X5R
C_{VCC}	2.2 µF, 10V, 0603, X5R (optional)
C_{PVCC}	2.2 µF, 10V, 0603, X5R (optional)
C_{FF}	220 pF
R_{TOP}	4.12 kΩ
R_{BOT}	5.9 kΩ
C_{OUT}	4 x 47 µF, 6.3V, 0805, X5R

6. Layout Recommendations

General

The MCPF1412M06 is a highly integrated device requiring minimal external components, which simplifies PCB layout. However, to ensure optimal performance, adhere to these general PCB design guidelines:

- Place bypass capacitors, including input/output capacitors and the VCC bypass capacitor (if used), as close as possible to the MCPF1412M06 pins.
- Sense the output voltage with a separate trace directly from the output capacitor.
- For thermal dissipation, connect the PGND pad to the power ground plane using vias. Copper-filled vias are preferred, but plated-through-hole vias are acceptable if not covered with solder mask. VIPPO techniques are also acceptable.
- Use an adequate number of vias to connect between layers, especially for power traces.
- Connect AGND pins to the PGND copper layer using vias.
- To minimize power losses and improve thermal dissipation, use wide copper polygons for input and output power connections.

Thermal

The MCPF1412M06 has undergone thermal testing and modeling in line with JEDEC standards JESD 51-2A and JESD 51-8. Testing was conducted using a 4-layer application PCB, featuring thermal vias beneath the device to aid in cooling.

The MCPF1412M06 has two main heat sources:

• The power MOSFET section of the IC

• The inductor

The IC is effectively coupled to the PCB, which serves as its primary cooling pathway. While the inductor is also connected to the PCB, its main cooling mechanism is through convection. Ultimately though, both heat sources dissipate heat through convection. The PCB functions as a heat spreader or, to some extent, a heat sink.

Figure 6-1. Heat Sources in the MCPF1412M06

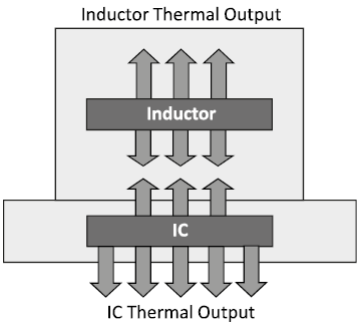
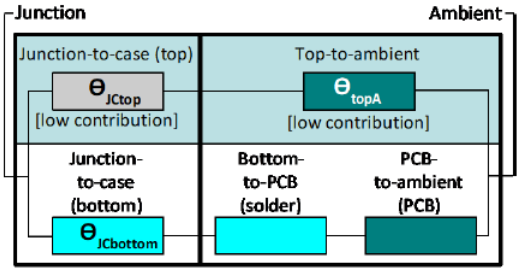


Figure 6-2 illustrates the thermal resistances in the MCPF1412M06, described as follows:

- θ_{JA} represents the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30 x 30 x 30 cm. The air in this environment is passive, with movement occurring solely due to convection from the device under test.
- $\theta_{JCbottom}$ indicates the heat flow from the IC to the bottom of the package, where it is well-coupled. The testing method follows the procedure outlined in JESD 51-8, with the test PCB clamped between cold plates at specified distances from the device.

- θ_{JCtop} theoretically represents the heat flow from the IC to the top of the package. However, this is not applicable to the MCPF1412M06 for two reasons: firstly, it is not the primary conduction path of the IC, and more importantly, the inductor is positioned directly over the IC. Since the inductor generates a similar amount of heat as the IC, a meaningful value for junction-to-case (top) cannot be determined.

Figure 6-2. Thermal Resistances of the MCPF1412M06. Internal on the Left, External on the Right



The thermal resistance values are as follows:

- θ_{JA} = 20.5°C/W
- $\theta_{JCbottom}$ = 5.5°C/W

While these values provide a comparison of the MCPF1412M06 with similar POL products under identical conditions and specifications, they are not sufficient for predicting overall thermal performance. For precise modeling of the device's interaction with its environment, Computational Fluid Dynamics (CFD) simulation software is required to simultaneously calculate the combined effects of conduction and convection.

Note: All tests assume passive or static airflow; applications using forced air may achieve better cooling.

7. PMBus Commands

Table 7-1. PMBus Commands List

No.	Name	Adr.	No.	Name	Adr.	No.	Name	Adr.
1	OPERATION	0x01	18	VOUT_OV_FAULT_RESPONSE	0x41	35	STATUS_BYTE	0x78
2	ON_OFF_CONFIG	0x02	19	VOUT_OV_WARN_LIMIT	0x42	36	STATUS_WORD	0x79
3	CLEAR_FAULTS	0x03	20	VOUT_UV_WARN_LIMIT	0x43	37	STATUS_VOUT	0x7A
4	WRITE_PROTECT	0x10	21	VOUT_UV_FAULT_LIMIT	0x44	38	STATUS_IOUT	0x7B
5	STORE_USER_ALL	0x15	22	VOUT_UV_FAULT_RESPONSE	0x45	39	STATUS_INPUT	0x7C
6	RESTORE_USER_ALL	0x16	23	IOUT_OC_FAULT_LIMIT	0x46	40	STATUS_TEMPERATURE	0x7D
7	CAPABILITY	0x19	24	IOUT_OC_FAULT_RESPONSE	0x47	41	STATUS_CML	0x7E
8	SMBALERT_MASK	0x1B	25	VIN_OV_FAULT_LIMIT	0x55	42	READ_VIN	0x88
9	VOUT_MODE	0x20	26	VIN_OV_FAULT_RESPONSE	0x56	43	READ_VOUT	0x8B
10	VOUT_COMMAND	0x21	27	VIN_UV_WARN_LIMIT	0x58	44	READ_TEMPERATURE	0x8D
11	VOUT_MAX	0x24	28	POWER_GOOD_ON	0x5E	45	PMBUS_REVISION	0x98
12	VOUT_MARGIN_HIGH	0x25	29	TON_DELAY	0x60	46	MFR_ID	0x99
13	VOUT_MARGIN_LOW	0x26	30	TON_RISE	0x61	47	MFR_MODEL	0x9A
14	VOUT_TRANSITION_RATE	0x27	31	TON_MAX_FAULT_LIMIT	0x62	48	MFR_REVISION	0x9B
15	VIN_ON	0x35	32	TON_MAX_FAULT_RESPONSE	0x63	49	IC_DEVICE_ID	0xAD
16	VIN_OFF	0x36	33	TOFF_DELAY	0x64	50	IC_DEVICE_REV	0xAE
17	VOUT_OV_FAULT_LIMIT	0x40	34	TOFF_FALL	0x65			

OPERATION (0x01)

The OPERATION command is used to turn the device output ON or OFF. It is also used to set the output voltage to the upper or lower MARGIN voltages.

COMMAND	OPERATION							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	1	0	0	0	0	0	0	0

Bit [7]: Controls if PMBus device output is ON or OFF

- 0 : Output is OFF
- 1 : Output is ON

Bit [6]: Controls the power down behavior

- 0 : Output is turned OFF immediately
- 1 : The device is powered down following the values set in the TOFF_DELAY command

Bit [5:4]: Voltage command source

- 00 : The nominal output voltage is set by the PMBus VOUT_COMMAND data
- 01 : The nominal output voltage is set by the PMBus VOUT_MARGIN_LOW data
- 10 : The nominal output voltage is set by the PMBus VOUT_MARGIN_HIGH data
- 11 : AVS Bus (AVS Bus not supported)

Bit [3:2]: Margin fault response

- 00 : Invalid
- 01 : The faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are ignored

- 10 : The faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are acted upon
- 11 : Invalid

Bit [1]: Transition control (AVS Bus not implemented)

Bit [0]: Reserved

ON_OFF_CONFIG (0x02)

COMMAND	ON_OFF_CONFIG							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	1	1	1	1	1

Bit [7:5]: Reserved

Bit [4]: Sets the default to either operate when power is present or for the ON/OFF to be controlled by serial bus commands

- 0 : Device powers up when the power is present
- 1 : Device does not power up until commanded by the OPERATION command

Bit [3]: Controls how the unit responds to commands received via the serial bus

- 0 : Device ignores the ON/OFF portion of the OPERATION command from serial bus
- 1 : Device requires the ON/OFF portion of the OPERATION command

Bit [2]: Controls how the unit responds to the EN pin

- 0 : Unit ignores the EN pin (ON/OFF controlled only the OPERATION command)
- 1 : Unit requires the EN pin to be asserted to start the unit

Bit [1]: Polarity of the EN pin

- 0 : Active low
- 1 : Active high

Bit [0]: EN pin action

- 0 : Use the programmed turn OFF delay and fall time
- 1 : Turn OFF the output and stop transferring energy to the output as fast as possible

CLEAR_FAULTS (0x03)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device releases its SMBALERT signal output if the device is asserting the SMBALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

WRITE_PROTECT (0x10)

COMMAND	WRITE_PROTECT							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	0	0

Bit [7]: Control writing to the PMBus device for protection against accidental changes

- 0 : Enable all writes as permitted in bit 5 or bit 6
- 1 : Disable all writes except the WRITE_PROTECT command (bit 5 and bit 6 must be 0)

Bit [6]: Control writing to the PMBus device for protection against accidental changes

- 0 : Enable all writes as permitted in bit 5 or bit 7
- 1 : Disable all writes except for the WRITE_PROTECT, and OPERATION commands (bit 5 and bit 7 must be 0)

Bit [5]: Control writing to the PMBus device for protection against accidental changes

- 0 : Enable all writes as permitted in bit 6 or bit 7
- 1 : Disable all writes except the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND. (bit 6 and bit 7 must be 0)

Bit [4:0]: Reserved

STORE_USER_ALL (0x15)

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permissible to use this command while the device is switching. To use this command:

1. Set all settings to the desired power up configuration.
2. Pull EN low to disable switching.
3. Apply 7.5 ± 0.25V to the VIN pin
4. Execute the command.
5. Execute a RESTORE_USRE_ALL command..
6. Compare the settings in the part values with the expected settings. If they differ, repeat this procedure. If the settings differ a second time, discard the part.

RESTORE_USER_ALL (0x16)

The RESTORE_USER_ALL command restores all of the storable register settings from EEPROM memory to those registers which are unprotected. This command should not be used while the part is converting power.

CAPABILITY (0x19)

COMMAND	CAPABILITY							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	1	1	0	0	0	0

Bit [7]: Packet Error Checking

- 0 : Packet Error Checking not supported

Bit [6:5]: Maximum Bus Speed

- 01 : Maximum supported bus speed is 400 kHz

Bit [4]: SMBALERT#

- 1 : Enable the SMBus Alert Response protocol

Bit [3]: Numeric Format

- 0 : Numeric data is in LINEAR11, ULINEAR16, SLINEAR16

Bit [2]: AVSBus Support

- 0 : AVSBus not supported

Bit [1:0]: Reserved

SMBALERT_MASK (0x1B)

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SMBALERT# signal. The bits in the mask byte align with the bits in the corresponding status register. For example if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an Overtemperature Warning condition would be blocked from asserting SMBALERT#. This command cannot be used with STATUS_BYTE or STATUS_WORD. Since these commands are the logical or of underlying status registers, use the underlying status commands as the status command code sent to set a mask value. The access mode is a write word transaction for the write and a block write block read transaction for reading. Refer to the SMBus specification for details on this transaction.

VOUT_MODE (0x20)

The data byte for the VOUT_MODE command is one byte that consists of bit [7:5] as Mode and bit[4:0] as Exponent Parameter. The three-bit Mode sets whether the device uses the ULINEAR16, Half-precision IEEE 754 floating point, VID or DIRECT modes for output voltage related commands. The five-bit Parameter provides more information about the selected mode.

COMMAND	VOUT_MODE							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	1	0	0	1	1	0	0	0

Bit [7]: Data type

- 1 : Device supports relative mode

Bit [6:5]: Data type

- 00 : Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command

Bit [4:0]: Exponent parameter

VOUT_COMMAND (0x21)

The VOUT_COMMAND command sets the output voltage in volts

COMMAND	VOUT_COMMAND															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 format															
Default #	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0

Bit [15:0]: Two linear16 data bytes

Note that this part does not use VOUT_SCALE_LOOP. The value provided via the VOUT_COMMAND command is the voltage that the part will regulate the FB pin to. Any voltage divider used on that pin will need to be accounted for by the user when using VOUT_COMMAND.

VOUT_MAX (0x24)

The VOUT_MAX command sets the maximum output voltage. The purpose is to protect the devices on the output rail supplied by this device from a higher than acceptable output voltage

COMMAND	VOUT_MAX															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 format															
Default #	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit [15:0]: Two linear 16 data bytes

VOUT_MARGIN_HIGH (0x25)

This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High.”

COMMAND	VOUT_MARGIN_HIGH															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 format															
Default #	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1

Bit [15:0]: Two linear 16 data bytes

VOUT_MARGIN_LOW (0x26)

This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low.”

COMMAND	VOUT_MARGIN_LOW															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 format															
Default #	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0

Bit [15:0]: Two linear 16 data bytes

VOUT_TRANSITION_RATE (0x27)

VOUT_TRANSITION_RATE command sets the rate in mV/µs at which the output should change voltage.

COMMAND	VIN_ON															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits [15:11]: A 5 bit, two’s complement exponent for the calculation, fixed at -2

Bits [10:0]: An 11 bit, two’s complement mantissa for the calculation

Valid range: 0 to 31.75 mV/ms

VIN_ON (0x35)

The VIN_ON command sets the value of the input voltage, in Volts, at which the unit should start power conversion.

COMMAND	VIN_ON															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0

Bits [15:11]: A 5 bit, two’s complement exponent, fixed at -1.

Bits [10:0]: An 11 bit, two’s complement mantissa

Valid range: 0V to 15.5V

VIN_OFF (0x36)

The VIN_OFF command sets the value of the input voltage, in Volts, at which the unit, once operation has started, should stop power conversion.

COMMAND	VIN_OFF															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1

Bits [15:11]: A 5 bit, two's complement exponent, fixed at -1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0V to 15.5V

VOUT_OV_FAULT_LIMIT (0x40)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured at the sense or output pins that causes an output overvoltage fault.

COMMAND	VOUT_OV_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default #	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1

Bit [15:0]: A 16 bit, two's complement integer

VOUT_OV_FAULT_RESPONSE (0x41)

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault

COMMAND	VOUT_OV_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	1	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption

0x80: Shuts down and does not attempt to restart

0xC0: Shuts down and attempts to restart when the fault condition is no longer present

VOUT_OV_WARN_LIMIT (0x42)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage at the sense or output pins that causes an output voltage high warning. This value is typically less than the output overvoltage threshold.

COMMAND	VOUT_OV_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default #	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0

Bit [15:0]: A 16 bit, two's complement integer

VOUT_UV_WARN_LIMIT (0x43)

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage at the sense or output pins that causes an output voltage low warning. This value is typically greater than the output undervoltage fault threshold.

COMMAND	VOUT_UV_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default #	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1

Bit [15:0]: A 16 bit, two's complement integer

VOUT_UV_FAULT_LIMIT (0x44)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage at the sense or output pins that causes an output undervoltage fault. This fault is masked until the unit reaches the programmed output voltage. This fault is also masked when the unit is disabled.

COMMAND	VOUT_UV_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default #	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0

Bit [15:0]: A 16 bit, two's complement integer

VOUT_UV_FAULT_RESPONSE (0x45)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault

COMMAND	VOUT_UV_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption

0x80: Shuts down and does not attempt to restart

IOUT_OC_FAULT_LIMIT (0x46)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in Amperes, that causes the overcurrent detector to indicate an overcurrent fault condition

COMMAND	IOUT_OC_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0

Bits [15:11]: A 5 bit, two's complement exponent, fixed at -1

Bits [10:0]: An 11 bit, two's complement mantissa

Valid range: 4.5 to 20 A

IOUT_OC_FAULT_RESPONSE (0x47)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault.

COMMAND	IOUT_OC_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	1	1	1	1	1	0	0	0

Valid values:

0xC0: Shuts down and does not attempt to restart

0xF8: Shuts down and attempts to restart continuously

VIN_OV_FAULT_LIMIT (0x55)

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Overvoltage Fault.

COMMAND	VIN_OV_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at 0.

Bit [10:0]: An 11 bit, two's complement mantissa

Maximum value: 18V

VIN_OV_FAULT_RESPONSE (0x56)

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an Input Overvoltage Fault.

COMMAND	VIN_OV_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption

0x80: Shuts down and does not attempt to restart

VIN_UV_WARN_LIMIT (0x58)

The VIN_UV_WARN_LIMIT command sets the value of the input voltage that causes an input voltage low warning. This value is typically greater than the Input Undervoltage Fault threshold, VIN_UV_FAULT_LIMIT

COMMAND	VIN_UV_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at -1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0V to 15.5V

POWER_GOOD_ON (0x5E)

The POWER_GOOD_ON command sets the output voltage at which an optional POWER_GOOD signal should be asserted, indicating that the output voltage is valid. Note that depending on the choice of the device manufacturer that a device may drive a POWER_GOOD signal high or low to indicate that the signal is asserted.

COMMAND	POWER_GOOD_ON															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default #	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0

Bit [15:0]: Two linear16 data bytes

TON_DELAY (0x60)

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise.

COMMAND	TON_DELAY															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at -1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.5ms

TON_RISE (0x61)

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. A value of 0 milliseconds instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible.

COMMAND	TON_RISE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at -2

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.75ms

TON_MAX_FAULT_LIMIT (0x62)

The TON_MAX_FAULT_LIMIT command sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. A value of 0 milliseconds means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely.

COMMAND	TON_MAX_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at -2

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.75ms

TON_MAX_FAULT_RESPONSE (0x63)

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault.

COMMAND	TON_MAX_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption

0x80: Shuts down and does not attempt to restart

Note: When writing to this command, the write must be performed twice in succession for the data to become effective.

TOFF_DELAY (0x64)

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output.

COMMAND	TOFF_DELAY															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at -1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.5ms

TOFF_FALL (0x65)

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-OFF delay time until the voltage is commanded to zero. A value of 0 milliseconds means that the device should ramp the output voltage down as fast as it can.

COMMAND	TOFF_FALL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default #	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at -2

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.75ms

STATUS_BYTE (0x78)

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults.

COMMAND	STATUS_BYTE (LOW BYTE of STATUS_WORD)							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: A fault was declared because the device was busy and unable to respond

Bit [6]: This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled

Bit [5]: An output overvoltage fault has occurred

Bit [4]: An output overcurrent fault has occurred

Bit [3]: An input undervoltage fault has occurred

Bit [2]: A temperature fault or warning has occurred

Bit [1]: A communications, memory or logic fault has occurred

Bit [0]: A fault or warning not listed in bits [7:1] has occurred

STATUS_WORD (0x79)

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

COMMAND	STATUS_WORD (HIGH BYTE of STATUS_WORD)							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: An output voltage fault or warning has occurred

Bit [6]: An output current fault or warning has occurred.

Bit [5]: An input voltage fault or warning has occurred

Bit [4]: A manufacturer specific fault or warning has occurred

Bit [3]: The POWER_GOOD signal, if present, is negated

Bit [2]: A fan or airflow fault or warning has occurred (not used)

Bit [1]: A bit in STATUS_OTHER is set

Bit [0]: A fault type not given in bits [15:1] of the STATUS_WORD has been detected

STATUS_VOUT (0x7A)

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults

COMMAND	STATUS_VOUT							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: OUT_OV_FAULT

Bit [6]: VOUT_OV_WARNING

Bit [5]: VOUT_UV_WARNING

Bit [4]: VOUT_UV_FAULT

Bit [3]: VOUT_MAX_MIN Warning

Bit [2]: TON_MAX_FAULT

Bit [1]: TOFF_MAX_WARNING

Bit [0]: VOUT Tracking Error (not used)

STATUS_IOUT (0x7B)

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.

COMMAND	STATUS_IOUT							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: OUT_OC_FAULT

Bit [6]: IOUT_OC_LV_FAULT

Bit [5]: IOUT_OC_WARNING

Bit [4]: IOUT_UC_FAULT (not used)

Bit [3]: Current Share Fault (not used)

Bit [2]: In Power Limiting Mode (not used)

Bit [1]: POUT_OP_FAULT (not used)

Bit [0]: POUT_OP_WARNING (not used)

STATUS_INPUT (0x7C)

The STATUS_INPUT command returns one byte of information relating to the status of the input-related faults of the converter.

COMMAND	STATUS_INPUT							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: VIN_OV_FAULT

Bit [6]: VIN_OV_WARNING

Bit [5]: VIN_UV_WARNING

Bit [4]: VIN_UV_FAULT

Bit [3]: Unit OFF For Insufficient Input Voltage

Bit [2]: IIN_OC_FAULT (not used)

Bit [1]: IIN_OC_WARNING (not used)

Bit [0]: PIN_OP_WARNING (not used)

STATUS_TEMPERATURE (0x7D)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults.

COMMAND	STATUS_TEMPERATURE							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: OT_FAULT

Bit [6]: OT_WARNING

Bit [5]: UT_WARNING (not used)

Bit [4]: UT_FAULT (not used)

Bit [3:0]: Reserved

STATUS_CML (0x7E)

The STATUS_CML command returns one byte of information relating to the status of the communication-related faults of the converter.

COMMAND	STATUS_CML							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	0	0	0	0	0	0

Bit [7]: Invalid or unsupported command received

Bit [6]: Invalid or unsupported data received

Bit [5]: Packet error check failed (not used)

Bit [4]: Memory fault detected

Bit [3]: Processor fault detected

Bit [2]: Reserved

Bit [1]: A communication fault other than the ones listed in this table has occurred

Bit [0]: Other memory or logic fault has occurred

READ_VIN (0x88)

The READ_VIN command returns two bytes of data in the linear data format that represent the input voltage of the converter.

COMMAND	READ_VIN															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R, Linear 11 format															

Bits [15:11]: A two's complement exponent, -4

Bits [10:0]: An 11 bit two's complement mantissa

READ_VOUT (0x8B)

The READ_VOUT command returns two bytes of data in the linear data format that represent the output voltage of the converter.

COMMAND	READ_VOUT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R, Linear 16 format															

Bits [15:0]: A two's complement mantissa for use with the exponent from VOUT_MODE, -8

READ_TEMPERATURE (0x8D)

The READ_TEMPERATURE command returns the external temperature in degrees Celsius.

COMMAND	READ_TEMPERATURE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R, Linear 11 format															

Bits [15:11]: A two's complement exponent, 0

Bits [10:0]: An 11 bit two's complement mantissa

PMBUS_REVISION (0x98)

PMBUS_REVISION command stores or reads the revision of the PMBus to which the device is compliant.

COMMAND	PMBUS_REVISION							
Bit	7	6	5	4	3	2	1	0
Access	R							
Default #	0	0	1	1	0	0	1	1

Bit [7:4]: Indicate the revision of PMBus specification Part I to which the device is compliant

Bit [3:0]: Indicate the revision of PMBus specification Part II to which the device is compliant

MFR_ID (0x99)

The MFR_ID command is used to either set or read the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer).

COMMAND	MFR_ID															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	Block R/W, 4 bytes															
Default #																

COMMAND	MFR_ID, 4 bytes															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R/W															
Default #																

MFR_MODEL (0x9A)

The MFR_MODEL command is used to either set or read the manufacturer's model number.

COMMAND	MFR_MODEL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R/W, 2 bytes															
Default #																

MFR_REVISION (0x9B)

The MFR_REVISION command is used to either set or read the manufacturer's revision number.

COMMAND	MFR_REVISION															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R 2 bytes															
Default #																

IC_DEVICE_ID (0xAD)

Th IC_DEVICE_ID command is a read-only block-read command that returns 2 bytes with the unique device-code identifier for the device.

COMMAND	IC_DEVICE_ID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R,2 bytes															
Default #																

IC_DEVICE_REV (0xAE)

The IC_DEVICE_REV command is used to read the revision of the IC.

COMMAND	IC_DEVICE_ID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R, 2 bytes															
Default #																

8. List of Registers

Table 8-1. Register List

No.	Name	Adr.	No.	Name	Adr.	No.	Name	Adr.
1	I2C_BASE	0x20	29	VOUT _OV_WARN_LIMIT_LOWER	0x41	57	MFR_ID_COUNT	0x66
2	PMBUS_BASE	0x21	30	VOUT _OV_WARN_LIMIT_UPPER	0x42	58	MFR_ID_1	0x67
3	OPERATION	0x22	31	VOUT _UV_WARN_LIMIT_LOWER	0x43	59	MFR_ID_2	0x68
4	ON_OFF_CONFIG	0x23	32	VOUT _UV_WARN_LIMIT_UPPER	0x44	60	MFR_ID_3	0x69
5	WRITE_PROTECT	0x24	33	VOUT _UV_FAULT_LIMIT_LOWER	0x45	61	MFR_MODEL_COUNT	0x6A
6	MASK_BYTE_VOUT	0x25	34	VOUT _UV_FAULT_LIMIT_UPPER	0x46	62	MFR_MODEL	0x6B
7	MASK_BYTE_IOUT	0x26	35	VOUT _UV_FAULT_RESPONSE	0x47	63	MFR_REVISION_COUNT	0x6C
8	MASK_BYTE_INPUT	0x27	36	IOUT_OC_FAULT_LIMIT_LOWER	0x48	64	MFR_REVISION	0x6D
9	MASK_BYTE_TEMP	0x28	37	IOUT_OC_FAULT_LIMIT_UPPER	0x49	65	CAPABILITY	0x6E
10	MASK_BYTE_CML	0x29	38	IOUT_OC_FAULT_RESPONSE	0x4A	66	BUS_VOLTAGE	0x7A
11	VOUT_MODE	0x2B	39	VIN_OV_FAULT_LIMIT_LOWER	0x52	67	OTP_ON	0x89
12	VOUT_COMMAND_LOWER	0x2C	40	VIN_OV_FAULT_LIMIT_UPPER	0x53	68	CLEAR_STATUS	0x8C
13	VOUT_COMMAND_UPPER	0x2D	41	VIN_OV_FAULT_RESPONSE	0x54	69	USER_OTP_POINTER	0x92
14	VOUT_MAX_LOWER	0x2E	42	VIN_UV_WARN_LIMIT_LOWER	0x55	70	STATUS	0x93
15	VOUT_MAX_UPPER	0x2F	43	VIN_UV_WARN_LIMIT_UPPER	0x56	71	IC_REV_BYTE_COUNT	0x94
16	VOUT_MARGIN_HIGH_LOWER	0x30	44	POWER_GOOD_ON_LOWER	0x57	72	IC_REV	0x95
17	VOUT_MARGIN_HIGH_UPPER	0x31	45	POWER_GOOD_ON_UPPER	0x58	73	IC_DEV_ID_COUNT	0x96
18	VOUT_MARGIN_LOW_LOWER	0x32	46	TON_DELAY_LOWER	0x5B	74	IC_DEV_ID	0x97
19	VOUT_MARGIN_LOW_UPPER	0x33	47	TON_DELAY_UPPER	0x5C	75	PVIN_REPORT_LOWER	0x9A
20	VOUT_TRANSITION_RATE_LOWER	0x34	48	TON_RISE_LOWER	0x5D	76	PVIN_REPORT_UPPER	0x9B
21	VOUT_TRANSITION_RATE _UPPER	0x35	49	TON_RISE_UPPER	0x5E	77	VOUT_REPORT_LOWER	0xA0
22	VIN_ON_LOWER	0x38	50	TON_MAX_FAULT_LIMIT_LOWER	0x5F	78	VOUT_REPORT_UPPER	0xA1
23	VIN_ON _UPPER	0x39	51	TON_MAX_FAULT_LIMIT_UPPER	0x60	79	TEMP_REPORT_LOWER	0xA2
24	VIN_OFF_LOWER	0x3A	52	TON_MAX_FAULT_RESPONSE	0x61	80	TEMP_REPORT_UPPER	0xA3
25	VIN_OFF _UPPER	0x3B	53	TOFF_DELAY_LOWER	0x62	81	VCC_REPORT_LOWER	0xA4
26	VOUT_OV_FAULT_LIMIT_LOWER	0x3E	54	TOFF_DELAY_UPPER	0x63	82	VCC_REPORT_UPPER	0xA5
27	VOUT _OV_FAULT_LIMIT_UPPER	0x3F	55	TOFF_FALL_LOWER	0x64	83	ADDR_REPORT_LOWER	0xA6
28	VOUT _OV_FAULT_RESPONSE	0x40	56	TOFF_FALL_UPPER	0x65	84	ADDR_REPORT_UPPER	0xA7

I2C_BASE (0x20)

Use	I2C Base address							
Bit	7	6	5	4	3	2	1	0
Access		R/W						
Default #	X	0	0	0	1	0	0	0

Bit [7]: Not used

Bits [6:0]: Base address for register level I2C access

PMBUS_BASE (0x21)

Use	PMBus Base address							
Bit	7	6	5	4	3	2	1	0
Access		R/W						
Default #	X	1	1	1	0	0	0	0

Bit [7]: Not used

Bits [6:0]: Base address for PMBUS access

OPERATION (0x22)
For a description of this register contents, see the OPERATION command in the PMBus Commands section.

ON_OFF_CONFIG (0x23)
For a description of this register content, see the ON_OFF_CONFIG command in the PMBus Commands section.

WRITE_PROTECT (0x24)
For a description of this register contents, see the WRITE_PROTECT command in the PMBus Commands section. Note that the protections in this register only apply to PMBus access. All access is always available via the direct register level I2C access.

MASK_BYTE_VOUT (0x25)
This register contains the mask byte applied to the STATUS_VOUT register using the SMBALERT_MASK command.

MASK_BYTE_IOUT (0x26)
This register contains the mask byte applied to the STATUS_IOUT register using the SMBALERT_MASK command.

MASK_BYTE_INPUT (0x27)
This register contains the mask byte applied to the STATUS_INPUT register using the SMBALERT_MASK command.

MASK_BYTE_TEMP (0x28)
This register contains the mask byte applied to the STATUS_TEMP register using the SMBALERT_MASK command.

MASK_BYTE_CML (0x29)
This register contains the mask byte applied to the STATUS_CML register using the SMBALERT_MASK command.

VOUT_MODE (0x2B)
For a description of this register contents, see the VOUT_MODE command in the PMBus Commands section.

VOUT_COMMAND_LOWER (0x2C)
For a description of this register contents, see the VOUT_COMMAND command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_COMMAND_UPPER (0x2D)
For a description of this register contents, see the VOUT_COMMAND command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_MAX_LOWER (0x2E)
For a description of this register contents, see the VOUT_MAX command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_MAX_UPPER (0x2F)
For a description of this register contents, see the VOUT_MAX command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_MARGIN_HIGH_LOWER (0x30)
For a description of this register contents, see the VOUT_MARGIN_HIGH command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_MARGIN_HIGH_UPPER (0x31)
For a description of this register contents, see the VOUT_MARGIN_HIGH command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_MARGIN_LOW_LOWER (0x32)
For a description of this register contents, see the VOUT_MARGIN_LOW command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_MARGIN_LOW_UPPER (0x33)
For a description of this register contents, see the VOUT_MARGIN_LOW command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_TRANSITION_RATE_LOWER (0x34)
For a description of this register contents, see the VOUT_TRANSITION_RATE command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_TRANSITION_RATE _UPPER (0x35)
For a description of this register contents, see the VOUT_ TRANSITION_RATE command in the PMBus Commands section. This register contains the high byte of the data for that command.

VIN_ON_LOWER (0x38)
For a description of this register contents, see the VIN_ON command in the PMBus Commands section. This register contains the low byte of the data for that command.

VIN_ON _UPPER (0x39)
For a description of this register contents, see the VIN_ON command in the PMBus Commands section. This register contains the high byte of the data for that command.

VIN_OFF_LOWER (0x3A)
For a description of this register contents, see the VIN_OFF command in the PMBus Commands section. This register contains the low byte of the data for that command.

VIN_OFF _UPPER (0x3B)
For a description of this register contents, see the VIN_OFF command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_OV_FAULT_LIMIT_LOWER (0x3E)
For a description of this register contents, see the VOUT_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT _OV_FAULT_LIMIT_UPPER (0x3F)
For a description of this register contents, see the VOUT_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT _OV_FAULT_RESPONSE (0x40)
For a description of this register contents, see the VOUT_OV_FAULT_RESPONSE command in the PMBus Commands section.

VOUT _OV_WARN_LIMIT_LOWER (0x41)
For a description of this register contents, see the VOUT_OV_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT _OV_WARN_LIMIT_UPPER (0x42)
For a description of this register contents, see the VOUT_ OV_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT _UV_WARN_LIMIT_LOWER (0x43)
For a description of this register contents, see the VOUT_UV_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT _UV_WARN_LIMIT_UPPER (0x44)
For a description of this register contents, see the VOUT_ UV_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT _UV_FAULT_LIMIT_LOWER (0x45)
For a description of this register contents, see the VOUT_UV_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT _UV_FAULT_LIMIT_UPPER (0x46)
For a description of this register contents, see the VOUT_ UV_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT _UV_FAULT_RESPONSE (0x47)
For a description of this register contents, see the VOUT_UV_FAULT_RESPONSE command in the PMBus Commands section.

IOUT_OC_FAULT_LIMIT_LOWER (0x48)
For a description of this register contents, see the IOUT_OC_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

IOUT_OC_FAULT_LIMIT_UPPER (0x49)
For a description of this register contents, see the IOUT_OC_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

IOUT_OC_FAULT_RESPONSE (0x4A)
For a description of this register contents, see the IOUT_OC_FAULT_RESPONSE command in the PMBus Commands section.

VIN_OV_FAULT_LIMIT_LOWER (0x52)
For a description of this register contents, see the VIN_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VIN_OV_FAULT_LIMIT_UPPER (0x53)
For a description of this register contents, see the VIN_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

VIN_OV_FAULT_RESPONSE (0x54)
For a description of this register contents, see the VIN_OV_FAULT_RESPONSE command in the PMBus Commands section.

VIN_UV_WARN_LIMIT_LOWER (0x55)
For a description of this register contents, see the VIN_UV_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VIN_UV_WARN_LIMIT_UPPER (0x56)
For a description of this register contents, see the VIN_UV_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

POWER_GOOD_ON_LOWER (0x57)
For a description of this register contents, see the POWER_GOOD_ON command in the PMBus Commands section. This register contains the low byte of the data for that command.

POWER_GOOD_ON_UPPER (0x58)
For a description of this register contents, see the POWER_GOOD_ON command in the PMBus Commands section. This register contains the high byte of the data for that command.

TON_DELAY_LOWER (0x5B)
For a description of this register contents, see the TON_DELAY command in the PMBus Commands section. This register contains the low byte of the data for that command.

TON_DELAY_UPPER (0x5C)
For a description of this register contents, see the TON_DELAY command in the PMBus Commands section. This register contains the high byte of the data for that command.

TON_RISE_LOWER (0x5D)
For a description of this register contents, see the TON_RISE command in the PMBus Commands section. This register contains the low byte of the data for that command.

TON_RISE_UPPER (0x5E)
For a description of this register contents, see the TON_RISE command in the PMBus Commands section. This register contains the high byte of the data for that command.

TON_MAX_FAULT_LIMIT_LOWER (0x5F)
For a description of this register contents, see the TON_MAX_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command.

TON_MAX_FAULT_LIMIT_UPPER (0x60)
For a description of this register contents, see the TON_MAX_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command.

TON_MAX_FAULT_RESPONSE (0x61)
For a description of this register contents, see the TON_MAX_FAULT_RESPONSE command in the PMBus Commands section.

Note: When writing to this register, the write must be performed twice in succession for the data to become effective.

TOFF_DELAY_LOWER (0x62)
For a description of this register contents, see the TOFF_DELAY command in the PMBus Commands section. This register contains the low byte of the data for that command.

TOFF_DELAY_UPPER (0x63)
For a description of this register contents, see the TOFF_DELAY command in the PMBus Commands section. This register contains the high byte of the data for that command.

TOFF_FALL_LOWER (0x64)

For a description of this register contents, see the TOFF_FALL command in the PMBus Commands section. This register contains the low byte of the data for that command.

TOFF_FALL_UPPER (0x65)

For a description of this register contents, see the TOFF_FALL command in the PMBus Commands section. This register contains the high byte of the data for that command.

MFR_ID_COUNT (0x66)

COMMAND	MFD_ID_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	1	1

This register does not have a direct PMBus counterpart but is used in the PMBus MFR_ID command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there are only 3 data bytes available for the MFR_ID command.

MFR_ID_1 (0x67)

This register contains the first byte used in the PMBus MFR_ID command.

MFR_ID_2 (0x68)

This register contains the second byte (if used) in the PMBus MFR_ID command.

MFR_ID_3 (0x69)

This register contains the third byte (if used) in the PMBus MFR_ID command.

MFR_MODEL_COUNT (0x6A)

COMMAND	MFR_MODEL_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus MFR_ID command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the MFR_MODEL command.

MFR_MODEL (0x6B)

This register contains the byte used in the PMBus MFR_MODEL command.

MFR_REVISION_COUNT (0x6C)

COMMAND	MFR_REVISION_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Default #	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus MFR_REVISION command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the MFR_MODEL command.

MFR_REVISION (0x6D)

This register contains the byte used in the PMBus MFR_REVISION command.

CAPABILITY (0x6E)

For a description of this register contents, see the CAPABILITY command in the PMBus Commands section. This register contains the low byte of the data for that command.

BUS_VOLTAGE (0x7A)

COMMAND	BUS_VOLTAGE							
Bit	7	6	5	4	3	2	1	0
Access	Reserved	Reserved	Reserved	R/W	R/W	R/W	Reserved	Reserved
Default #	1	1	1	1	1	1	0	0

This register sets the bus voltage for the I^2C bus.

Bit [4]:

0: Enable PLL, Mode B

1: Disable PLL, Mode A (default)

Bit [3]:

0: Power Good based on POWER_GOOD_ON command value

1: Power Good based on DAC (Default)

Bit [2]:

0: 1.8V to 2.5V

1: 3.3V to 5V

All other bits are reserved.

OTP_ON (0x89)

COMMAND	OTP_ON							
Bit	7	6	5	4	3	2	1	0
Access	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/W	Reserved
Default #	1	1	1	1	1	1	0	0

This register sets the bus voltage for the I^2C bus.

Bit [1]:

0: Do not initiate write of user memory

1: Initiate write of user memory

Bit [0] is reserved.

All other bits are unused.

CLEAR_STATUS (0x8C)

COMMAND	OTP_ON							
Bit	7	6	5	4	3	2	1	0
Access	Reserved	Unused	Unused	Unused	Unused	Reserved	Reserved	R/W
Default #	1	1	1	1	1	1	0	0

This register sets the bus voltage for the I^2C bus.

Bit [0]:

0: Do not clear status flags

1: Clear status flags

Bits [7] and [2] are reserved.

All other bits are unused.

USER_OTP_POINTER (0x92)

COMMAND	USER_OTP_POINTER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	Unused	Unused	Unused	Unused
Default #	0	0	1	0				

This register shows the number of remaining write allowed to the user NVM area.

Bits [7:4]:

0001: 9 writes remaining

0010: 8 writes remaining (default after factory trimming and initial setup)

0011: 7 writes remaining

0100: 6 writes remaining

0101: 5 writes remaining

0110: 4 writes remaining

0111: 3 writes remaining

1000: 2 writes remaining

1001: 1 write remaining

1010: 0 writes remaining

Bits [3:0] are unused.

STATUS (0x93)

COMMAND	STATUS							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #								

This register shows the status flags for the part.

Bit [7]: Power Good status

Bit [6]: Overvoltage status

Bit [5]: Overcurrent status

Bit [4]: Temperature status

Bit [3]: Enable pin status

Bit [2]: Not used

Bit [1]: User NVM write status

Bit [0]: Status cleared indicator. This is a mirror of register 0x8C, bit 0.

IC_REV_BYTE_COUNT (0x94)

COMMAND	IC_REV_BYTE_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus IC_DEVICE_REV command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the IC_DEVICE_REV command.

IC_REV (0x95)

This register contains the byte used in the PMBus IC_DEVICE_REV command.

IC_DEV_ID_COUNT (0x96)

COMMAND	IC_DEV_ID_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus IC_DEVICE_ID command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the IC_DEVICE_REV command.

IC_DEV_ID (0x97)

This register contains the byte used in the PMBus IC_DEVICE_ID command.

PVIN_REPORT_LOWER (0x9A)

For a description of this register contents, see the READ_VIN command in the PMBus Commands section. This register contains the low byte of the data for that command.

PVIN_REPORT_UPPER (0x9B)

For a description of this register contents, see the READ_VIN command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_REPORT_LOWER (0xA0)

For a description of this register contents, see the READ_VOUT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_REPORT_UPPER (0xA1)

For a description of this register contents, see the READ_VOUT command in the PMBus Commands section. This register contains the high byte of the data for that command.

TEMP_REPORT_LOWER (0xA2)

For a description of this register contents, see the READ_TEMPERATURE command in the PMBus Commands section. This register contains the low byte of the data for that command.

TEMP_REPORT_UPPER (0xA3)

For a description of this register contents, see the READ_TEMPERATURE command in the PMBus Commands section. This register contains the high byte of the data for that command.

VCC_REPORT_LOWER (0xA4)

COMMAND	VCC_REPORT_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #								

This register contains the low byte of a linear 11 format representation of the VCC voltage of the part.

VCC_REPORT_UPPER (0xA5)

COMMAND	VCC_REPORT_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #	1	1	0	1	1			

This register contains the high byte of a linear 11 format representation of the VCC voltage of the part. The exponent for this calculation, with a value of -5, is in bits [7:3].

ADDR_REPORT_LOWER (0xA6)

COMMAND	ADDR_REPORT_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #	0	0	0	0	0	0	0	0

This register contains the low byte of the result of the ADC converter that looks at the ADDR pin for determining the address offset to apply to the base addresses for both PMBus and direct register access.

ADDR_REPORT_UPPER (0xA7)

COMMAND	ADDR_REPORT_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default #	0	0	0	0	0	0	0	0

This register contains the high byte of the result of the ADC converter that looks at the ADDR pin for determining the address offset to apply to the base addresses for both PMBus and direct register access.

9. Programming the OTP

In order to program the OTP, complete the following steps:

1. Write and verify that all registers contain the desired values.
2. Read register 0x92 [7:4] to determine the number of remaining user banks available for writing:

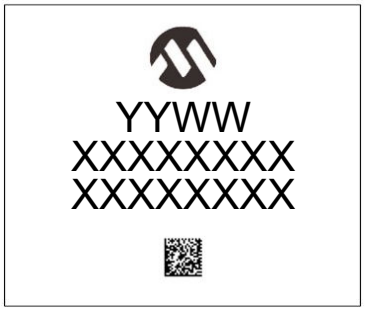
Register 0x92 [7:4] Value	Remaining Writes
0001	9
0010	8
0011	7
0100	6
0101	5
0110	4
0111	3
1000	2
1001	1
1010	0

3. If there is an available bank, apply 7.5V (±250 mV) to the VIN pin. If not, stop. The part cannot have the OTP burned with new values.
4. Write 0 then 1 to register 0x89 [1].
5. Read register 0x93 and check bit [2]. If it is set, the write was successful. If not, the write failed.
6. If the write was successful, power cycle VIN.
7. Read all registers and compare with expected values.
8. If steps 5 or 7 fail, repeat steps 1 through 4.
9. If there is another failure of steps 5 or 7, discard the part.

10. Package Information

Package Marking Information

22-Pin LGA 5.8 mm x 4.9 mm:



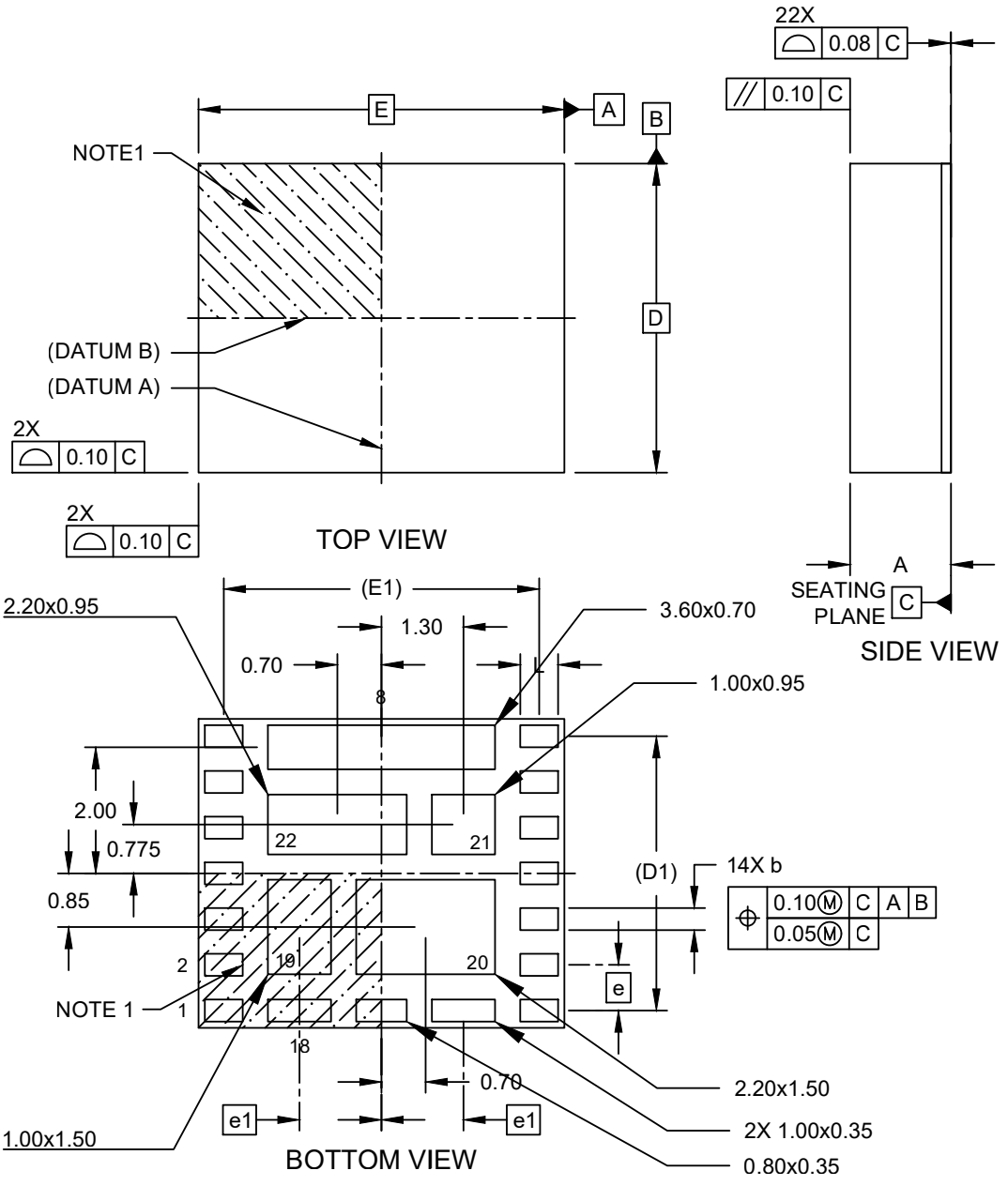
Example:

Note: The MCPF1412M06 is engineered for compatibility with standard surface-mount technology (SMT) assembly methods. It features a raised footprint, with pads elevated above the surrounding substrate. The pads are finished with ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold). Due to these characteristics, the MCPF1412M06 performs exceptionally well in lead-free environments. The surface wets easily, and the raised footprint accommodates processing variations.

Package Outline Drawing

22-Lead Land Grid Array 5.8x4.9x1.71mm (8FW) [LGA] - System in Package [SIP]

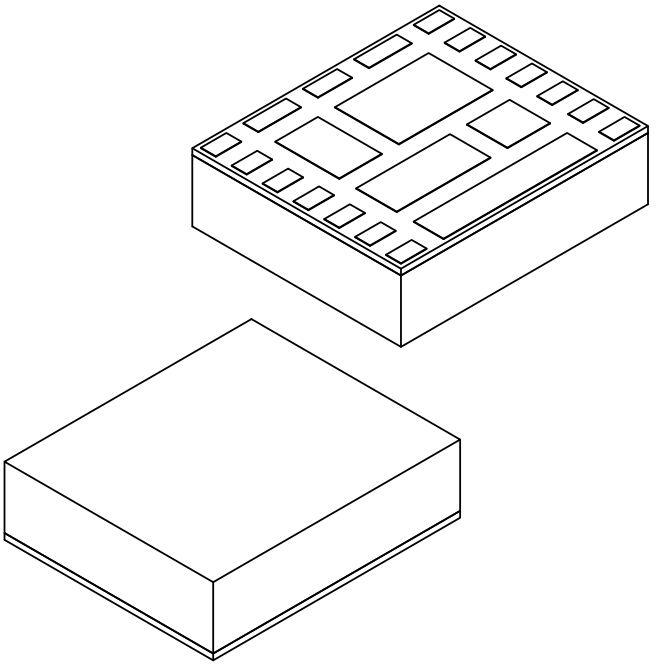
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00660 Rev B Sheet 1 of 2

22-Lead Land Grid Array 5.8x4.9x1.71mm (8FW) [LGA] - System in Package [SIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		22	
Pitch	e		0.725 BSC	
Pitch	e1		1.300 BSC	
Overall Height	A	1.41	1.56	1.71
Overall Length	D		4.90 BSC	
Lead Pad Length Pitch	D1		4.35 REF	
Overall Width	E		5.80 BSC	
Lead Pad Width Pitch	E1		5.00 REF	
Terminal Width	b	0.30	0.35	0.40
Terminal Length	L	0.55	0.60	0.65

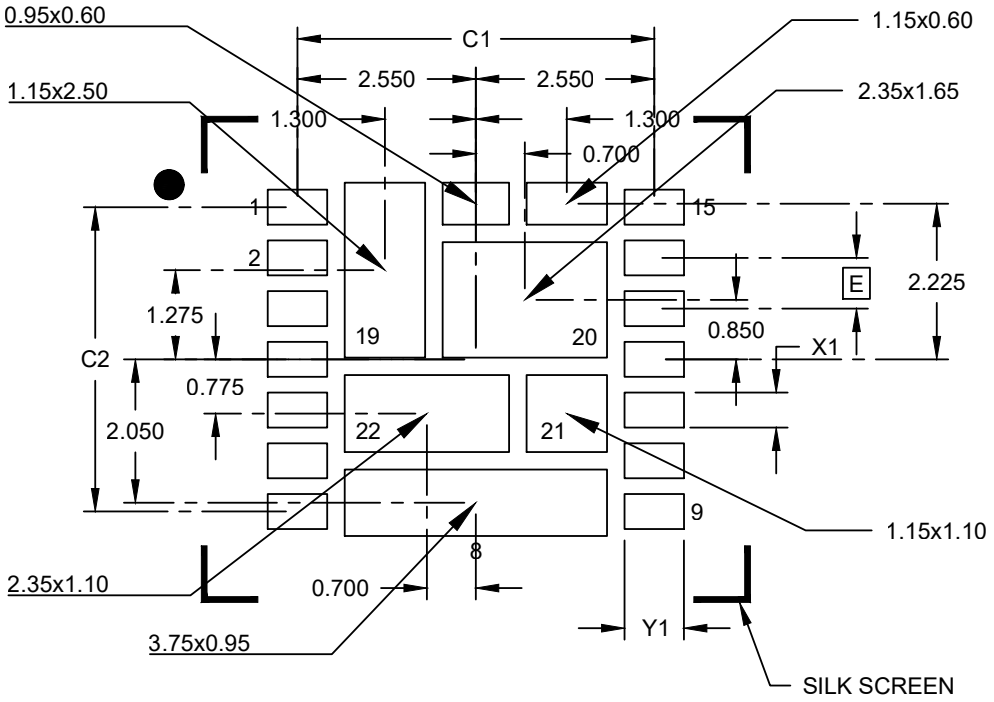
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerances, for information purposes only.

Microchip Technology Drawing C04-00660 Rev B Sheet 2 of 2

22-Lead Land Grid Array 5.8x4.9x1.71mm (8FW) [LGA] - System in Package [SIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.725 BSC	
Contact Pad Spacing	C1		5.10	
Contact Pad Spacing	C2		4.35	
Contact Pad Width (X14)	X1			0.50
Contact Pad Length (X14)	Y1			0.85

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, pleease refer to current industry standard IPC-7093.

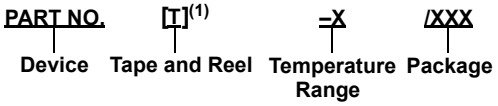
Microchip Technology Drawing C04-02660 Rev B

11. Revision History

Doc. Rev.	Date	Section	Comments
A	April 2025		Initial release of this document.

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device:	MCPF1412M06: 16V, 12A Switching Buck Regulator Module	
Tape & Reel Option(1):	Blank	= Tube
	T	= Tape & Reel
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	8FW	= Low-Profile Land Grid Array (LGA), 22-Pin, 5.8 x 4.9 x 1.71 mm

Examples:

- MCPF1412M06T-E/8FW : 16V, 12A Switching Buck Regulator Module, Tape and Reel, Extended temperature, LGA 22-Pin package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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