Standard LCD Segment Driver

BU9797FUV MAX 144 Segments (SEG36×COM4)

Features

- Integrated RAM for Display Data (DDRAM): 36 x 4 bit (Max 144 Segment)
- LCD Drive Output: 4 Common Output, Max 36 Segment Output
- Integrated Buffer AMP for LCD Driving
- Integrated Oscillator Circuit
- No External Components
- Low Power Consumption Design

Key Specifications

- Supply Voltage Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 144Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 2wire serial interface

Package W (Typ) x D (Typ) x H (Max)

Applications

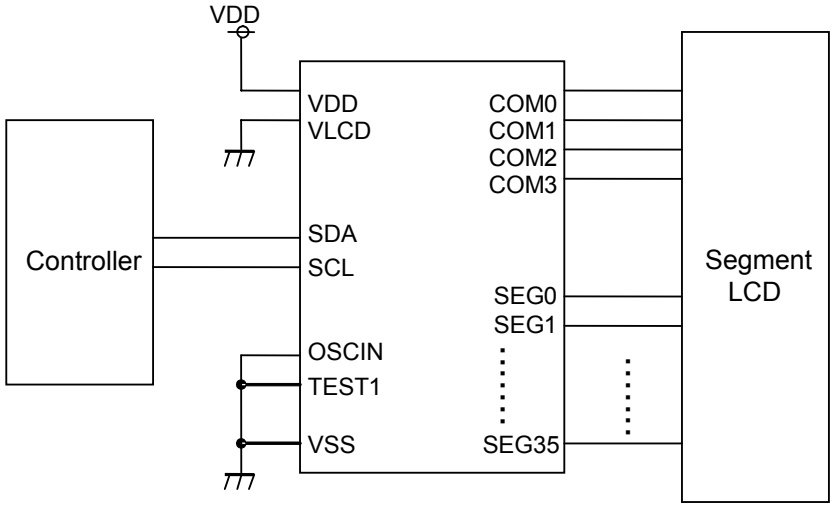
- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment

Etc.



TSSOP-C48V
8.1mm x 12.5mm x 1.0mm

Typical Application Circuit



Using internal oscillator

Figure 1. Typical application circuit

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Block Diagram / Pin Configuration / Pin Description

BU9797FUV

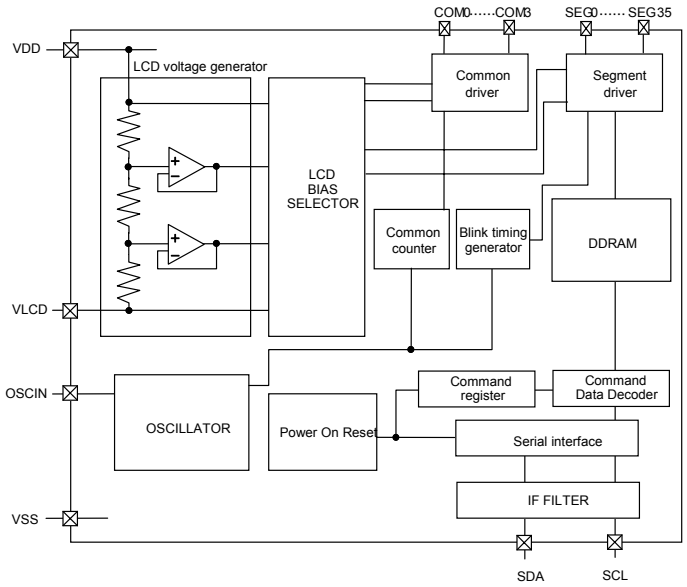


Figure 2. Block Diagram

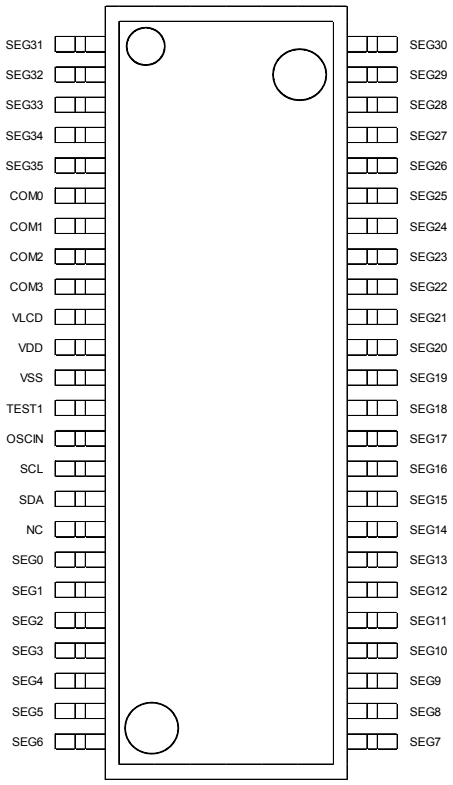


Figure 3. Pin Configuration (TOP VIEW)

Table 1. Pin Description

Pin Name	Pin No.	I/O	Function
TEST1	13	I	Test input (ROHM use only) Must be connect to VSS
NC	17		OPEN terminal
OSCIN	14	I	External clock input External clock and Internal clock can be selected by command Must be connect to VSS when use internal oscillator
SDA	16	I/O	Serial data in-out terminal
SCL	15	I	Serial clock for data transfer terminal
VSS	12		Ground
VDD	11		Power supply
VLCD	10		Power supply for LCD driving
SEG0 to 35	18-48, 1-5	O	SEGMENT output for LCD driving
COM0 to 3	6-9	O	COMMON output for LCD driving

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Absolute Maximum Ratings (Ta=25°C, VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 to VDD	V	LCD drive voltage
Power Dissipation	Pd	0.64	W	When use more than Ta=25°C, subtract 6.4mW per degree. (Package only)
Input Voltage Range	VIN	-0.5 to VDD+0.5	V	
Operational Temperature Range	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +125	°C	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +85°C, VSS=0V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	0	-	VDD-2.4	V	LCD drive voltage, VDD-VLCD ≥ 2.4V

Electrical Characteristics

DC Characteristics (VDD=2.5V to 5.5V, VLCD=0V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
"H" Level Input Voltage		V_{IH}	0.7VDD	-	VDD	V	SDA,SCL
"L" Level Input Voltage		V_{IL}	VSS	-	0.3VDD	V	SDA,SCL
"H" Level Input Current		I_{IH}	-	-	1	μA	SDA,SCL
"L" Level Input Current		I_{IL}	-1	-	-	μA	SDA,SCL
SDA "L" Level Output Voltage		V_{OL_sda}	0	-	0.4	μA	Iload = 3mA
LCD Driver On Resistance	SEG	R_{ON}	-	3	-	KΩ	Iload=±10μA
	COM	R_{ON}	-	3	-	kΩ	
Standby Current		I_{DD1}	-	-	5	μA	Display off, Oscillation off
Operating Power Consumption		I_{DD2}	-	7.5	20	μA	VDD=3.3V, VLCD=0V, Ta=25°C Power save mode1, FR=71Hz 1/3 bias, Frame inverse

Oscillation Characteristics (VDD=2.5V to 5.5V, VLCD=0V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Frame Frequency1	f_{CLK1}	56	80	104	Hz	FR = 80Hz setting, VDD=2.5V to 5.5V, Ta=-40°C to 85°C
Frame Frequency2	f_{CLK2}	70	80	90	Hz	FR = 80Hz setting, VDD=3.5V, Ta=25°C
Frame Frequency3	f_{CLK3}	77.5	87.5	97.5	Hz	FR = 80Hz setting, VDD=5.0V, Ta=25°C
Frame Frequency4	f_{CLK4}	67.5	87.5	102	Hz	FR = 80Hz setting, VDD=5.0V, Ta=-40°C to 85°C
External Frequency	f_{EXCLK}	15	-	300	KHz	External clock use case (Note1)

(Note1) <Frame frequency calculation at external clock mode>
DISCTL 80HZ setting: Frame frequency [Hz] = external clock [Hz] ÷ 512
DISCTL 71HZ setting: Frame frequency [Hz] = external clock [Hz] ÷ 576
DISCTL 64HZ setting: Frame frequency [Hz] = external clock [Hz] ÷ 648
DISCTL 53HZ setting: Frame frequency [Hz] = external clock [Hz] ÷ 768

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Electrical Characteristics - continued

MPU interface Characteristics (VDD=2.5V to 5.5V, VLCD=0V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input Rise Time	tr	-	-	0.3	µs	
Input Fall Time	tf	-	-	0.3	µs	
SCL Cycle Time	tSCYC	2.5	-	-	µs	
“H” SCL Pulse Width	tSHW	0.6	-	-	µs	
“L” SCL Pulse Width	tSLW	1.3	-	-	µs	
SDA Setup Time	tSDS	100	-	-	µs	
SDA Hold Time	tSDH	100	-	-	us	
Buss Free Time	tBUF	1.3	-	-	µs	
START Condition Hold Time	tHD;STA	0.6	-	-	µs	
START Condition Setup Time	tSU;STA	0.6	-	-	µs	
STOP Condition Setup Time	tSU;STO	0.6	-	-	µs	

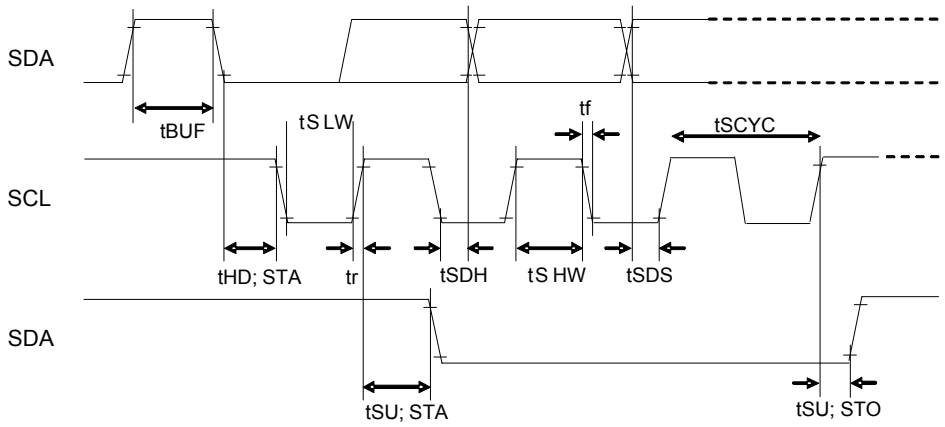


Figure 4. Interface Timing

I/O equivalence circuit

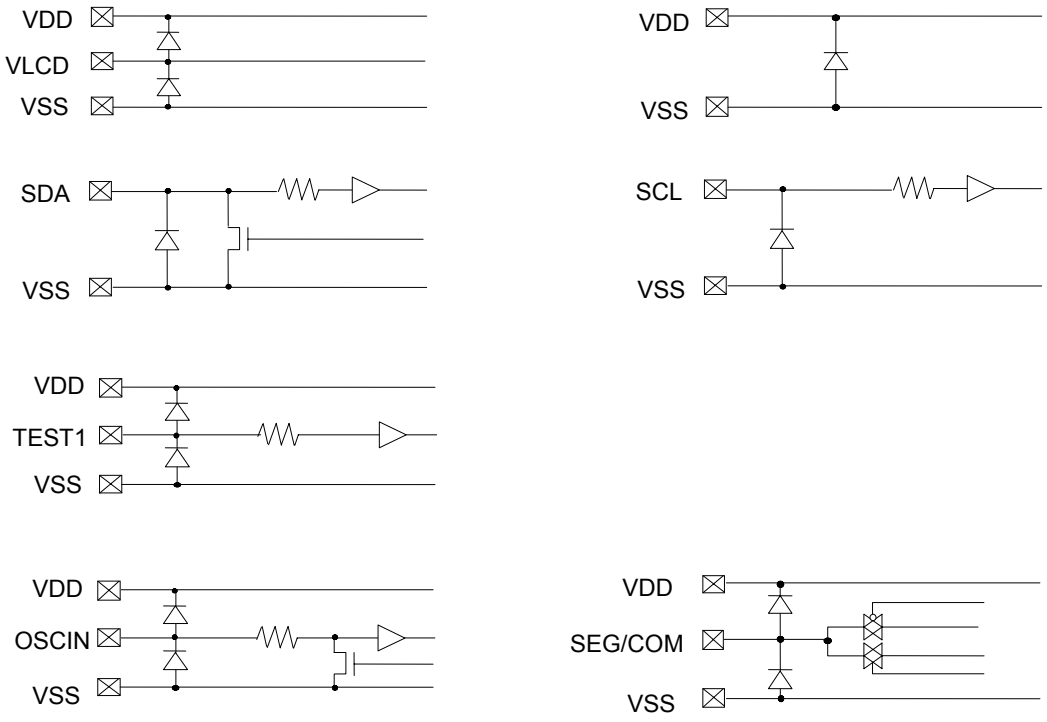
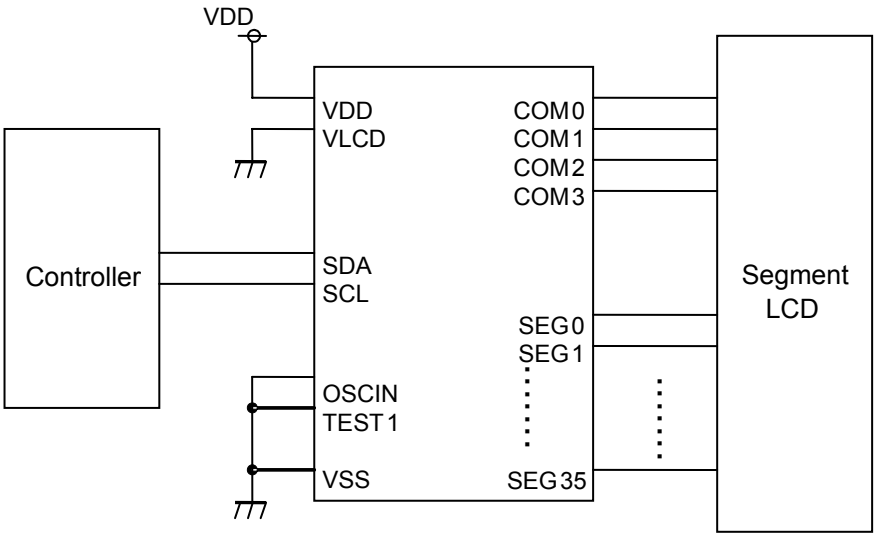


Figure 5. I/O equivalence circuit

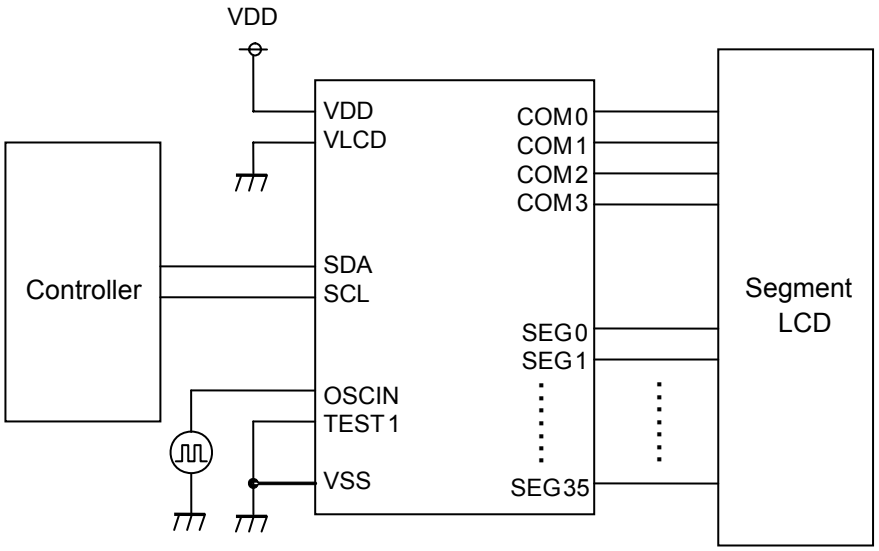
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Example of recommended circuit



Internal Oscillator circuit mode



External clock input mode

Figure 6. Example of recommended circuit

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Functional descriptions

Command /Data transfer method

This device is controlled by 2wire signal (SDA, SCL).

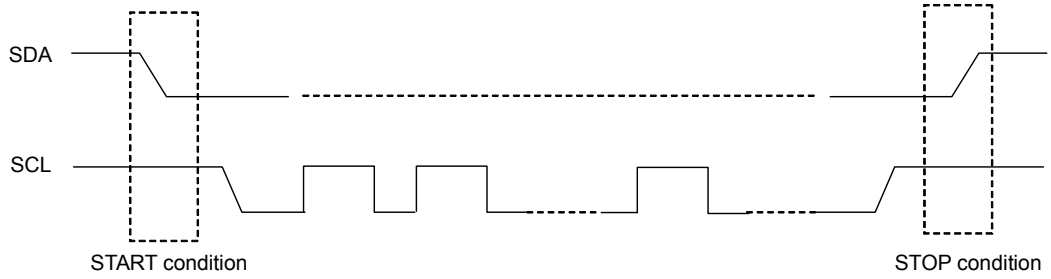


Figure 7. 2 wire Command/Data transfer Format

It has to generate the condition such as START condition and STOP condition in 2wire serial interface transfer method.

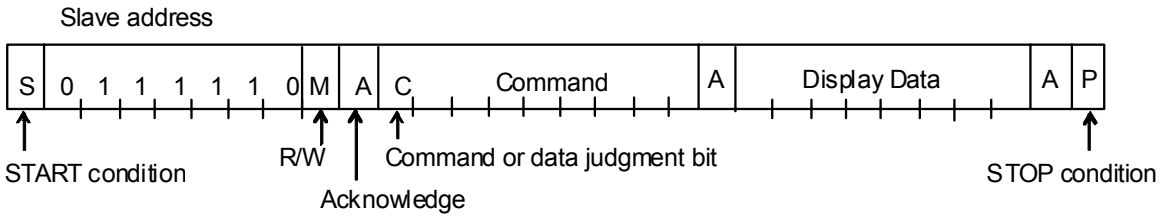


Figure 8. Interface protcol

Method of how to transfer command and data is shown as follows.

(1) Generate “START condition”.
(2) Issue Slave address.
(3) Transfer command and display data.

Acknowledge (ACK)

Data format is 8bits and return Acknowledge after transfer 8bits data.
When SCL 8th=’L’ after transfer 8bit data (Slave Address, Command, Display Data), output ’L’ and open SDA line.
When SCL 9th=’L’, stop output function.
(As Output format is NMOS-Open-Drain, can’t output ‘H’ level.)
If no need Acknowledge function, please input ‘L’ level from SCL 8th=’L’ to SCL 9th=’L’.

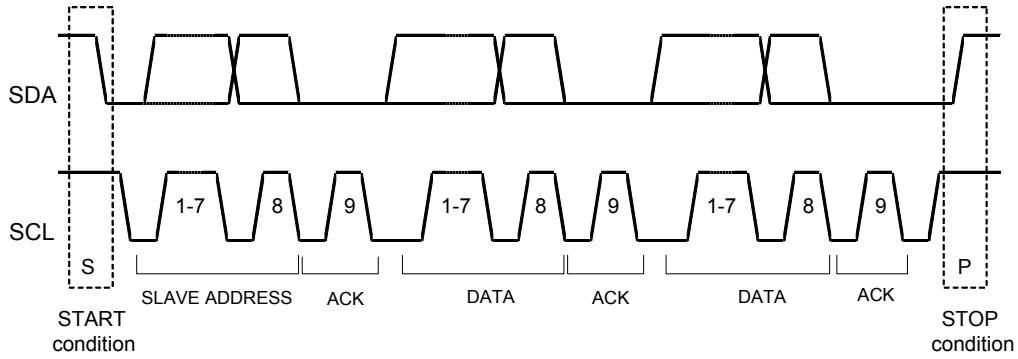


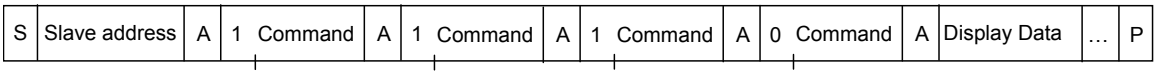
Figure 9. Acknowledge timing

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Command transfer method

Issue Slave Address (“01111100” for Write Mode or “01111101” for Read Mode) after generate “START condition”.
1byte after Slave Address always becomes command input.
The least significant bit (LSB” of the Slave Address determines if the operation to be done is Write or Read operation.
MSB (“command or data judge bit”) of command decide to next data is command or display data.
When set “command or data judge bit”=‘1’, next byte will be command.
When set “command or data judge bit”=‘0’, next byte data is display data.

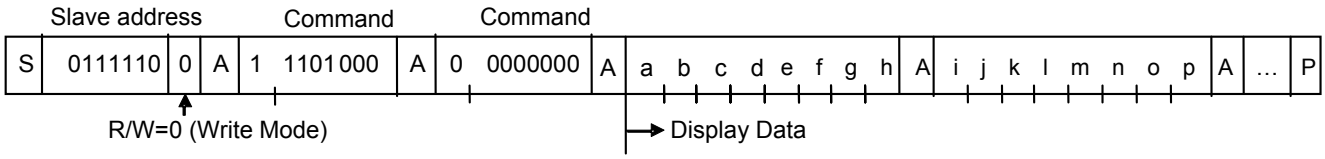


Once it becomes display data transfer condition, it cannot input command.
When want to input command again, please generate “START condition” once.
If “START condition” or “STOP condition” are inputted in the middle of command transmission, command will be canceled.
If Slave address is continuously inputted following “START condition”, it will be in command input condition.
Please input “Slave Address” in the first data transmission after “START condition”.
When Slave Address cannot be recognized in the first data transmission, Acknowledge does not return and next transmission will be invalid. When data transmission is in invalid status, if “START conditions” are transmitted again, it will return to valid status.

Please consider the MPU interface characteristic such as Input rise time and Setup/Hold time when transferring command and data (Refer to MPU Interface).

Write display and transfer method

Set R/W bit to “0” to come into Write Mode.
This device has Display Data RAM (DDRAM) of 36×4=144bit.
The relationship between data input and display data, DDRAM data and address are as follows;



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.
Data can be continuously written in DDRAM by transmitting Data continuously.
(When RAM data is written successively after writing RAM data to 23h (SEG35), the address is returned to 00h (SEG0) by the auto-increment function.

DDRAM address

BIT	00	01	02	03	04	05	06	07	・・・	21h	22h	23h	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG33	SEG34	SEG35	

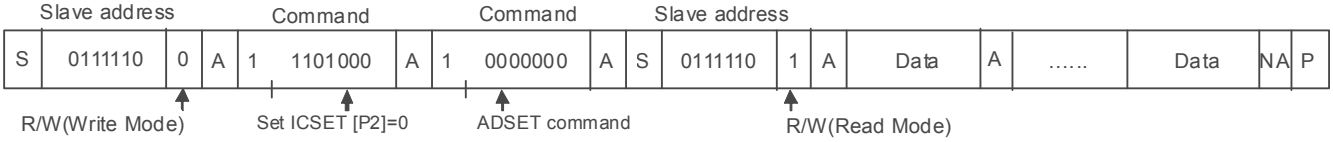
Data transference to DDRAM will be executed in every 4bit data.
So it will be finished to transfer with no need to wait ACK.

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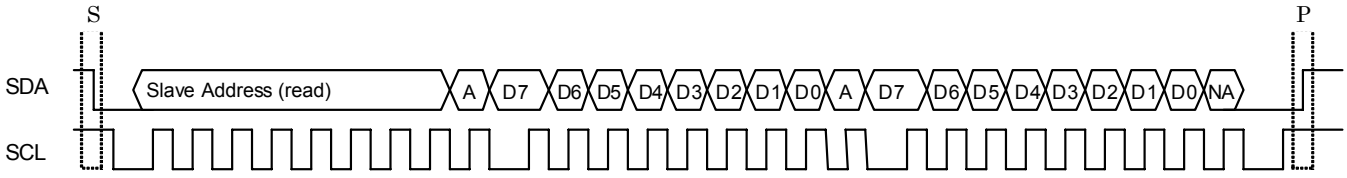
Read Display Data and Transfer Method

If the LSB of the slave address is “1”, it will be set read mode.
The display data and command register value can be read during read mode.
The read mode sequence is shown below.



During read mode, the display data can be read from the DDRAM through the SDA line.
The data will output with SCL input synchronous.
First it has to set address by write mode ADSET command to read display data.
If DDRAM address does not specify before DDRAM read, the read address will be start from the current DDRAM address.
Address will be increment +2 addresses by 8bit data output automatically.
Master side should be output ACK output by each 8bit data output.
It will be able to keep read mode and address increment by ACK from master side.
If there is no ACK response, SDA output status will be released, please transmit “STOP condition”.
Read mode will be stopped by “STOP condition” transfer.
Address will be set 00h automatically after 23h. (It does not increment to 24h or 25h address)

An example of the display data read sequence is shown below.

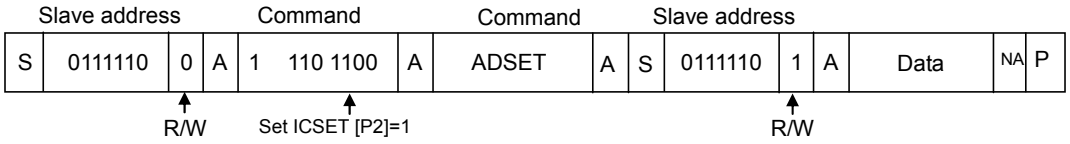


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Read command register and transfer method

Also the command registers can be read during read mode.
The sequence for the command register read is shown below and is similar to the display data read sequence.



Regarding address setting, please refer to ADSET command.
It will be able to read register values if it set address 24h or 25h.
Address does not increment automatically after register value read.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	0	0	P5	P4	P3	P2	P1	P0	24h
REG2	P7	P6	P5	P4	P3	P2	P1	P0	25h

REG1: P5 = Bias setting
P4 = Internal/External clock setting
P3 = Software Reset setting
P2 to P0 = Blink setting

REG2: P7 to P6 = Frame Frequency (FR) setting
P5 to P4 = Power Save Mode (SR) setting
P3 = Frame/Line inversion setting
P2 = Display ON/OFF setting
P1 = APON setting
P0 = APOFF setting

Address map between ADSET and ICSET is shown as follows;

Write Mode												
RAM address	ADSET				ICSET							
	D7	D6	D5	**D[4:0]**	*D7*	*D6*	*D5*	*D4*	*D3*	***D2****	*D1*	*D0*
00 0000 to 01 1111 (bin)	0	0	0	***0 0000 to 1 1111***	*1*	*1*	*1*	*0*	*1*	***0***	*0*	*0*
10 0000 to 10 0011 (bin)	0	0	0	***0 0000 to 0 0011***	*1*	*1*	*1*	*0*	*1*	***1***	*0*	*0*

Read mode												
RAM address	ADSET				ICSET							
	D7	D6	D5	**D[4:0]**	*D7*	*D6*	*D5*	*D4*	*D3*	***D2****	*D1*	*D0*
00 0000 to 01 1111 (bin)	1	0	0	***0 0000 to 1 1111***	*1*	*1*	*1*	*0*	*1*	***0***	*0*	*0*
10 0000 to 10 0101 (bin)	1	0	0	***0 0000 to 0 0101***	*1*	*1*	*1*	*0*	*1*	***1***	*0*	*0*

(Note) Please take care ICSET [P2] setting.

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OSCILLATOR

The clock signals for logic and analog circuit can be generated from internal oscillator or external clock.
If internal oscillator circuit is used, OSCIN must be connected to VSS level.
When using external clock mode, input external clock from OSCIN terminal after ICSET command setting.

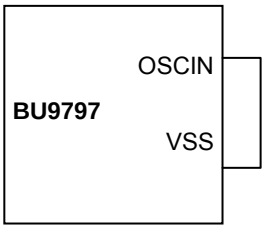


Figure 10. Internal oscillator circuit mode

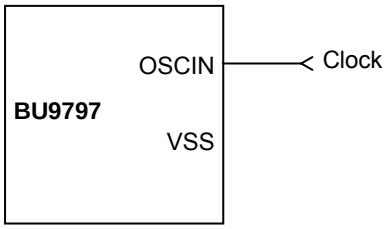


Figure 11. Ext clock input mode

LCD Driver Bias Circuit

This device generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
1/3 and 1/2Bias can set in MODESET command.
Line and frame inversion can set in DISCTL command.
Refer to the “LCD driving waveform” about each LCD driving waveform.

Blink timing generator

This device has Blink function.
This device will be Blink mode with BLKCTL command.
Blink frequency varies widely by characteristic of fCLK, when internal oscillation circuit.
About the characteristics of f_{CLK}, refer to Oscillation Characteristics.

Reset initialize condition

Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Command Description about initialize value of register.

Command / Function List

Description List of Command / Function

No.	Command	Function
1	Set IC Operation (ICSET)	Software reset, internal/external clock setting
2	Display control (DISCTL)	Frame frequency, power save mode setting
3	Address set (ADSET)	DRAM address setting (00h to 23h) Register address setting (24 to 25h)
4	Mode set (MODESET)	Display on/off,1/2bias,1/3bias
5	Blink control (BLKCTL)	Blink off/0.5s/1s/2s/3s/5s blink setting
6	All pixel control (APCTL)	All pixels on/off during DISON

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Detailed command description

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

Set IC Operation (ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2: MSB data of DDRAM address. Please refer to “ADSET” command.

Set Software Reset condition.

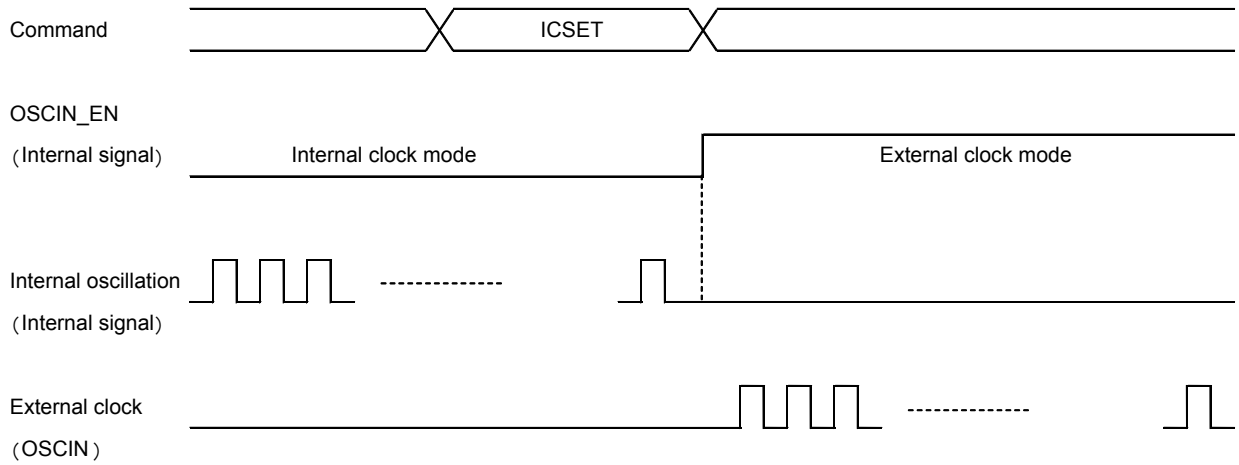
Setup	P1
No operation	0
Software reset	1

When “Software Reset” is executed, this device is reset to initial condition. (Refer to Reset initialize condition)
Don’t set Software Reset (P1) with P2, P0 at the same time.

Switch between internal clock and external clock.

Setup	P0	Initial condition
Internal clock	0	○
External clock input	1	

In Internal clock mode: OSCIN must be connect to VSS level.
In external clock input mode:: Input external clock from OSCIN terminal..



OSC MODE switch timing

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Display control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Power save mode FR.

Setup	P4	P3	Reset initialize condition
Normal mode(80Hz)	0	0	○
Power save mode1(71Hz)	0	1	
Power save mode2(64Hz)	1	0	
Power save mode3(53Hz)	1	1	

(Note) Operation current decrease in order as
Normal mode > Power save mode1 > Power save mode2 > Power save mode 3.

Set LCD drive waveform.

Setup	P2	Reset initialize condition
Line inversion mode	0	○
Frame inversion mode	1	

(Note) Operation current is Line inversion > Frame inversion
Regarding driving waveform, refer to LCD driving waveform.

Set Power save mode SR.

Setup	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

(Note1) Operation current increase in order as
Power save mode 1 < Power save mode 2 < Normal mode < High power mode.
(Note2) Please use VDD- VLCD ≥ 3.0V in High power mode condition.

(Reference current consumption data)

Setup	Current consumption
Power save mode 1	×0.5
Power save mode 2	×0.67
Normal mode	×1.0
High power mode	×1.8

(Note) Above current consumption data is reference value. Change according to panel load.

Power save mode FR / LCD drive waveform / Power save mode SR will affect display image.
Select the best setting in point of current consumption and display image view using LCD panel.

Mode	Flicker	Display grade/Contrast
Power save mode FR	○	-
LCD waveform	○	○
Power save mode SR	-	○

Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

In the write mode, the range of address can be set from 000000 to 100011(bin).
In the read mode, the range of address can be set from 000000 to 100101(bin).

(Note) Address [5:0]: MSB bit is specified in ICSET P2 and [4:0] are specified as ADSET P4 - P0.
Don't specify another address, otherwise address will be set to "000000".

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Mode Set (MODE SET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(* : Don't care)

Set display ON and OFF.

Setup	P3	Reset initialize condition
Display OFF (DISPOFF)	0	○
Display ON (DISPON)	1	

Display OFF: Despite of the contents of DDRAM, All of SEGMENT and COMMON output will stop after 1 frame period. Display OFF mode will finish in Display ON (DISPON).

Display ON: SEGMENT and COMMON output is active, start read operation to Display from DDRAM.

Set Bias level

Setup	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

Regarding driving waveform, refer to LCD driving waveform.

Blink control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	P2	P1	P0

Set Blink condition.

Setup	P2	P1	P0	Reset initialize condition
OFF	0	0	0	○
0.5Hz	0	0	1	
1Hz	0	1	0	
2Hz	0	1	1	
0.3Hz	1	0	0	
0.2Hz	1	0	1	

All pixel control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display Set ON, OFF

Setup	P1	Reset initialize condition
Normal	0	○
All pixel ON (APON)	1	

Setup	P0	Reset initialize condition
Normal	0	○
All pixel OFF (APOFF)	1	

All pixels ON : All pixels are ON regardless of DDRAM data.

All pixels OFF : All pixels are OFF regardless of DDRAM data.

(Note) All pixels ON/OFF is effective only at Display ON status. The contents of DDRAM do not change at this time.
When set P1 and P0='1', APOFF is selected. APOFF has higher priority than APON.

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LCD driving waveform

(1/3bias)

Line inversion

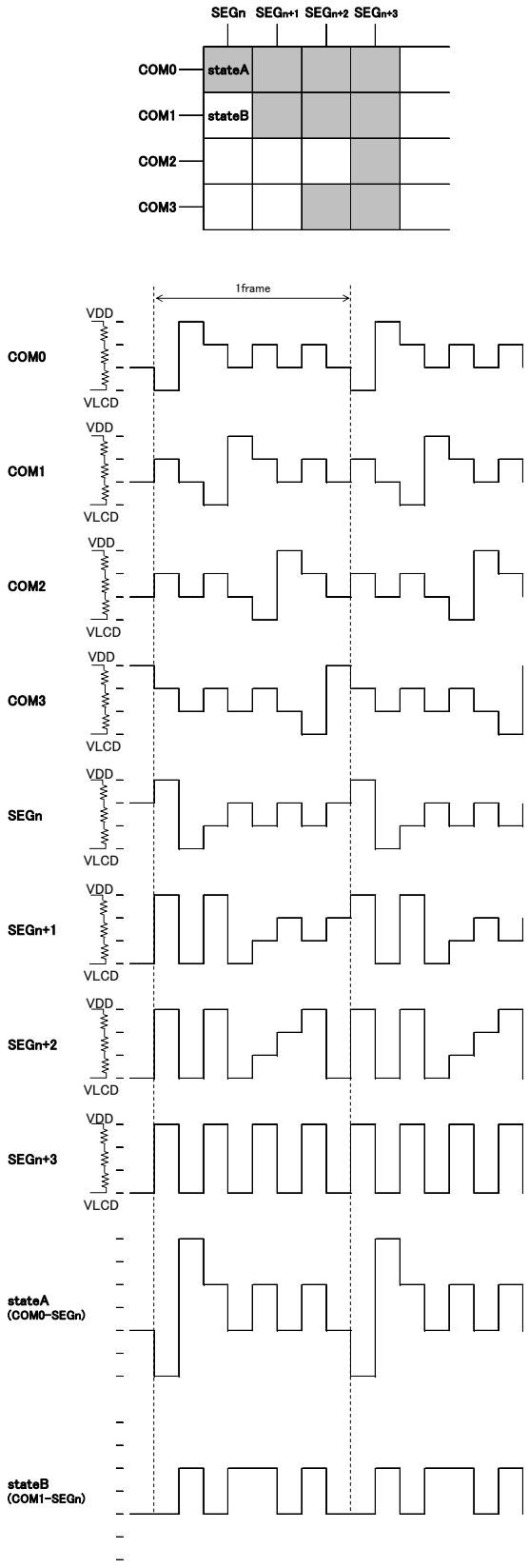


Figure 12. LCD waveform at line inversion (1/3bias)

Frame inversion

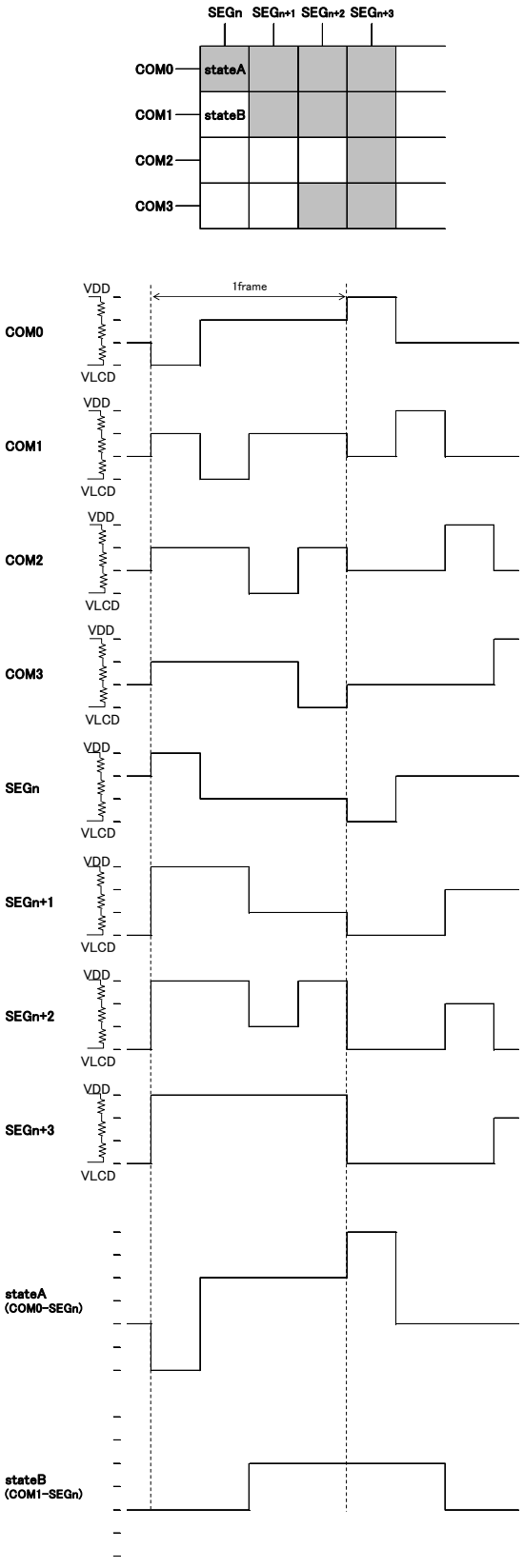


Figure 13. LCD waveform at frame inversion (1/3bias)

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(1/2bias)

Line inversion

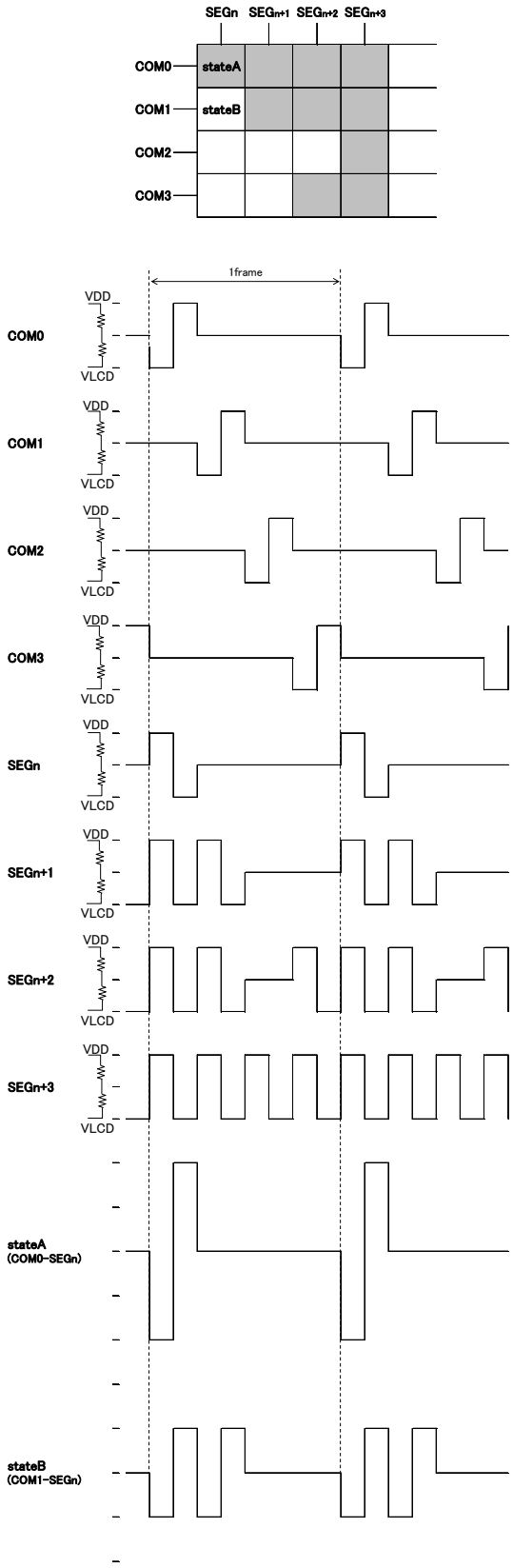


Figure 14. LCD waveform in line inversion (1/2bias)

Frame inversion

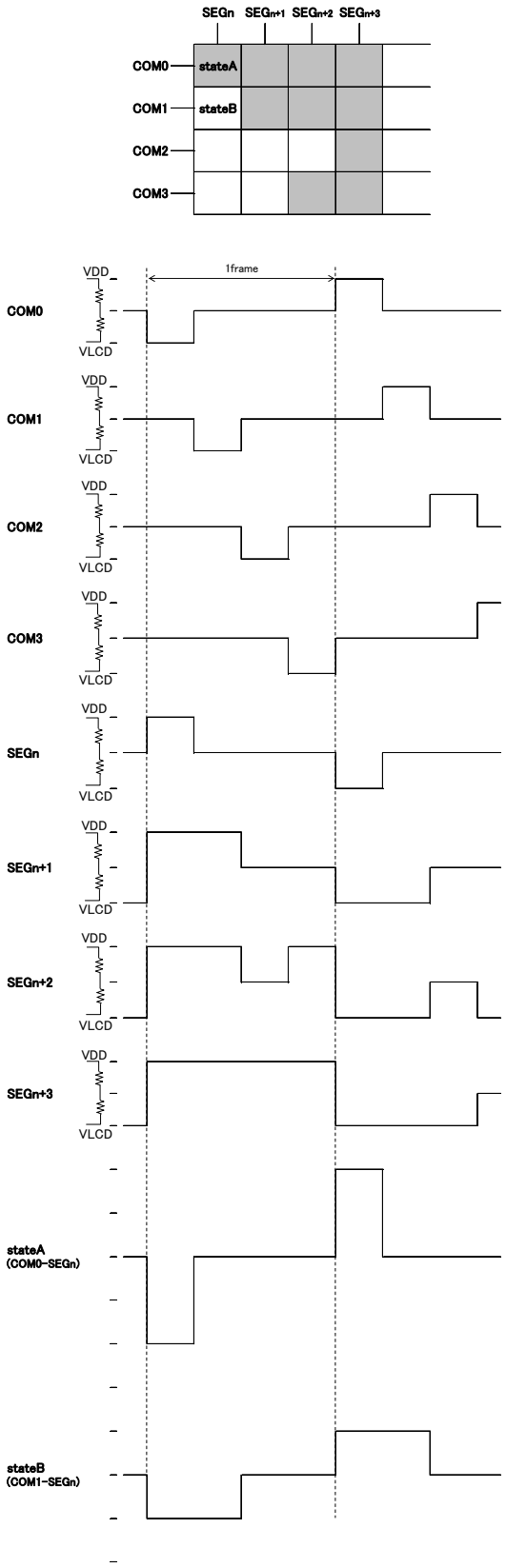


Figure 15. LCD waveform in frame inversion (1/2bias)

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Example of display data

If LCD layout pattern is like as Figure 16, Figure 17, and display pattern is like as Figure 18.
Display data will be shown as follows;

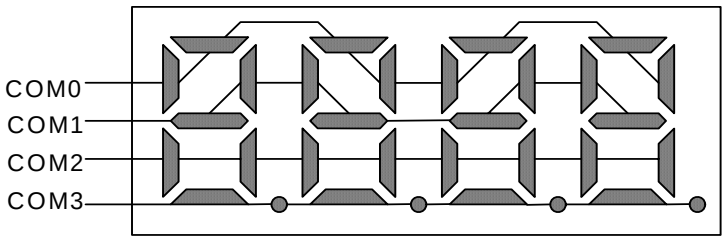


Figure 16. E.g. COM line pattern

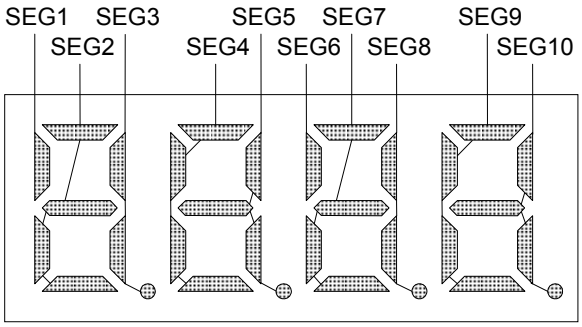


Figure 17. E.g. SEG line pattern

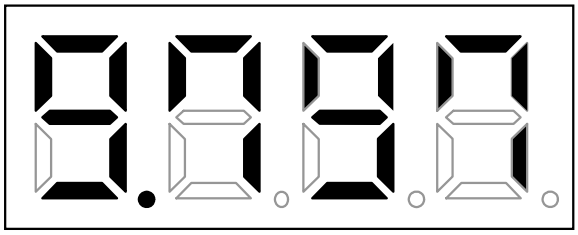


Figure 18. E.g. Display pattern

<DDRAM data mapping in Figure 18 display pattern>

		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	D0	0	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
COM2	D2	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
COM3	D3	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Address		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

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Initialize sequence

Please follow below sequence after Power-on to set this LSI to initial condition.

Power on
↓
STOP condition
↓
START condition
↓
Issue slave address
↓
Execute Software Reset by sending ICSET command.

(Note) Each register value and DDRAM address, DDRAM data are random condition after power on till initialize sequence is executed.

Start sequence

Start sequence example1

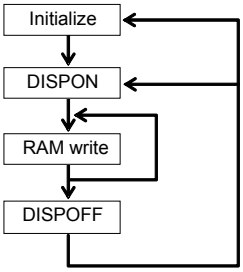
No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0→5V (Tr: max 5ms)
	↓									
2	wait 100μs									Initialize IC
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
	↓									
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	0	1	0	1	0	Software Reset
	↓									
7	BLKCTL	1	1	1	1	0	0	0	0	Blink OFF
	↓									
8	DISCTL	1	0	1	0	0	1	0	0	80Hz, Frame inv., Power save mode1
	↓									
9	ICSET	1	1	1	0	1	0	0	1	External clock input
	↓									
10	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
11	Display Data	*	*	*	*	*	*	*	*	address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	address 02h to 03h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	address 22h to 23h
	↓									
12	Stop									Stop condition
	↓									
13	Start									Start condition
	↓									
14	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
15	MODESET	1	1	0	*	1	0	*	*	Display ON, 1/3bias
	↓									
16	Stop									Stop condition

*: don't care

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Start sequence example2



Initialize Sequence

DISPON Sequence

RAM write Sequence

DISPOFF Sequence

This LSI is initialized with Initialize Sequence. And start to display with DISPON Sequence.
This LSI will update display data with RAM write Sequence. And stop the display with DISPOFF sequence.
If you want to restart to display, This LSI will restart to display with DISPON Sequence.

Initialize sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Power on									
Wait 100us									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	7C
APOFF	1	1	1	1	1	1	0	1	Set all pixel off
MODESET	1	1	0	*	0	0	*	*	Set display off
ICSET	1	1	1	0	1	0	1	0	Software reset
DISCTL	1	0	1	1	0	1	1	0	Set DISCTL setting
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display Data	*	*	*	*	*	*	*	*	
STOP									

DISPON sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	7C
DISCTL	1	0	1	1	0	1	1	0	Set DISCTL setting
BLKCTL	1	1	1	1	0	0	0	0	Set blink setting
APCTL	1	1	1	1	1	1	0	0	Close all pixel on/off function
MODESET	1	1	0	*	1	0	*	*	Set display on

STOP

RAM write sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	7C
DISCTL	1	0	1	1	0	1	1	0	Set DISCTL setting
BLKCTL	1	1	1	1	0	0	0	0	Set blink setting
APCTL	1	1	1	1	1	1	0	0	Close all pixel on/off function
MODESET	1	1	0	0	1	0	0	0	Set display on
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display Data	*	*	*	*	*	*	*	*	
STOP									

DISPOFF sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	7C
MODESET	1	1	0	0	0	0	0	0	Set display off
STOP									

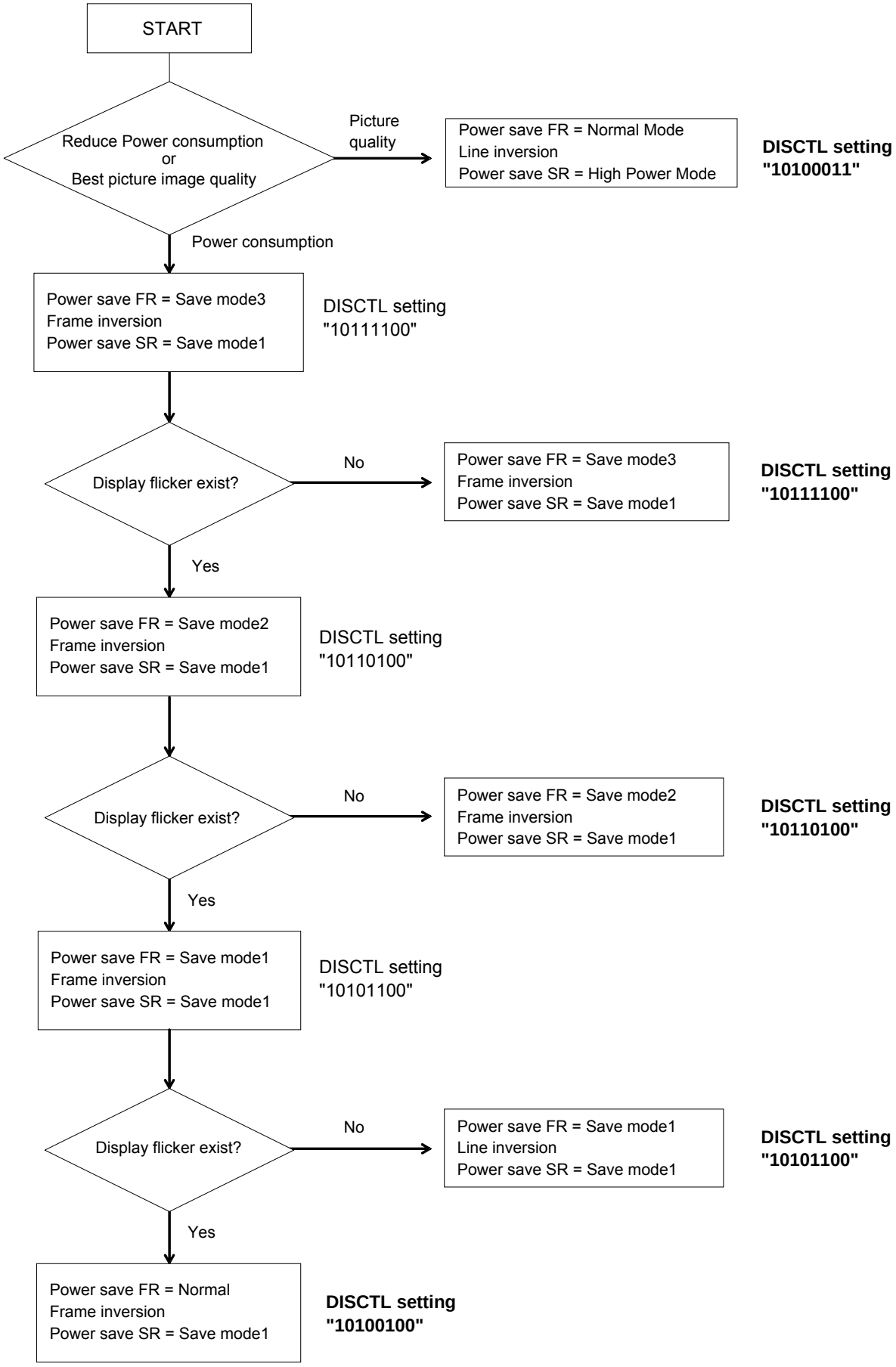
*: don't care

Abnormal operation may occur in BU9797FUV due to the effect of noise or other external factor.
To avoid this phenomenon, please input command according to sequence described above during initialization, display ON/OFF and refresh of RAM data.

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DISCTL setup flow chart



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Cautions in Power ON/OFF

This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation

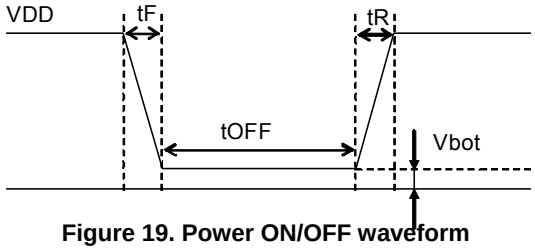


Figure 19. Power ON/OFF waveform

Recommended condition of tR, tF, tOFF, Vbot (Ta=25°C)

tR	tF	tOFF	Vbot
Max 5ms	Max 5ms	Min 20ms	Less than 0.3V

If it is difficult to meet above conditions, execute the following sequence after Power-On.

1. Generate STOP condition

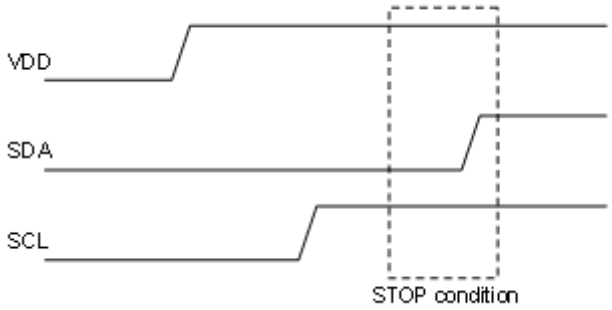


Figure 20. Stop Condition

2. Generate START condition.

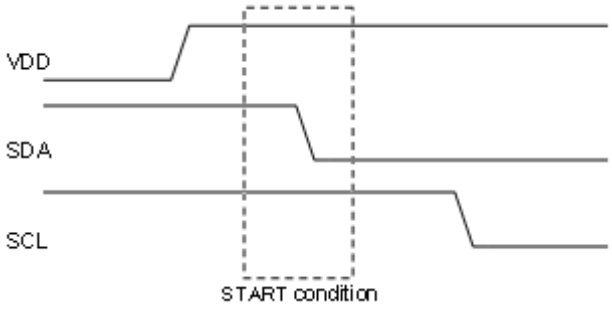


Figure 21. Start Condition

3. Issue slave address

4. Execute Software Reset (ICSET) command

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

B U 9 7 9 7 F U V - E 2

Part Number

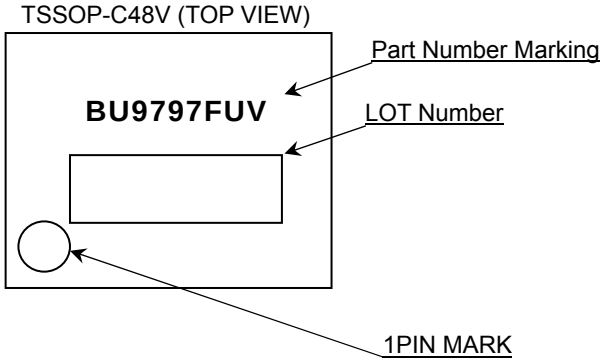
Package
FUV : TSSOP-C48V

Packaging and forming specification
E2: Embossed tape and reel
(TSSOP-C48V)

Lineup

Package		Orderable Part Number
TSSOP-C48V	Reel of 2000	BU9797FUV-E2

Marking Diagram

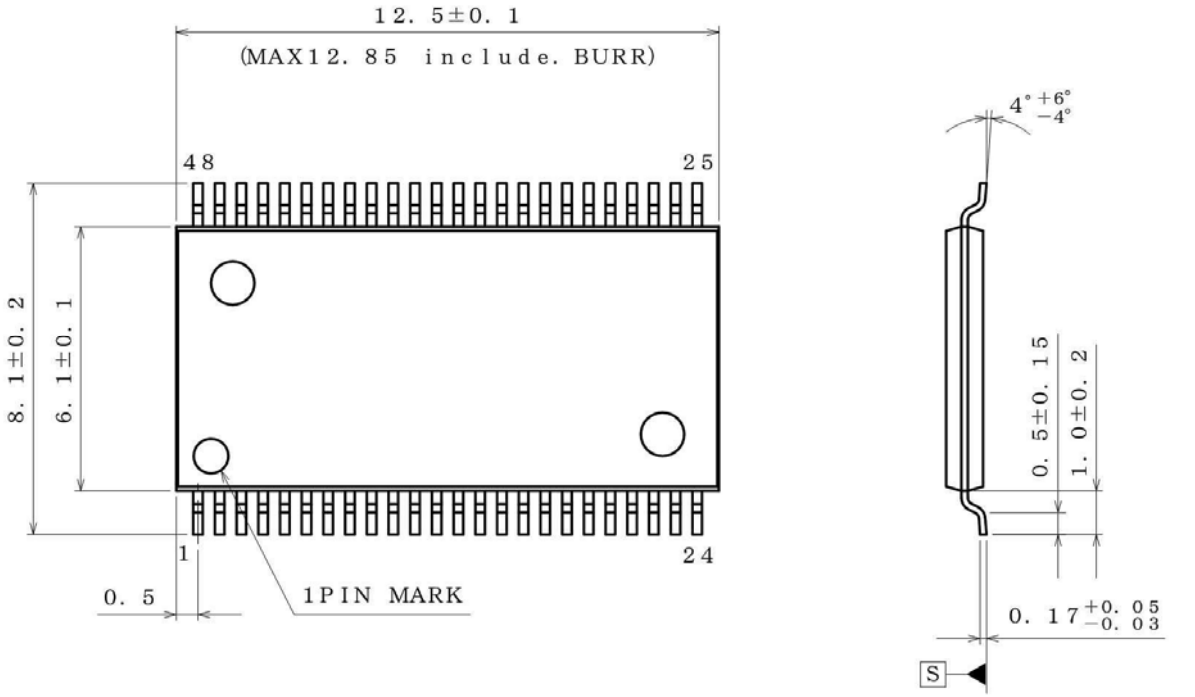


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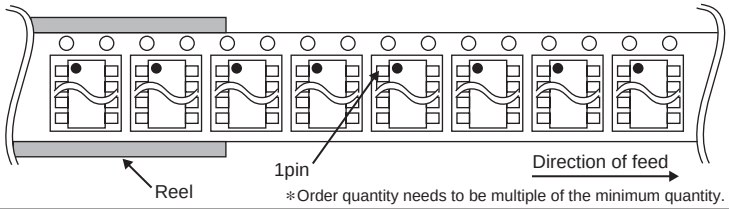
Physical Dimension Tape and Reel Information

Package Name	TSSOP-C48V



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Revision	Changes
5.Aug.2014	001	New release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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BU9797FUV - Web Page

Part Number	BU9797FUV
Package	TSSOP-C48V
Unit Quantity	2000
Minimum Package Quantity	2000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes

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