

# THC63LVD1027

## Dual Link LVDS Repeater

### General Description

The THC63LVD1027 LVDS (Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.

THC63LVD1027 receives the dual link LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.

### Features

- 30bits/pixel dual link LVDS Receiver
- 30bits/pixel dual Link LVDS Transmitter
- Operating Temperature Range : -40°C~85°C
- Wide LVDS input skew margin:  $\pm 480\text{ps}$  at 75MHz
- Accurate LVDS output timing:  $\pm 250\text{ps}$  at 75MHz
- Reduced swing LVDS output mode supported to suppress the system EMI
- Various line rate conversion modes supported
  - Dual link input / Dual link output [clkout=1x clk<sub>in</sub>]
  - Single link input / Dual link output [clkout=1/2x clk<sub>in</sub>]
  - Dual link input / Single link output [clkout=2x clk<sub>in</sub>]
- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- No external components required for PLLs
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)

### Block Diagram

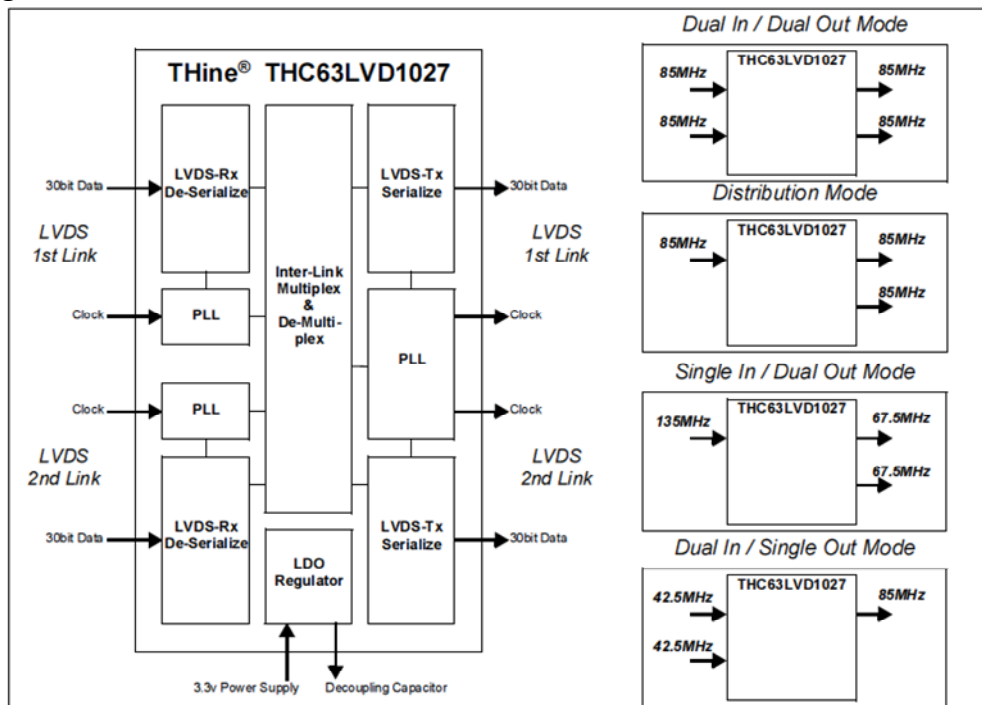


Figure 1. Block Diagram

## Pin Diagram

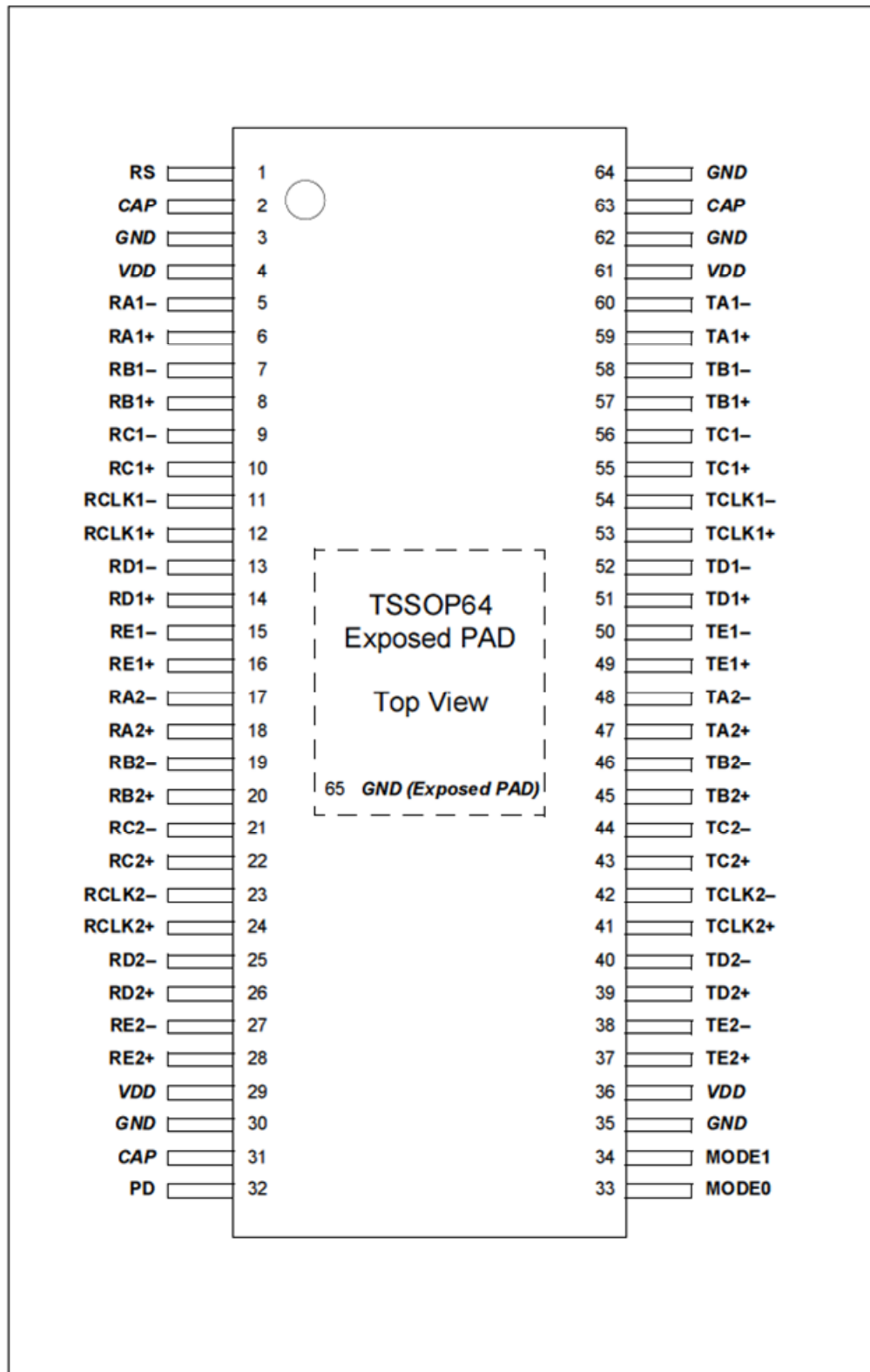


Figure 2. Pin Diagram

## Pin Description

Table 1. Pin Description

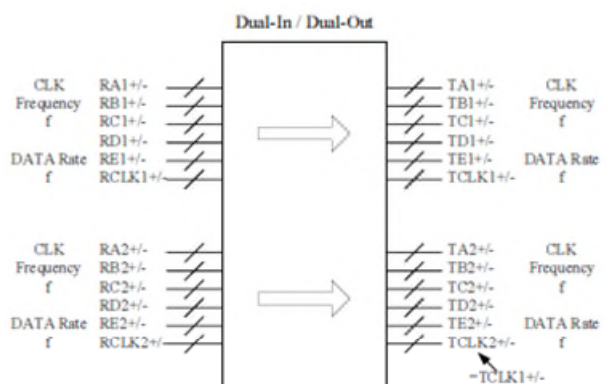
| Pin Name                                                            | Direction | Type   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
|---------------------------------------------------------------------|-----------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------|----------|-------------|---|---|-------|-----------------------|---|---|------|-------------------|---|---|------|-------------------------|---|---|-------|-------------------------|---|---|---|----------|
| RA1+/-                                                              | Input     | LVDS   | LVDS data input for channel A of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RB1+/-                                                              |           |        | LVDS data input for channel B of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RC1+/-                                                              |           |        | LVDS data input for channel C of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RD1+/-                                                              |           |        | LVDS data input for channel D of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RE1+/-                                                              |           |        | LVDS data input for channel E of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RCLK1+/-                                                            |           |        | LVDS clock input for 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                             |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RA2+/-                                                              |           |        | LVDS data input for channel A of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RB2+/-                                                              |           |        | LVDS data input for channel B of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RC2+/-                                                              |           |        | LVDS data input for channel C of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RD2+/-                                                              |           |        | LVDS data input for channel D of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RE2+/-                                                              |           |        | LVDS data input for channel E of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RCLK2+/-                                                            |           |        | LVDS clock input for 2nd Link<br>In Distribution and Single-in/Dual-out mode,RCLK2+/- must be Hi-Z.<br>(See “Mode selection” below in this page.)                                                                                                                                                                                                                                                                                                                         |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TA1+/-                                                              | Output    |        | LVDS data output for channel A of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TB1+/-                                                              |           |        | LVDS data output for channel B of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TC1+/-                                                              |           |        | LVDS data output for channel C of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TD1+/-                                                              |           |        | LVDS data output for channel D of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TE1+/-                                                              |           |        | LVDS data output for channel E of 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TCLK1+/-                                                            |           |        | LVDS clock output for 1st Link                                                                                                                                                                                                                                                                                                                                                                                                                                            |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TA2+/-                                                              |           |        | LVDS data output for channel A of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TB2+/-                                                              |           |        | LVDS data output for channel B of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TC2+/-                                                              |           |        | LVDS data output for channel C of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TD2+/-                                                              |           |        | LVDS data output for channel D of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TE2+/-                                                              |           |        | LVDS data output for channel E of 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| TCLK2+/-                                                            |           |        | LVDS clock output for 2nd Link                                                                                                                                                                                                                                                                                                                                                                                                                                            |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| PD                                                                  | Input     | LV-TTL | <b>Power Down</b><br>H: Normal operation<br>L: Power down state, all LVDS output signals turn to Hi-Z                                                                                                                                                                                                                                                                                                                                                                     |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| RS                                                                  |           |        | <b>LVDS output swing level selection</b><br>H: Normal swing<br>L: Reduced swing                                                                                                                                                                                                                                                                                                                                                                                           |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| MODE1<br>MODE0                                                      |           |        | <b>Mode selection</b> <table><tr><td>MODE1</td><td>MODE0</td><td>RCLK2+/-</td><td>Description</td></tr><tr><td>L</td><td>L</td><td>Clkin</td><td>Dual-in/Dual-out mode</td></tr><tr><td>L</td><td>L</td><td>Hi-Z</td><td>Distribution mode</td></tr><tr><td>H</td><td>L</td><td>Hi-Z</td><td>Single-in/Dual-out mode</td></tr><tr><td>L</td><td>H</td><td>Clkin</td><td>Dual-in/Single-out mode</td></tr><tr><td>H</td><td>H</td><td>-</td><td>Reserved</td></tr></table> | MODE1    | MODE0       | RCLK2+/- | Description | L | L | Clkin | Dual-in/Dual-out mode | L | L | Hi-Z | Distribution mode | H | L | Hi-Z | Single-in/Dual-out mode | L | H | Clkin | Dual-in/Single-out mode | H | H | - | Reserved |
| MODE1                                                               |           |        | MODE0                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | RCLK2+/- | Description |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| L                                                                   | L         | Clkin  | Dual-in/Dual-out mode                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| L                                                                   | L         | Hi-Z   | Distribution mode                                                                                                                                                                                                                                                                                                                                                                                                                                                         |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| H                                                                   | L         | Hi-Z   | Single-in/Dual-out mode                                                                                                                                                                                                                                                                                                                                                                                                                                                   |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| L                                                                   | H         | Clkin  | Dual-in/Single-out mode                                                                                                                                                                                                                                                                                                                                                                                                                                                   |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| H                                                                   | H         | -      | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z. |           |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| VDD                                                                 | Power     | -      | <b>3.3V power supply pins</b>                                                                                                                                                                                                                                                                                                                                                                                                                                             |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| GND                                                                 |           |        | <b>Ground pins (Exposed PAD is also Ground)</b>                                                                                                                                                                                                                                                                                                                                                                                                                           |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |
| CAP                                                                 |           |        | <b>Decoupling capacitor pins</b><br>These pins should be connected to external decoupling capacitors(Ccap).<br>Recommended Ccap is 0.1μF.                                                                                                                                                                                                                                                                                                                                 |          |             |          |             |   |   |       |                       |   |   |      |                   |   |   |      |                         |   |   |       |                         |   |   |   |          |

## Mode Setting

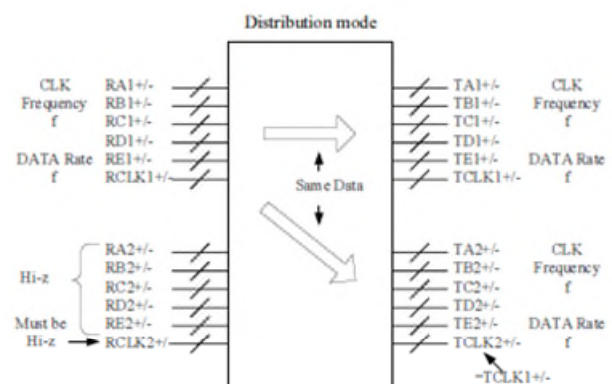
**Table 2. Mode Setting**

| Input/Output                         | RCLK2+/- | MODE1<br>(Input mode) | MODE0<br>(Output mode) |
|--------------------------------------|----------|-----------------------|------------------------|
|                                      |          | H: Single<br>L: Dual  | H: Single<br>L: Dual   |
| Dual-In/Dual-Out<br>(Fig.3-1,14-1)   | CLK in   | L                     | L                      |
| Distribution<br>(Fig.3-2,14-2)       | Hi-Z     | L                     | L                      |
| Single-In/Dual-Out<br>(Fig.3-3,14-3) | Hi-Z     | H                     | L                      |
| Dual-In/Single-Out<br>(Fig.3-4,14-4) | CLK in   | L                     | H                      |
| Reserved                             | -        | H                     | H                      |

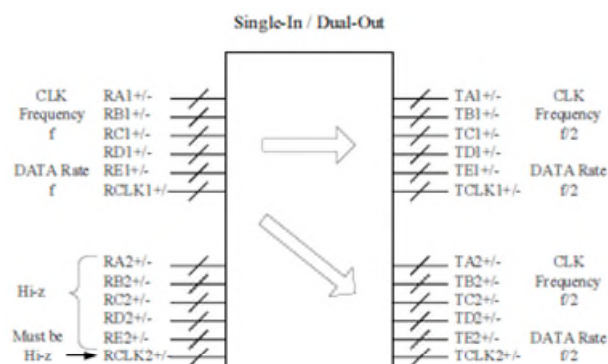
## Signal Flow for Each Setting



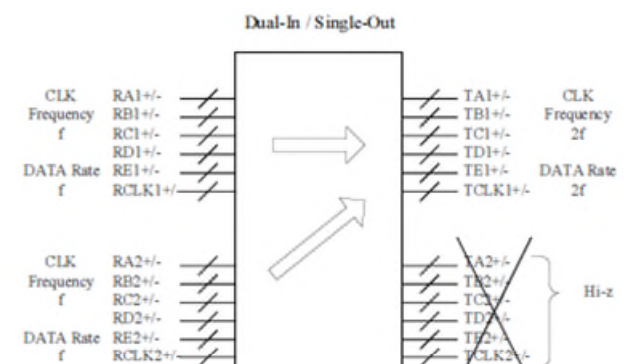
**Figure 3-1**



**Figure 3-2**



**Figure 3-3**



**Figure 3-4**

## Output Control / Fail Safe

THC63LVD1027 has a function to control output depending on LVDS input condition.

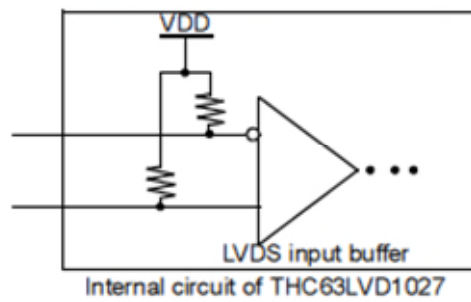
**Table 3. Output Control**

| PD | RCLK1+/- | RCLK2+/- | Output                      |
|----|----------|----------|-----------------------------|
| L  | *        | *        | All Hi-Z                    |
| H  | Hi-Z     | *        | All Hi-Z                    |
| H  | CLK in   | CLK in   | Refer to p.4 Mode Setting # |
| H  | CLK in   | Hi-Z     | Refer to p.4 Mode Setting # |

\*: Don't care

#: If a particular input data pair is Hi-Z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting Hi-Z state.



**Figure 4. Fail Safe Circuit**

## Absolute Maximum Ratings

**Table 4. Absolute Maximum Rating**

| Parameter                        | Min  | Max          | Unit |
|----------------------------------|------|--------------|------|
| Power Supply Voltage             | -0.3 | +4.0         | V    |
| LVC MOS Input Voltage            | -0.3 | $V_{DD}+0.3$ | V    |
| LVDS Input Voltage               | -0.3 | $V_{DD}+0.3$ | V    |
| Junction Temperature             | -    | 125          | °C   |
| Storage Temperature              | -55  | 125          | °C   |
| Reflow Peak Temperature / Time   | -    | 260 / 10sec  | °C   |
| Maximum Power Dissipation @+25°C | -    | 2.5          | W    |

## Operating Conditions

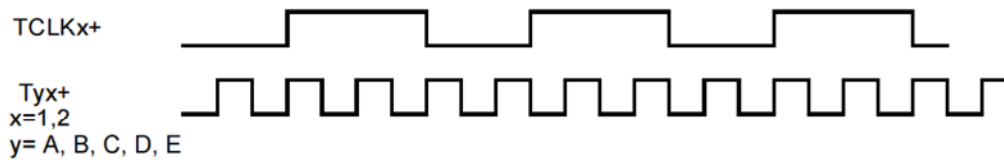
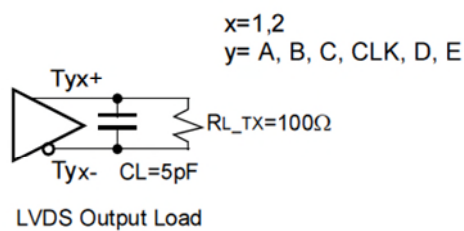
**Table 5. Operating Condition**

| Symbol                 | Parameter                     |        | Min | Typ | Max  | Unit |
|------------------------|-------------------------------|--------|-----|-----|------|------|
| <b>T<sub>a</sub></b>   | Operating Ambient Temperature |        | -40 | 25  | +85  | °C   |
| <b>V<sub>DD</sub></b>  | Power Supply Voltage          |        | 3.0 | 3.3 | 3.6  | V    |
| <b>F<sub>clk</sub></b> | Dual-In/Dual-Out              | Input  | 20  | -   | 85   | MHz  |
|                        |                               | Output | 20  | -   | 85   |      |
|                        | Distribution                  | Input  | 20  | -   | 85   | MHz  |
|                        |                               | Output | 20  | -   | 85   |      |
|                        | Single-In/Dual-Out            | Input  | 40  | -   | 135  | MHz  |
|                        |                               | Output | 20  | -   | 67.5 |      |
|                        | Dual-In/Single-Out            | Input  | 20  | -   | 42.5 | MHz  |
|                        |                               | Output | 40  | -   | 85   |      |

## Power Consumption

**Table 6. Power Consumption**

| Symbol                 | Parameter                                               | Conditions         |               |                                                             | Min | Typ. | Max | Unit |
|------------------------|---------------------------------------------------------|--------------------|---------------|-------------------------------------------------------------|-----|------|-----|------|
| <b>I<sub>CCW</sub></b> | Operating Current<br>(Worst Case Pattern)<br><br>Fig 5. | Dual-In/Dual-Out   | CLKIN=40MHz   | $R_{L\_Tx}=100\Omega$<br><br>CL=5pF<br>RS=VDD<br><br>Fig 6. | -   | -    | 265 | mA   |
|                        |                                                         |                    | CLKIN=65MHz   |                                                             | -   | -    | 305 |      |
|                        |                                                         |                    | CLKIN=75MHz   |                                                             | -   | -    | 325 |      |
|                        |                                                         |                    | CLKIN=85MHz   |                                                             | -   | -    | 340 |      |
|                        |                                                         | Distribution       | CLKIN=40MHz   |                                                             | -   | -    | 215 | mA   |
|                        |                                                         |                    | CLKIN=65MHz   |                                                             | -   | -    | 235 |      |
|                        |                                                         |                    | CLKIN=75MHz   |                                                             | -   | -    | 245 |      |
|                        |                                                         |                    | CLKIN=85MHz   |                                                             | -   | -    | 260 |      |
|                        |                                                         | Single-In/Dual-Out | CLKIN=40MHz   |                                                             | -   | -    | 175 | mA   |
|                        |                                                         |                    | CLKIN=65MHz   |                                                             | -   | -    | 190 |      |
|                        |                                                         |                    | CLKIN=75MHz   |                                                             | -   | -    | 200 |      |
|                        |                                                         |                    | CLKIN=85MHz   |                                                             | -   | -    | 210 |      |
|                        |                                                         |                    | CLKIN=112MHz  |                                                             | -   | -    | 230 |      |
|                        |                                                         |                    | CLKIN=135MHz  |                                                             | -   | -    | 250 |      |
|                        |                                                         | Dual-In/Single-Out | CLKIN=20MHz   |                                                             | -   | -    | 215 | mA   |
|                        |                                                         |                    | CLKIN=32.5MHz |                                                             | -   | -    | 235 |      |
|                        |                                                         |                    | CLKIN=37.5MHz |                                                             | -   | -    | 245 |      |
|                        |                                                         |                    | CLKIN=42.5MHz |                                                             | -   | -    | 260 |      |
| <b>I<sub>CCS</sub></b> | Power Down Current                                      | -                  | -             | -                                                           | -   | -    | 8   | mA   |


**Figure 5. Test Pattern (LVDS Output Full Toggle Pattern)**

**Figure 6. LVDS Output Load**

## Electrical Characteristics

### DC Specifications

Table 7. DC Specifications

| Symbol              | Parameter                        | Conditions              | Min | Typ | Max | Unit |
|---------------------|----------------------------------|-------------------------|-----|-----|-----|------|
| V <sub>CAP</sub>    | Capacitor pin appearance voltage | C <sub>CAP</sub> =0.1μF | -   | 1.8 | -   | V    |
| V <sub>IL</sub>     | LV-TTL Input Low Voltage         | -                       | GND | -   | 0.8 | V    |
| V <sub>IH</sub>     | LV-TTL Input High Voltage        | -                       | 2.0 | -   | VDD | V    |
| I <sub>IN_TTL</sub> | LV-TTL Input Leakage Current     | -                       | -4  | -   | +4  | μA   |

### LVDS Receiver DC Specifications

Table 8. LVDS Receiver DC Specifications

| Symbol             | Parameter                           | Conditions                            | Min  | Typ | Max  | Unit |
|--------------------|-------------------------------------|---------------------------------------|------|-----|------|------|
| V <sub>IN_RX</sub> | LVDS-Rx Input Voltage Range         | -                                     | 0.3  | -   | 2.1  | V    |
| V <sub>IC_RX</sub> | LVDS-Rx Common Voltage              | -                                     | 0.6  | 1.2 | 1.8  |      |
| V <sub>TH_RX</sub> | LVDS-Rx Differential High Threshold | V <sub>IC_RX</sub> = 1.2V             | -    | -   | +100 | mV   |
| V <sub>TL_RX</sub> | LVDS-Rx Differential Low Threshold  |                                       | -100 | -   | -    |      |
| V <sub>ID_RX</sub> | LVDS-Rx Differential Input Voltage  | -                                     | 100  | -   | 600  |      |
| I <sub>IN_RX</sub> | LVDS-Rx Input Leakage Current       | PD=VDD                                | -0.3 | -   | +0.3 | mA   |
|                    |                                     | PD=GND<br>V <sub>in</sub> =GND or VDD | -10  | -   | +10  | μA   |

### LVDS Transmitter DC Specifications

Table 9. LVDS Transmitter DC Specifications

| Symbol              | Parameter                                         | Conditions                  |                              | Min   | Typ  | Max   | Unit |
|---------------------|---------------------------------------------------|-----------------------------|------------------------------|-------|------|-------|------|
| V <sub>OC_TX</sub>  | LVDS-Tx Common Voltage                            | R <sub>L_TX</sub> =<br>100Ω | -                            | 1.125 | 1.25 | 1.375 | V    |
| ΔV <sub>OC_TX</sub> | Change in VOC between complementary output states |                             | -                            | -     | -    | 35    | mV   |
| V <sub>OD_TX</sub>  | LVDS-Tx Differential Output Threshold             |                             | Normal Swing                 | 250   | 350  | 450   | mV   |
|                     |                                                   |                             | Reduced Swing                | 100   | 200  | 300   |      |
| ΔV <sub>OD_TX</sub> | Change in VOD between complementary output states |                             | -                            | -     | -    | 35    | mV   |
| I <sub>OS_TX</sub>  | LVDS-Tx Output Short Current                      | V <sub>DD</sub> =3.3V       | V <sub>out</sub> =GND        | -24   | -    | -     | mA   |
| I <sub>OZ_TX</sub>  | LVDS-Tx Output Tri-state Current                  | PD=GND                      | V <sub>out</sub> =GND to VDD | -10   | -    | +10   | μA   |

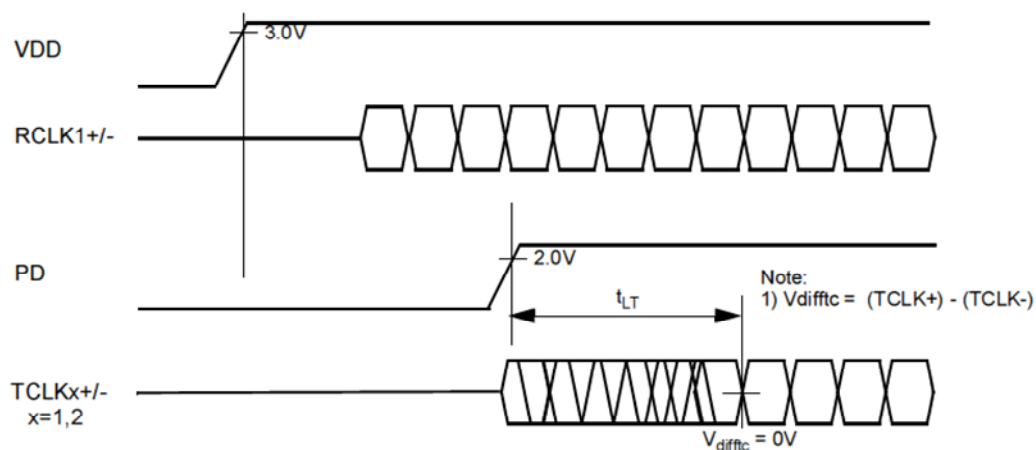


## AC Specifications

**Table 10. AC Specifications**

| Symbol      | Parameter                         | Conditions         |               | Min                 | Typ                                 | Max                 | Unit |
|-------------|-----------------------------------|--------------------|---------------|---------------------|-------------------------------------|---------------------|------|
| $t_{LT}$    | Phase Lock Loop Set Time (Fig 7.) | -                  | -             | -                   | -                                   | 10                  | ms   |
| $t_{DL}$    | Data Latency (Fig 8.)             | Dual-In/Dual-Out   | CLKIN=75MHz   | $9t_{RCP}+3$        | $9t_{RCP}+5$                        | $9t_{RCP}+7$        | ns   |
|             |                                   | Distribution       | CLKIN=75MHz   | $9t_{RCP}+3$        | $9t_{RCP}+5$                        | $9t_{RCP}+7$        |      |
|             |                                   | Single-In/Dual-Out | CLKIN=75MHz   | $(11+2/7)t_{RCP}+3$ | $(11+2/7)t_{RCP}+5$                 | $(11+2/7)t_{RCP}+7$ |      |
|             |                                   | Dual-In/Single-Out | CLKIN=37.5MHz | $(8+5/14)t_{RCP}+3$ | $(8+5/14)t_{RCP}+5$                 | $(8+5/14)t_{RCP}+7$ |      |
| $t_{DEH}$   | DE Input High Time (Fig 9.)       | Single-In/Dual-Out | -             | $2t_{RCP}$          | -                                   | -                   | ns   |
| $t_{DEL}$   | DE Input Low Time (Fig 9.)        |                    | -             | $2t_{RCP}$          | -                                   | -                   |      |
| $t_{DEINT}$ | DE Input Period (Fig 9.)          |                    | -             | $4t_{RCP}$          | Must be $2n t_{RCP}$<br>(n=integer) | -                   |      |

## AC Timing Diagrams



**Figure 7. Phase Lock Loop Set Time**

## AC Timing Diagrams (Continued)

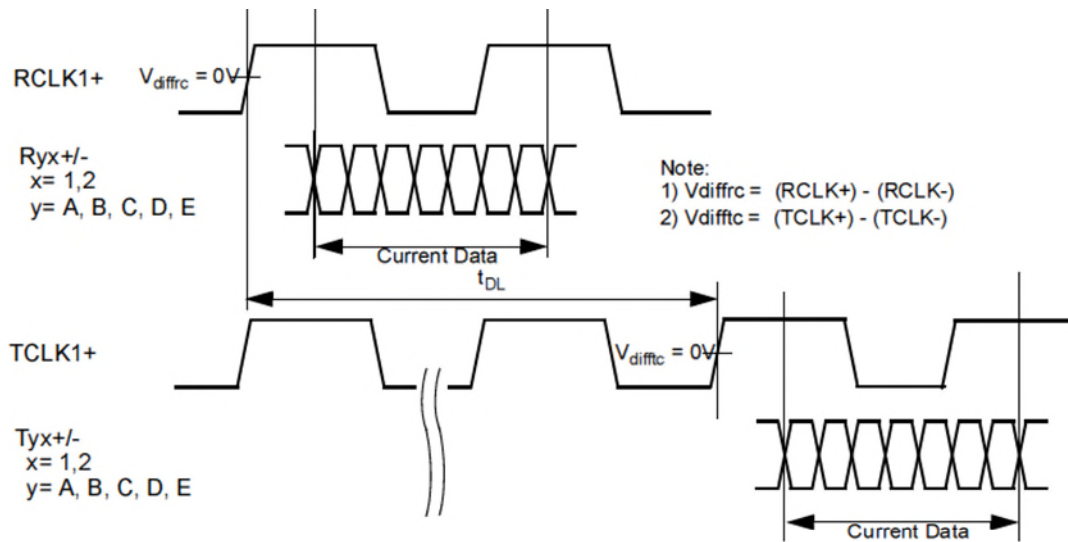


Figure 8. DATA Latency

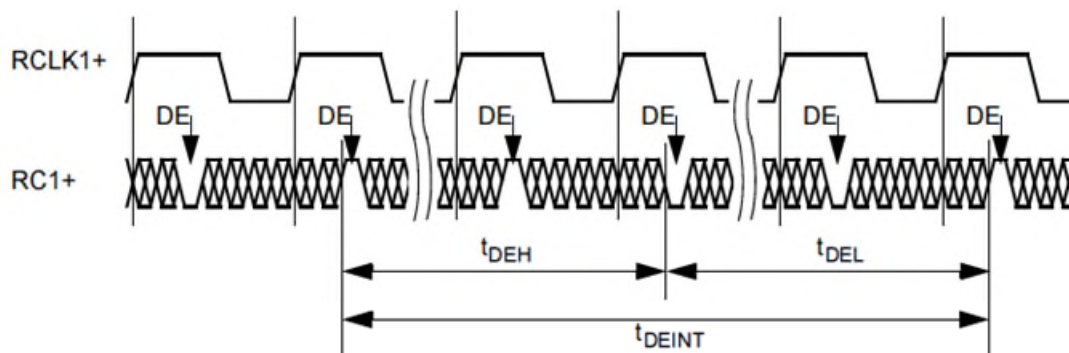


Figure 9. Single Link Input / Dual Link Output Mode RC1(DE) Input Timing

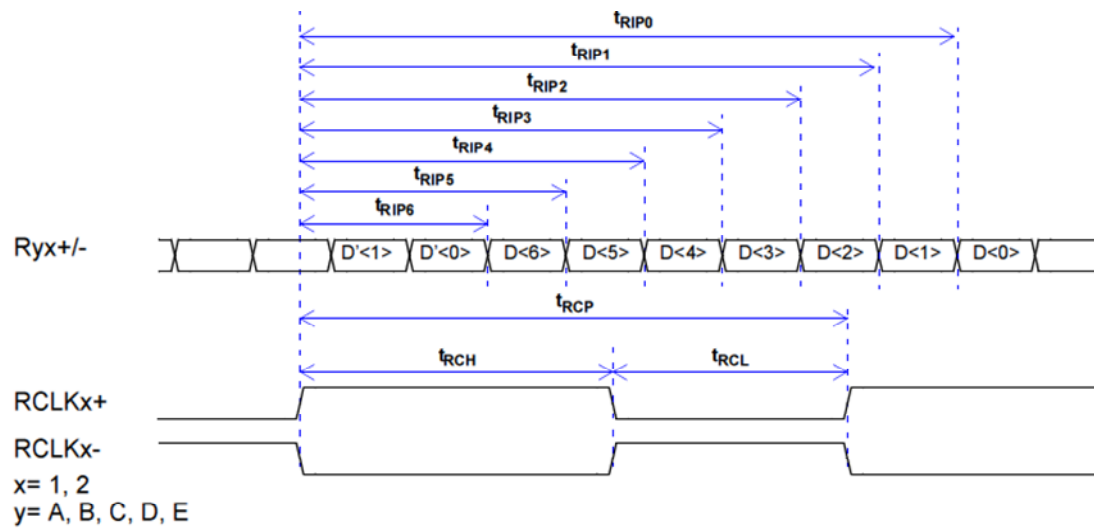
## LVDS Receiver AC Specifications

**Table 11. LVDS Receiver AC Specifications**

| Symbol     | Parameter                         | Conditions                  | Min                      | Typ           | Max                      | Unit |
|------------|-----------------------------------|-----------------------------|--------------------------|---------------|--------------------------|------|
| $t_{RCP}$  | LVDS Clock Period                 | -                           | 7.4                      | -             | 50                       | ns   |
| $t_{RCH}$  | LVDS Clock High Duration          | -                           | $2/7 t_{RCP}$            | $4/7 t_{RCP}$ | $5/7 t_{RCP}$            |      |
| $t_{RCL}$  | LVDS Clock Low Duration           | -                           | $2/7 t_{RCP}$            | $3/7 t_{RCP}$ | $5/7 t_{RCP}$            |      |
| $t_{RSUP}$ | LVDS Data Input Setup Margin      | CLKIN=75MHz <sup>(1)</sup>  | 480                      | -             | -                        | ps   |
|            |                                   | CLKIN=112MHz <sup>(1)</sup> | 250                      | -             | -                        |      |
|            |                                   | CLKIN=135MHz <sup>(1)</sup> | 220                      | -             | -                        |      |
| $t_{RHLD}$ | LVDS Data Input Hold Margin       | CLKIN=75MHz <sup>(1)</sup>  | 480                      | -             | -                        | ps   |
|            |                                   | CLKIN=112MHz <sup>(1)</sup> | 250                      | -             | -                        |      |
|            |                                   | CLKIN=135MHz <sup>(1)</sup> | 220                      | -             | -                        |      |
| $t_{RIP6}$ | LVDS Data Input Position 6        | -                           | $2/7 t_{RCP} - t_{RHLD}$ | $2/7 t_{RCP}$ | $2/7 t_{RCP} + t_{RSUP}$ | ps   |
| $t_{RIP5}$ | LVDS Data Input Position 5        | -                           | $3/7 t_{RCP} - t_{RHLD}$ | $3/7 t_{RCP}$ | $3/7 t_{RCP} + t_{RSUP}$ |      |
| $t_{RIP4}$ | LVDS Data Input Position 4        | -                           | $4/7 t_{RCP} - t_{RHLD}$ | $4/7 t_{RCP}$ | $4/7 t_{RCP} + t_{RSUP}$ |      |
| $t_{RIP3}$ | LVDS Data Input Position 3        | -                           | $5/7 t_{RCP} - t_{RHLD}$ | $5/7 t_{RCP}$ | $5/7 t_{RCP} + t_{RSUP}$ |      |
| $t_{RIP2}$ | LVDS Data Input Position 2        | -                           | $6/7 t_{RCP} - t_{RHLD}$ | $6/7 t_{RCP}$ | $6/7 t_{RCP} + t_{RSUP}$ |      |
| $t_{RIP1}$ | LVDS Data Input Position 1        | -                           | $7/7 t_{RCP} - t_{RHLD}$ | $7/7 t_{RCP}$ | $7/7 t_{RCP} + t_{RSUP}$ |      |
| $t_{RIP0}$ | LVDS Data Input Position 0        | -                           | $8/7 t_{RCP} - t_{RHLD}$ | $8/7 t_{RCP}$ | $8/7 t_{RCP} + t_{RSUP}$ |      |
| $t_{CK12}$ | Skew Time Between RCLK1 and RCLK2 | -                           | $-0.3 t_{RCP}$           | -             | $+0.3 t_{RCP}$           | ps   |

(1)  $V_{IC\_RX}=1.2V$ ,  $t_{RCH}=4/7 t_{RCP}$

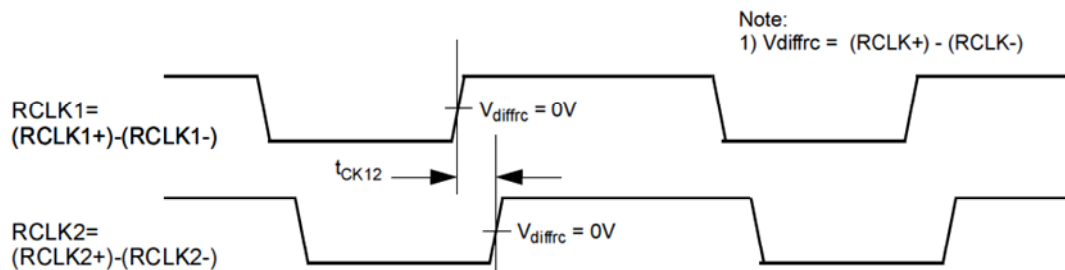
## LVDS Receiver Input Timing



$R_{y1+/-}$  skew margin is the one between  $RCLK1+/-$  and  $R_{y1+/-}$ .

$R_{y2+/-}$  skew margin is the one between  $RCLK2+/-$  and  $R_{y2+/-}$ .

**Figure 10. LVDS Receiver Timing**



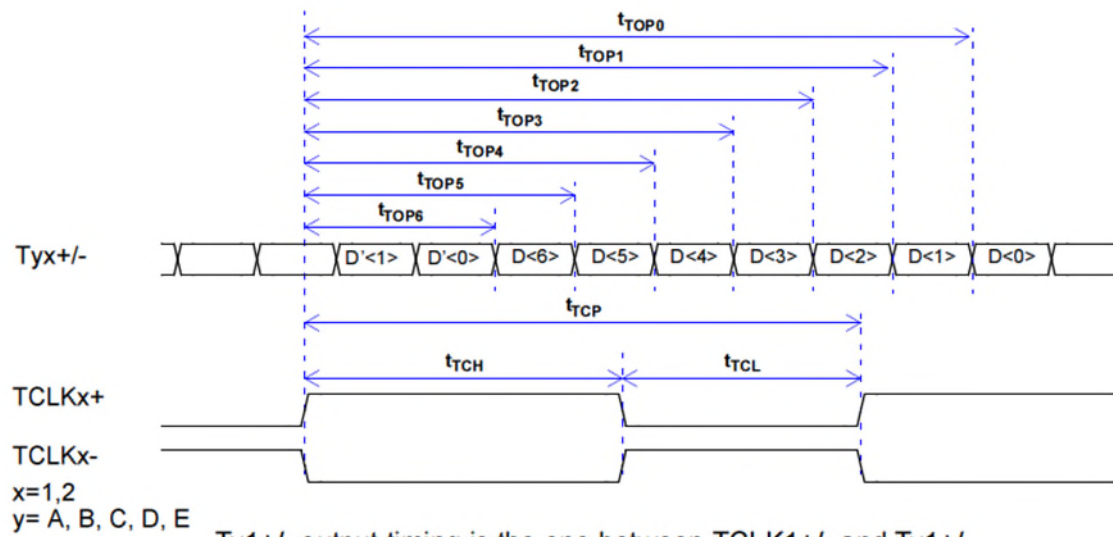
**Figure 11. Skew time between RCLK1 and RCLK2**

## LVDS Transmitter AC Specifications

**Table 12. LVDS Transmitter AC Specifications**

| Symbol     | Parameter                      | Conditions   | Min                   | Typ          | Max                   | Unit |
|------------|--------------------------------|--------------|-----------------------|--------------|-----------------------|------|
| $t_{TCP}$  | LVDS Clock Period              | -            | 11.76                 | -            | 50                    | ns   |
| $t_{TCH}$  | LVDS Clock High Duration       | -            | -                     | $4/7t_{TCP}$ | -                     |      |
| $t_{TCL}$  | LVDS Clock Low Duration        | -            | -                     | $3/7t_{TCP}$ | -                     |      |
| $t_{TSUP}$ | LVDS Data Output Setup         | CLKOUT=75MHz | -                     | -            | 250                   | ps   |
| $t_{THLD}$ | LVDS Data Output Hold          | CLKOUT=75MHz | -                     | -            | 250                   | ps   |
| $t_{TOP6}$ | LVDS Data Output Position 6    | -            | $2/7t_{TCP}-t_{THLD}$ | $2/7t_{TCP}$ | $2/7t_{TCP}+t_{TSUP}$ | ps   |
| $t_{TOP5}$ | LVDS Data Output Position 5    | -            | $3/7t_{TCP}-t_{THLD}$ | $3/7t_{TCP}$ | $3/7t_{TCP}+t_{TSUP}$ |      |
| $t_{TOP4}$ | LVDS Data Output Position 4    | -            | $4/7t_{TCP}-t_{THLD}$ | $4/7t_{TCP}$ | $4/7t_{TCP}+t_{TSUP}$ |      |
| $t_{TOP3}$ | LVDS Data Output Position 3    | -            | $5/7t_{TCP}-t_{THLD}$ | $5/7t_{TCP}$ | $5/7t_{TCP}+t_{TSUP}$ |      |
| $t_{TOP2}$ | LVDS Data Output Position 2    | -            | $6/7t_{TCP}-t_{THLD}$ | $6/7t_{TCP}$ | $6/7t_{TCP}+t_{TSUP}$ |      |
| $t_{TOP1}$ | LVDS Data Output Position 1    | -            | $7/7t_{TCP}-t_{THLD}$ | $7/7t_{TCP}$ | $7/7t_{TCP}+t_{TSUP}$ |      |
| $t_{TOP0}$ | LVDS Data Output Position 0    | -            | $8/7t_{TCP}-t_{THLD}$ | $8/7t_{TCP}$ | $8/7t_{TCP}+t_{TSUP}$ |      |
| $t_{LVT}$  | LVDS Transition Time (Fig 13.) | Fig.6        | -                     | 0.6          | 1.5                   | ns   |

## LVDS Transmitter Output Diagram



$Ty_{1+/-}$  output timing is the one between  $TCLK_{1+/-}$  and  $Ty_{1+/-}$ .

$Ty_{2+/-}$  output timing is the one between  $TCLK_{2+/-}$  and  $Ty_{2+/-}$ .

Figure 12. LVDS Transmitter Timing

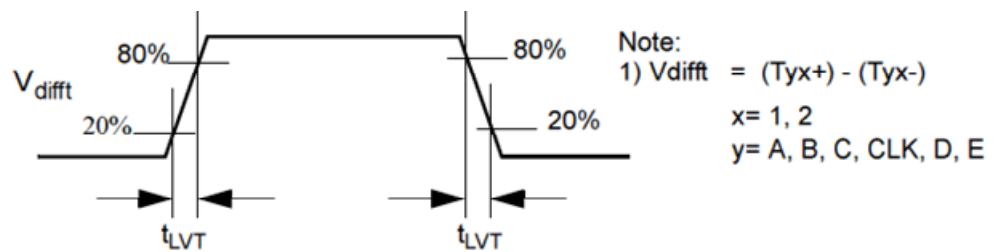


Figure 13. LVDS Transition Timing



## LVDS Data Mapping

### Dual-In / Dual-Out

#### LVDS-Rx Input Mapping



#### LVDS-Tx Output Mapping



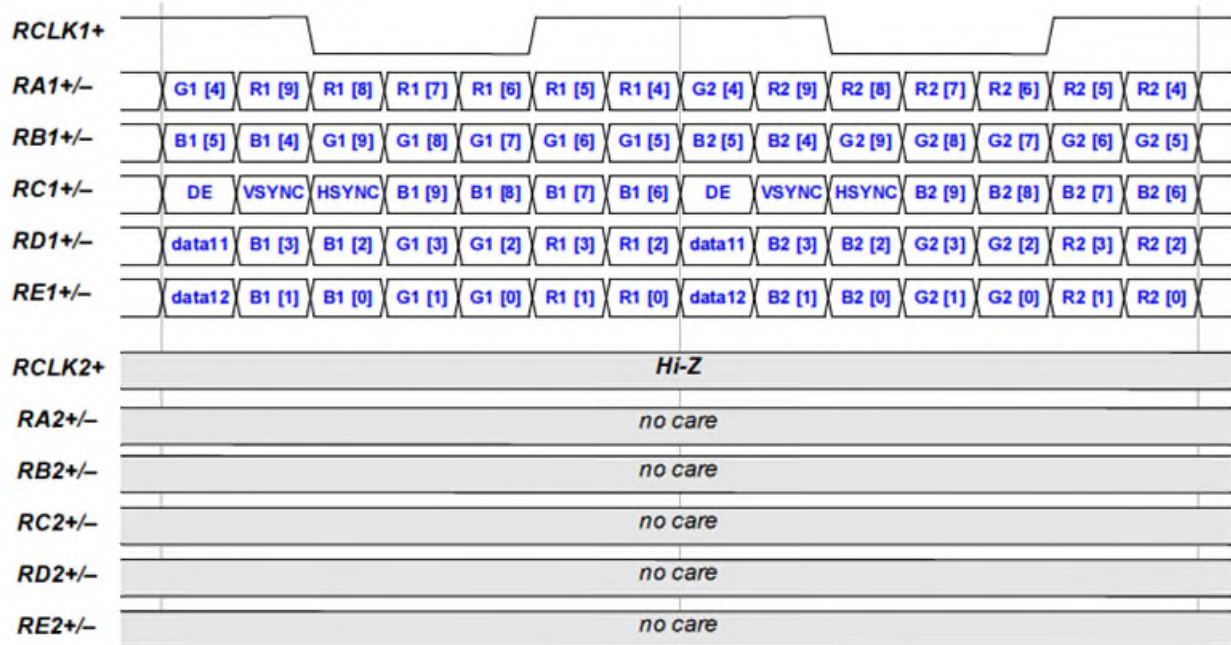
Data bits "data11, data12, data21, data22" are available for additional data transmission.

Figure 14-1. Data Mapping for Dual-In/Dual-Out

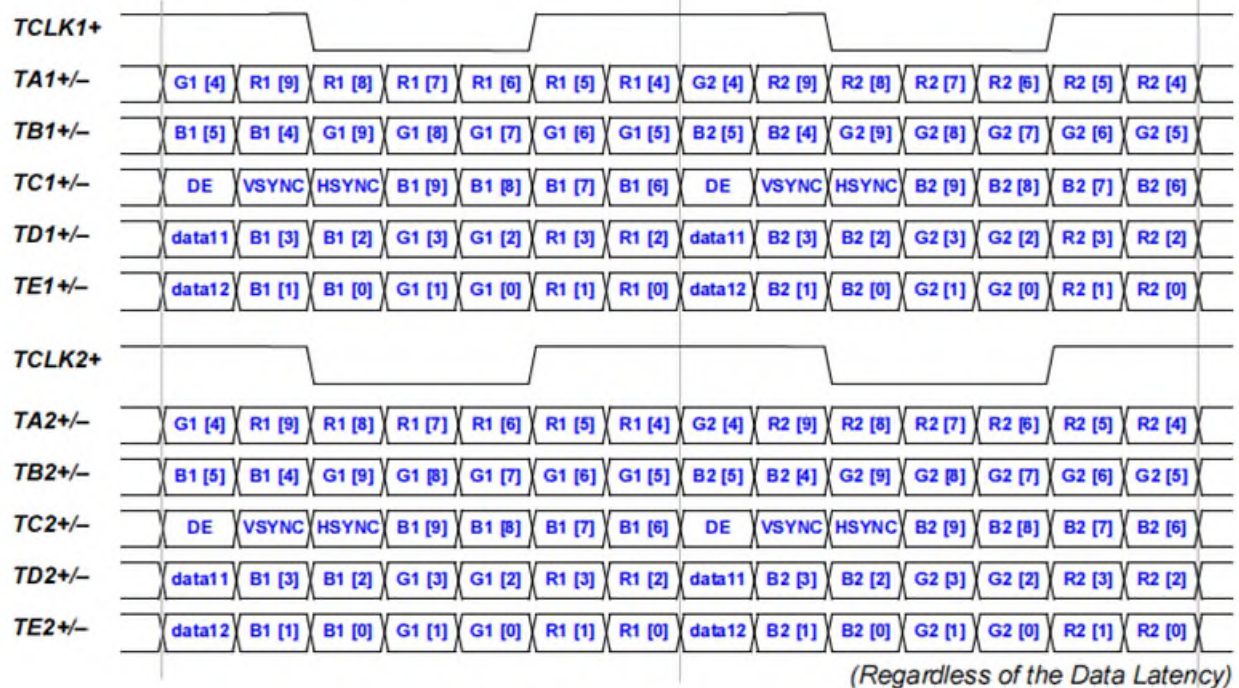
## Distribution Mode

In Distribution mode, RCLK2+/- must be Hi-Z.

### LVDS-Rx Input Mapping



### LVDS-Tx Output Mapping



Data bits "data11, data12" are available for additional data transmission.

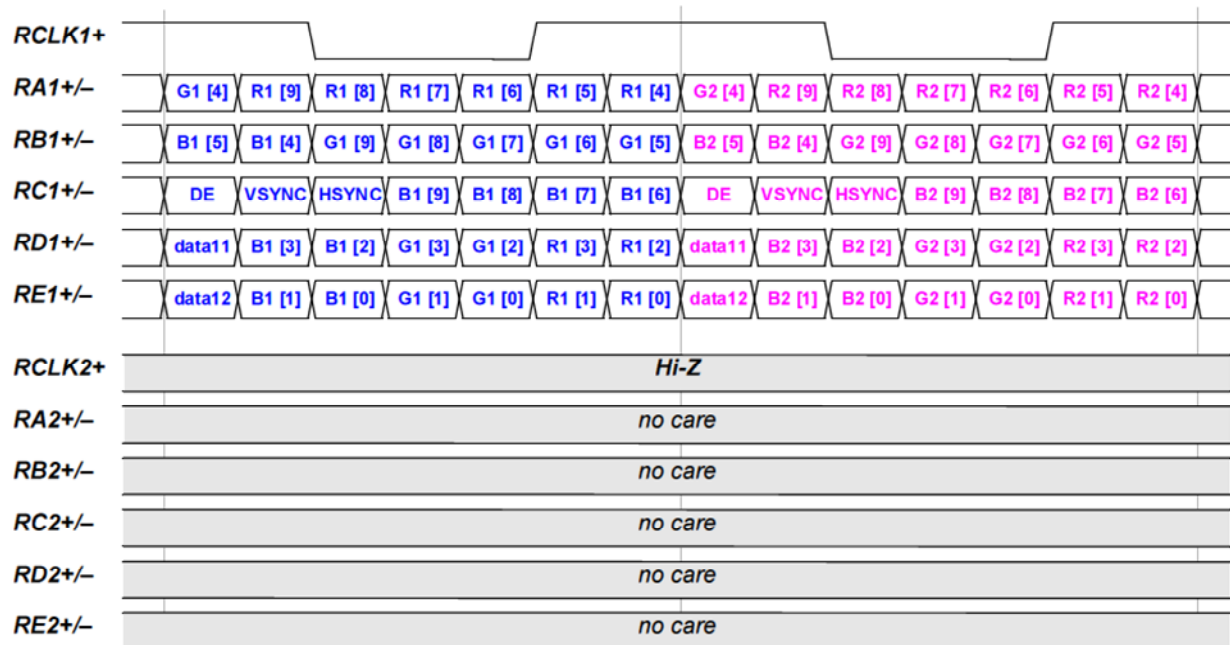
Figure 14-2. Data Mapping for Distribution mode



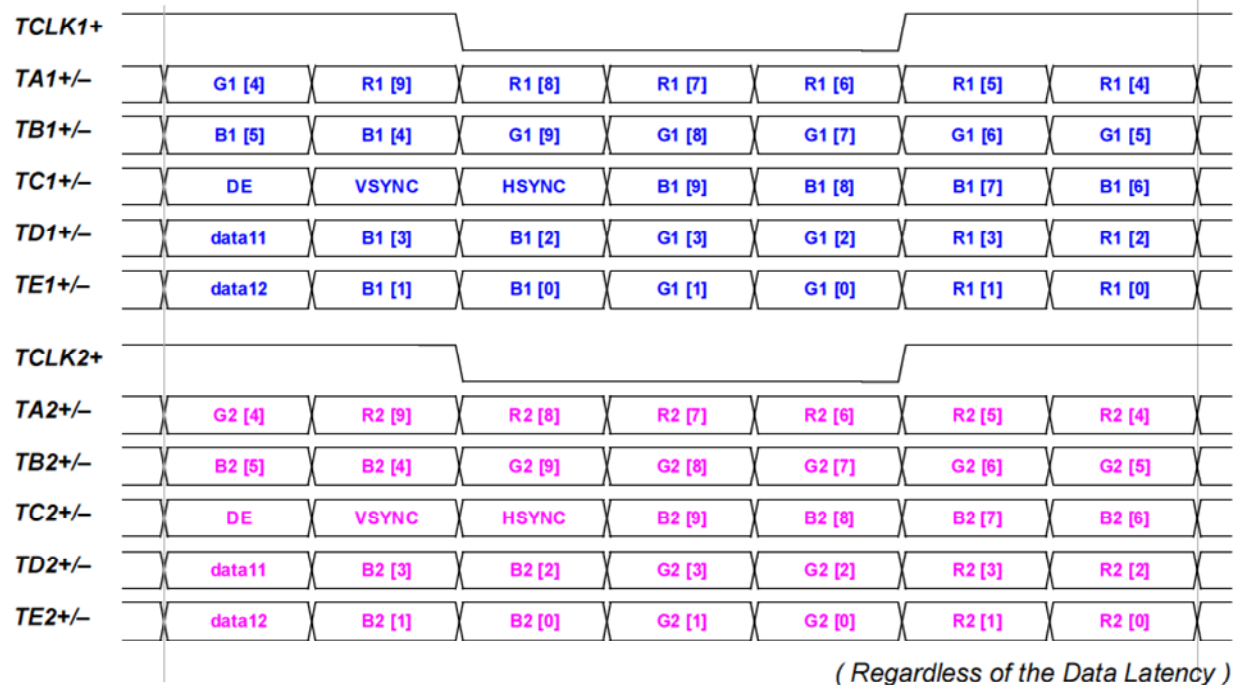
## Single-In / Dual-Out

In Single-in / Dual-out mode, RCLK2+/- must be Hi-Z.

### LVDS-Rx Input Mapping



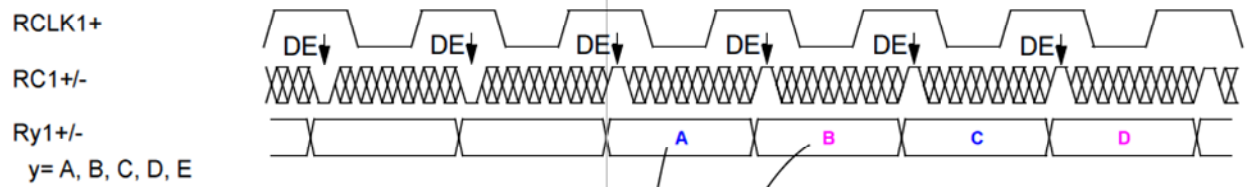
### LVDS-Tx Output Mapping



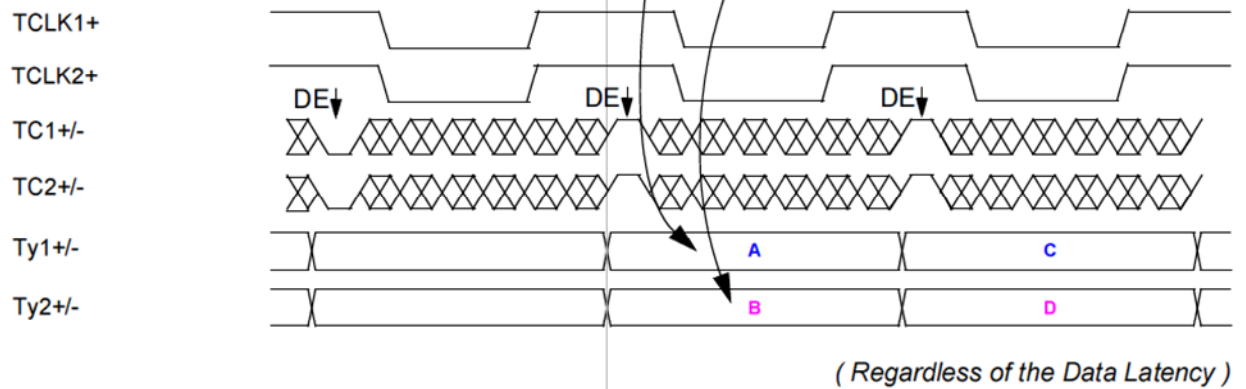
Data bits "data11, data12" are available for additional data transmission.

Figure 14-3(a). Data Mapping for Single-In/Dual-Out

### Single Link Input



### Dual Link Output



**Schematic diagram  
of DE transition**

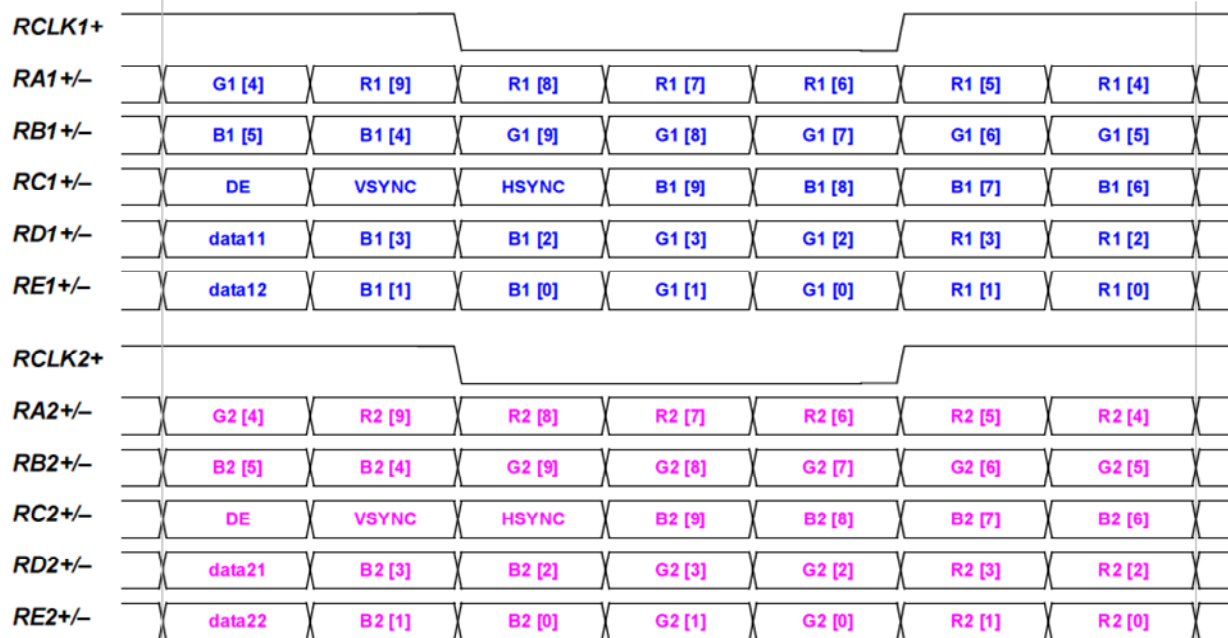


Single-in / Dual-out mode uses DE signal L-to-H-edge to start distribution of input data.

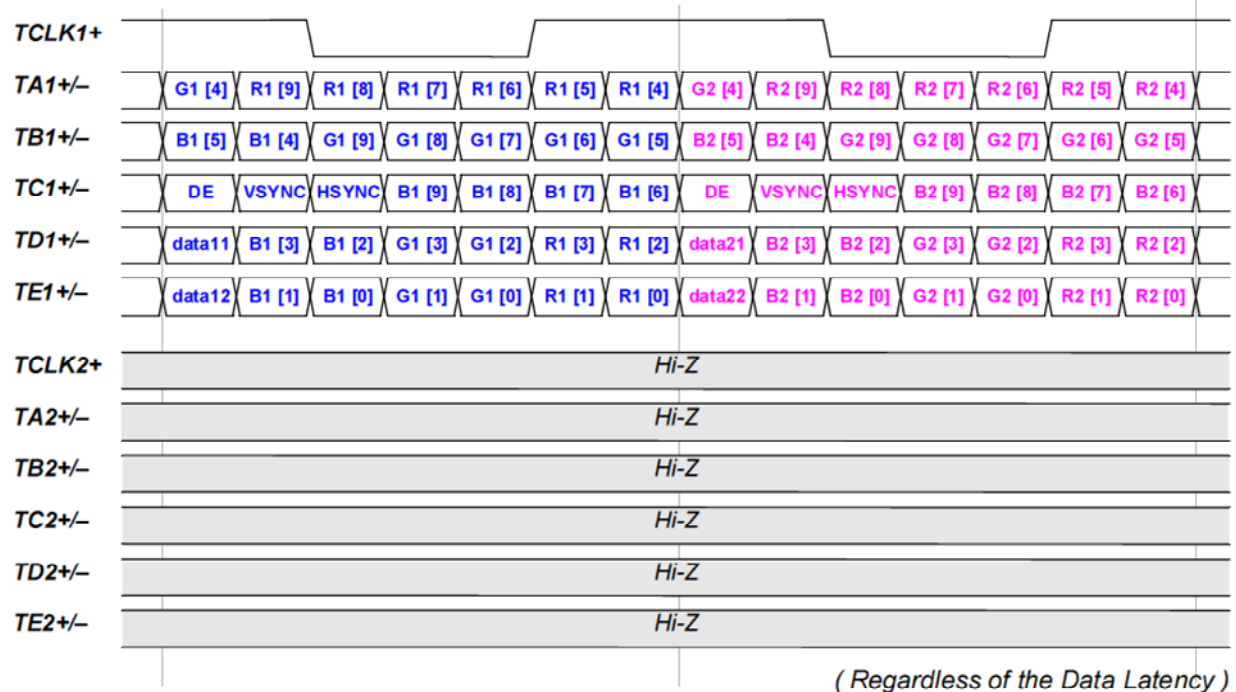
**Figure 14-3(b). Data Mapping for Single-In/Dual-Out**

## Dual-In / Single-Out

## LVDS-Rx Input Mapping



## LVDS-Tx Output Mapping



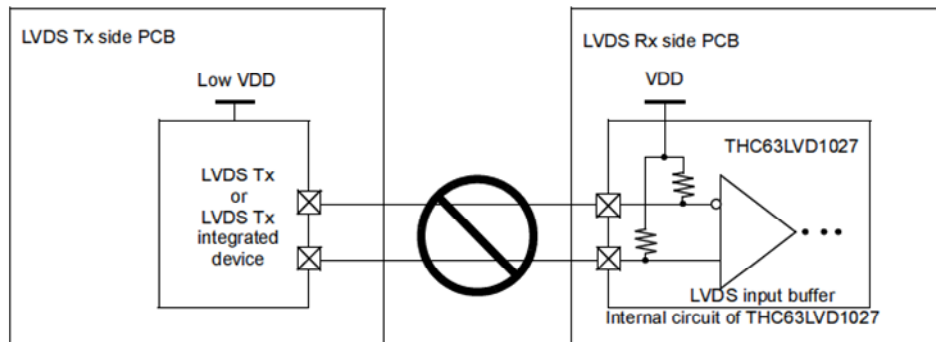
Data bits "data11, data12, data21, data22" are available for additional data transmission.

Figure 14-4. Data Mapping for Dual-In/Single-Out

## Notes

### 1) LVDS input pin connection

When LVDS line is not derived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.



**Figure 15. LVDS input pin connection**

### 2) Power On Sequence

Don't input RCLK1+/- and RCLK2+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.

### 3) Cable Connection and Disconnection

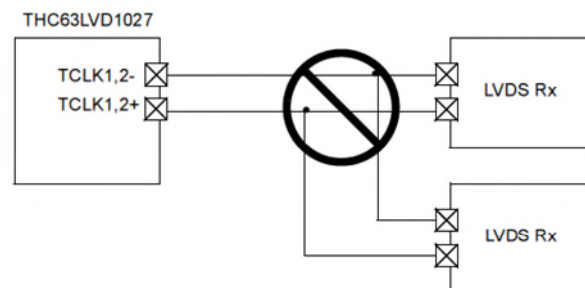
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

### 4) GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

### 5) Multi Drop Connection

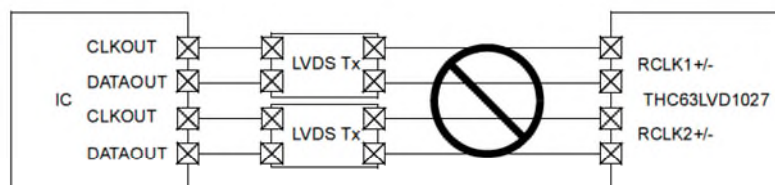
Multi drop connection is not recommended.



**Figure 16. Multi Drop Connection**

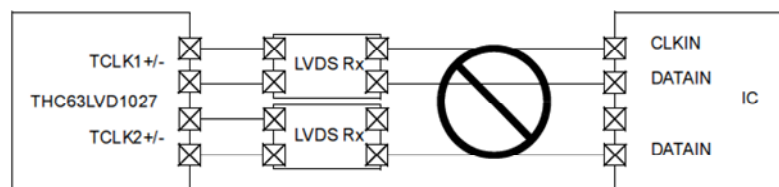
### 6) Asynchronous use

Asynchronous use such as following systems are not recommended. Page.11 tCK12 spec should be kept.



**Figure 17-1. Asynchronous Use1**

Asynchronous use such as following systems are not recommended.



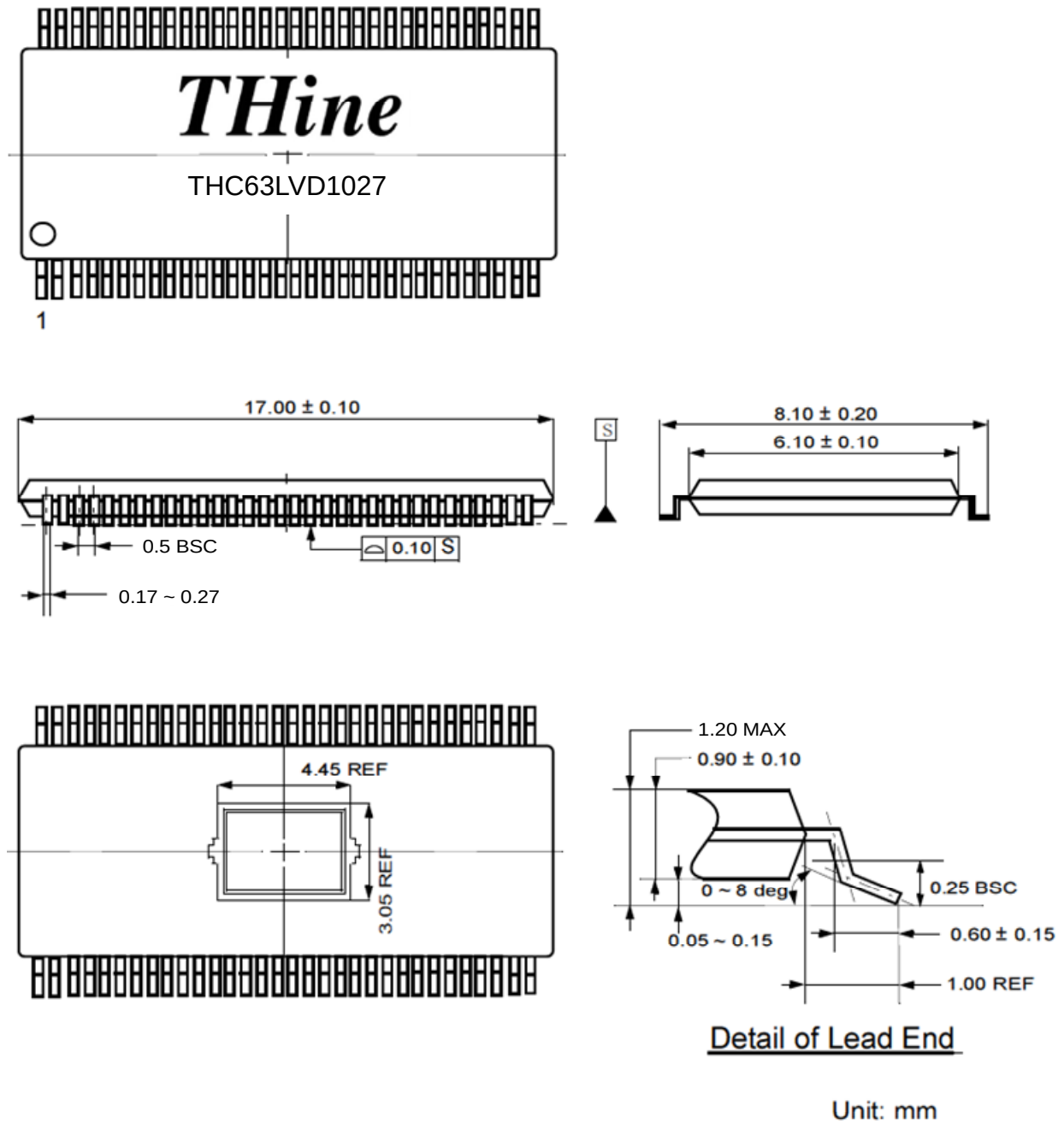
**Figure 17-2. Asynchronous Use2**

### 7) De-coupling capacitor

THC63LVD1027 requires appropriate de-coupling capacitor placement on VDD.

Especially, VDD pin 36 and pin 61 requires 0.1uF and 4.7nF capacitor parallel placement close to IC pins.

## Package



Exposed PAD is GND and must be soldered to PCB.

Figure 18. Package Diagram

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