

## TC74HC165AP, TC74HC165AF

### 8-Bit Shift Register (P-IN, S-OUT)

The TC74HC165A is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock inputs. When the  $\overline{\text{SHIFT}}/\overline{\text{LOAD}}$  input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.

When the  $\overline{\text{SHIFT}}/\overline{\text{LOAD}}$  input is held low, the parallel data is loaded asynchronously into the register at positive going transition of the clock pulse.

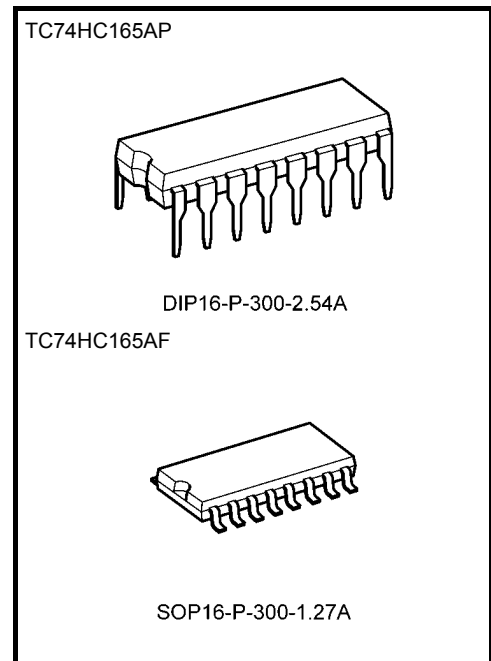
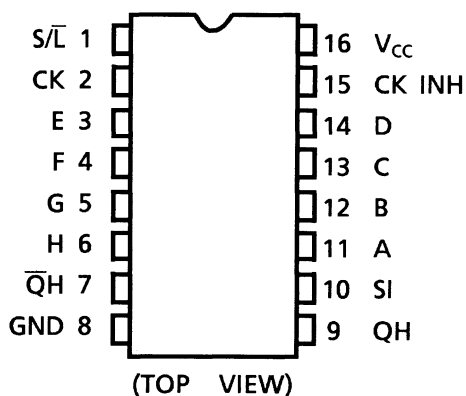
The CK-INH input should be shifted high only when the CK input is held high.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{\text{max}} = 56 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide operating voltage range:  $V_{\text{CC}} (\text{opr}) = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS165

### Pin Assignment

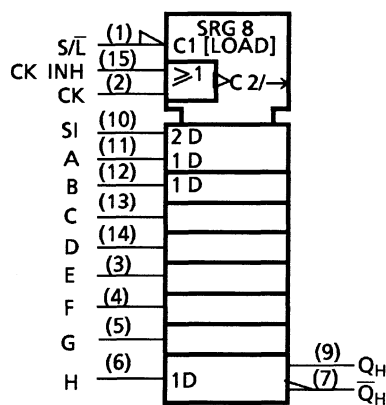


#### Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production  
1988-05

IEC Logic Symbol



Truth Table

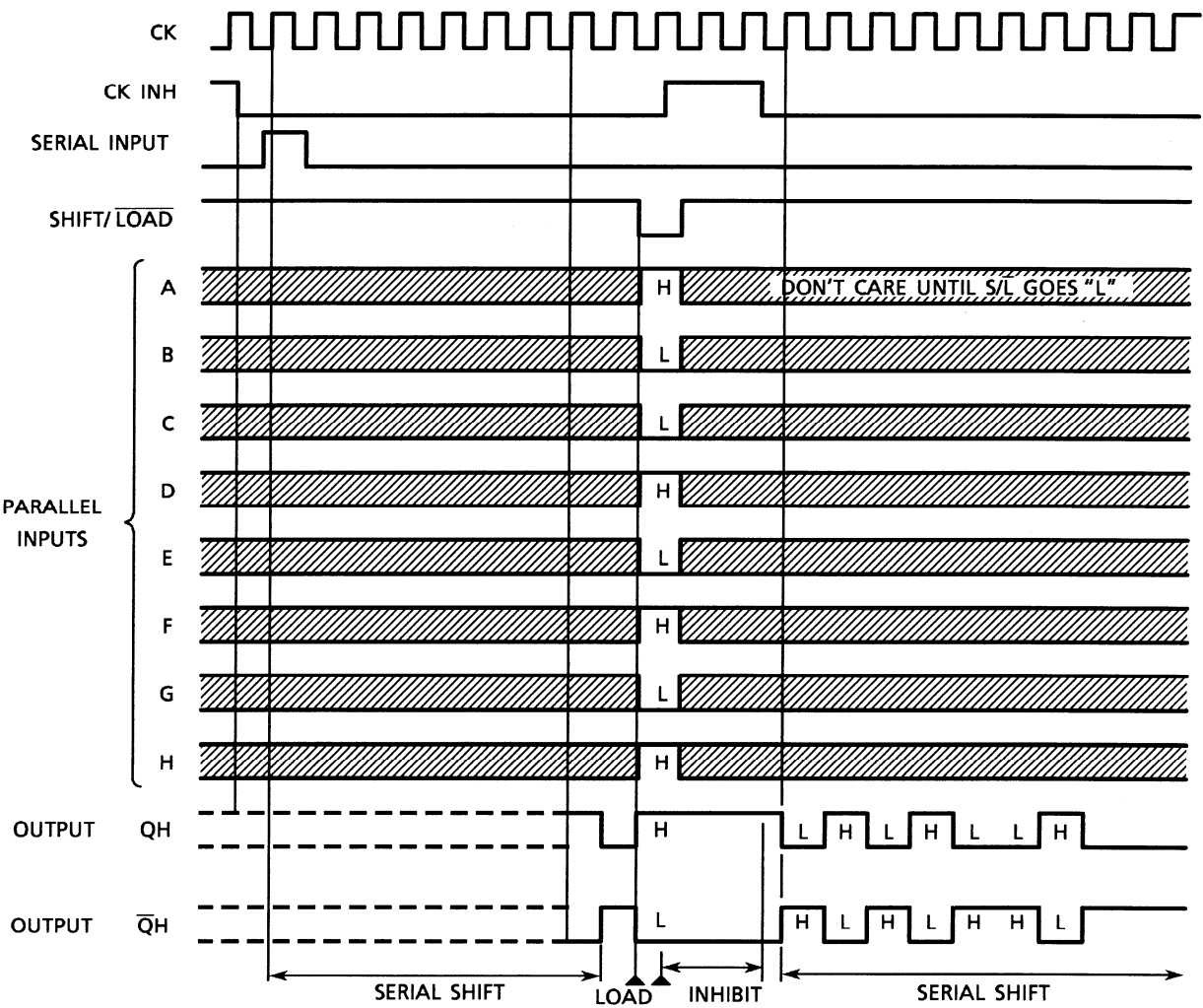
Inputs					Internal Outputs		Outputs	
SHIFT/LOAD	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A.....H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a.....h	a	b	h	$\overline{h}$
H	L		H	X	H	QAn	QGn	$\overline{QGn}$
H	L		L	X	L	QAn	QGn	$\overline{QGn}$
H		L	H	X	H	QAn	QGn	$\overline{QGn}$
H		L	L	X	L	QAn	QGn	$\overline{QGn}$
H	X	H	X	X	No Change			
H	H	X	X	X	No Change			

X: Don't care

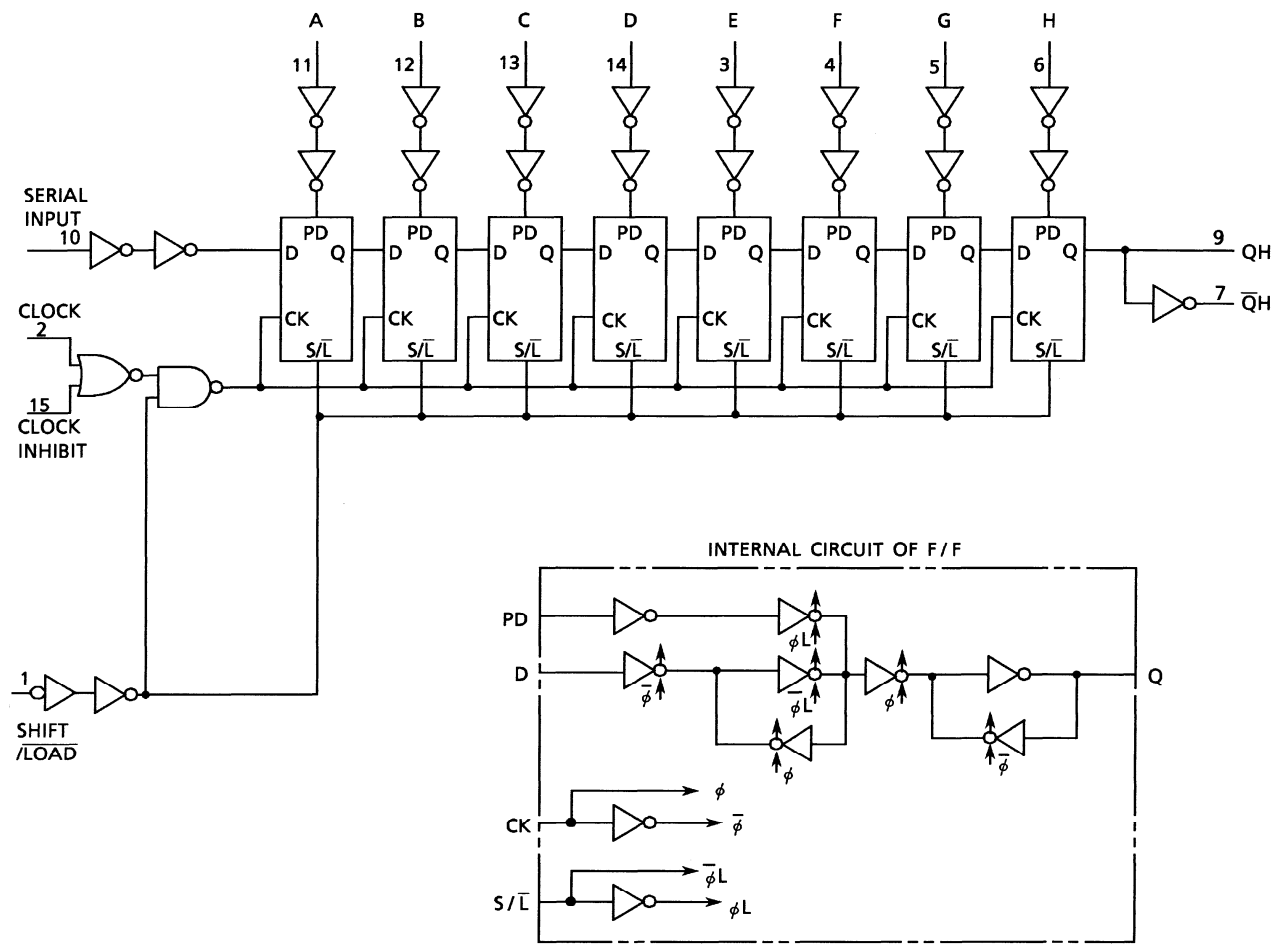
a.....h: The level of steady state input voltage at inputs A through H respectively

QAn~QGn: The level of QA~QG, respectively, before the most recent positive transition of the CK.

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  shall be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

## DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = –40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V	
Low-level input voltage	V <sub>IL</sub>	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	V	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			I <sub>OH</sub> = –4 mA I <sub>OH</sub> = –5.2 mA	6.0	5.9	6.0	—	5.9	—	
				4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 5.2 mA	6.0	—	0.0	0.1	—	0.1	
				4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (CK, CK INH)	$t_W$ (H) $t_W$ (L)	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum pulse width ( $S/\bar{L}$ )	$t_W$ (L)	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum set-up time (PI- $S/\bar{L}$ )	$t_s$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum set-up time (SI-CK, CK INH)	$t_s$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum set-up time ( $S/\bar{L}$ -CK, CK INH)	$t_s$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time (PI- $S/\bar{L}$ )	$t_h$	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Minimum hold time (SI-CK, CK INH)	$t_h$	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Minimum hold time ( $S/\bar{L}$ -CK, CK INH)	$t_h$	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Minimum removal time (CK INH-CK) (CK-CK INH)	$t_{rem}$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Clock frequency	f	—	2.0	—	7	MHz
			4.5	—	30	
			6.0	—	41	

AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$	—	—	4	8	ns
	$t_{THL}$					
Propagation delay time (CK, CK INH-QH, $\bar{Q}H$ )	$t_{PLH}$	—	—	15	25	ns
	$t_{PHL}$					
Propagation delay time ( $S/\bar{L}$ -QH, $\bar{Q}H$ )	$t_{PLH}$	—	—	15	25	ns
	$t_{PHL}$					
Propagation delay time (H-QH, $\bar{Q}H$ )	$t_{PLH}$	—	—	14	26	ns
	$t_{PHL}$					
Maximum clock frequency	$f_{max}$	—	35	56	—	MHz

AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	25	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation delay time (CK, CK INH-QH, $\overline{QH}$ )	$t_{PLH}$ $t_{PHL}$	—	2.0	—	55	150	—	190
			4.5	—	18	30	—	38
			6.0	—	15	26	—	33
Propagation delay time (S/L-QH, $\overline{QH}$ )	$t_{PLH}$ $t_{PHL}$	—	2.0	—	60	165	—	205
			4.5	—	19	33	—	41
			6.0	—	16	28	—	35
Propagation delay time (H-QH, $\overline{QH}$ )	$t_{PHL}$	—	2.0	—	52	135	—	170
			4.5	—	17	27	—	34
			6.0	—	14	23	—	29
Maximum clock frequency	$f_{max}$	—	2.0	7	14	—	6	—
			4.5	30	46	—	24	—
			6.0	41	65	—	28	—
Input capacitance	$C_{IN}$	—	—	—	5	10	—	10
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	—	55	—	—	—

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

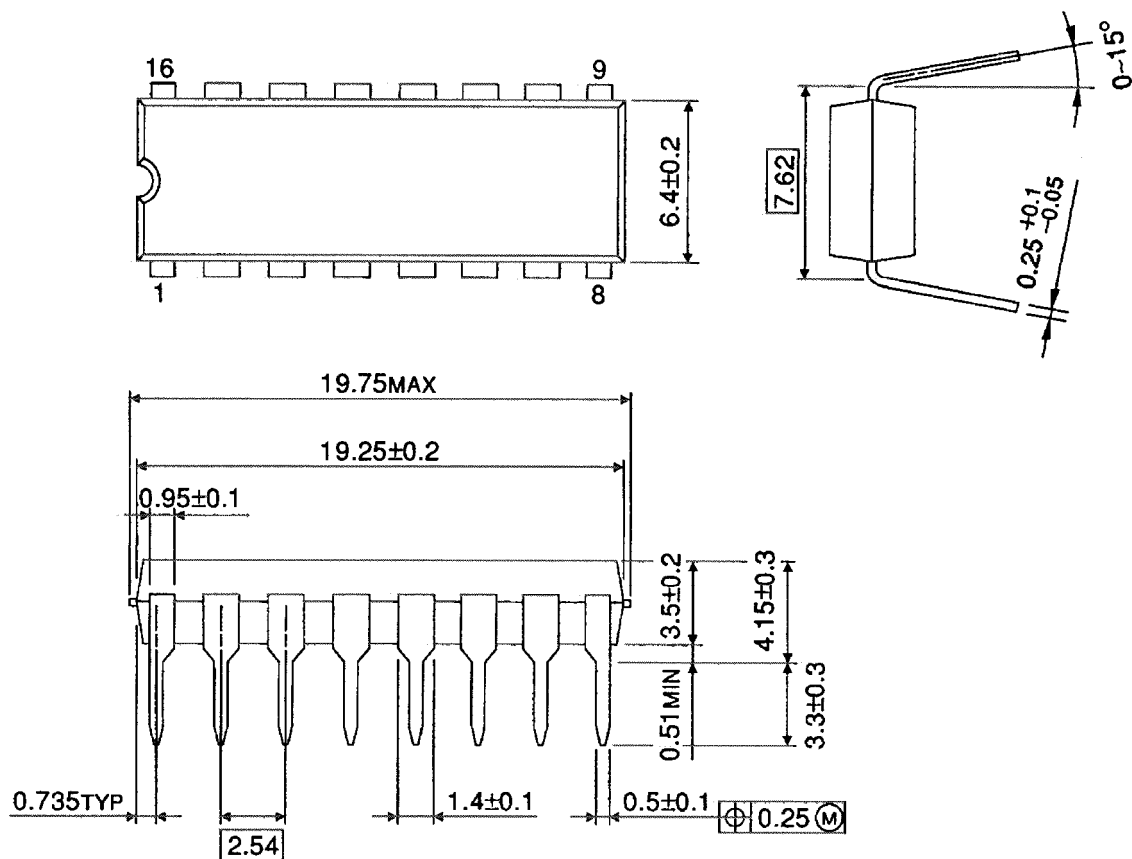
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm



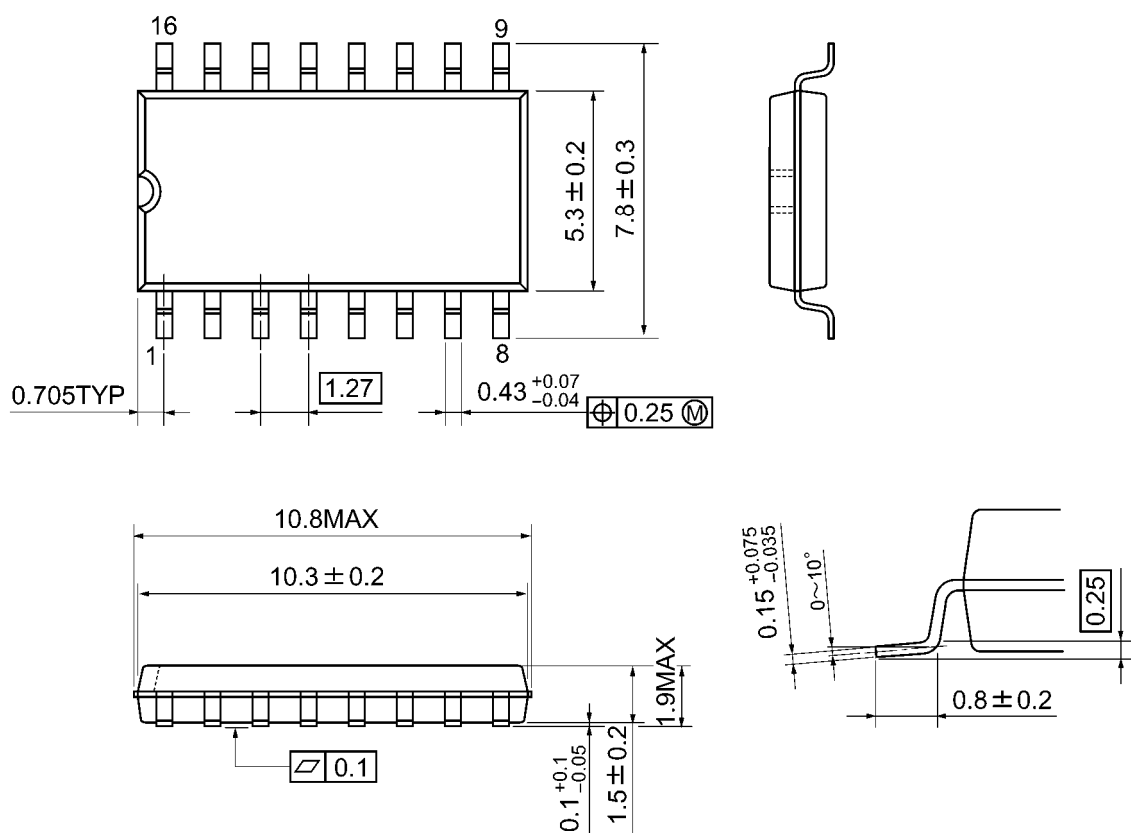
Weight: 1.00 g (typ.)



## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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