

# SNx4AHCT02 Quadruple 2-Input Positive-NOR Gates

## 1 Features

- Operating range of 4.5V to 5.5V
- Low power consumption, 10μA maximum  $I_{CC}$
- ±8mA output drive at 5V
- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17

## 2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)

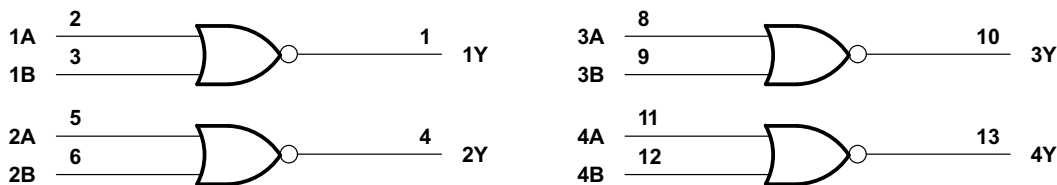
## 3 Description

These devices contain four independent 2-input NOR gates that perform the Boolean function  $Y = \overline{A} \times \overline{B}$  or  $Y = \overline{A + B}$  in positive logic.

### Device Information

| PART NUMBER | RATING     | PACKAGE SIZE <sup>(1)</sup> |
|-------------|------------|-----------------------------|
| SN54AHCT02  | Military   | J (CDIP, 14)                |
|             |            | W (CFP, 14)                 |
|             |            | FK (LCCC, 20)               |
| SN74AHCT02  | Commercial | D (SOIC, 14)                |
|             |            | DB (SSOP, 14)               |
|             |            | DGV (TVSOP, 14)             |
|             |            | N (PDIP, 14)                |
|             |            | NS (SOP, 14)                |
|             |            | PW (SOP, 14)                |
|             |            | RGY (VQFN, 14)              |
|             |            | BQA (WQFN, 14)              |

(1) For more information, see [Section 11](#).



Logic Diagram (Positive Logic)

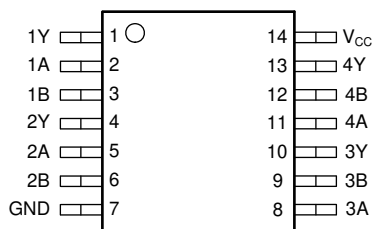


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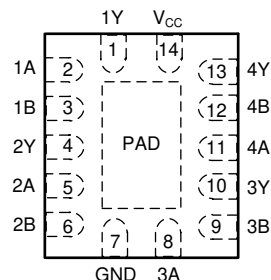
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## 4 Pin Configuration and Functions

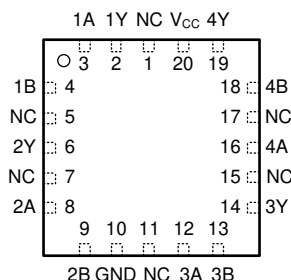


**Figure 4-1. SN54AHCT02 J or W Package, 14-Pin (Top View)**

**SN74AHCT02 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)**



**Figure 4-2. SN74AHCT02 RGY or BQA Package, 14-Pin (Top View)**



**Figure 4-3. SN54AHCT02 FK Package, 20-Pin (Top View)**

**Table 4-1. Pin Functions**

| NAME            | PIN                                              |                    |                        | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----------------|--------------------------------------------------|--------------------|------------------------|---------------------|---------------|
|                 | SN74AHCT02<br>D, DB, DGV, N, NS,<br>PW, RGY, BQA | SN54AHCT02<br>J, W | FK                     |                     |               |
| 1A              | 2                                                | 2                  | 3                      | I                   | 1A Input      |
| 1B              | 3                                                | 3                  | 4                      | I                   | 1B Input      |
| 1Y              | 1                                                | 1                  | 2                      | O                   | 1Y Output     |
| 2A              | 5                                                | 5                  | 8                      | I                   | 2A Input      |
| 2B              | 6                                                | 6                  | 9                      | I                   | 2B Input      |
| 2Y              | 4                                                | 4                  | 6                      | O                   | 2Y Output     |
| 3A              | 8                                                | 8                  | 12                     | I                   | 3A Input      |
| 3B              | 9                                                | 9                  | 13                     | I                   | 3B Input      |
| 3Y              | 10                                               | 20                 | 14                     | O                   | 3Y Output     |
| 4A              | 11                                               | 11                 | 16                     | I                   | 4A Input      |
| 4B              | 12                                               | 12                 | 18                     | I                   | 4B Input      |
| 4Y              | 13                                               | 13                 | 19                     | O                   | 4Y Output     |
| GND             | 7                                                | 7                  | 10                     | —                   | Ground Pin    |
| NC              | —                                                | —                  | 1, 5, 7,<br>11, 15, 17 | —                   | No Connection |
| V <sub>CC</sub> | 14                                               | 14                 | 20                     | —                   | Power Pin     |

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                                             | MIN  | MAX            | UNIT |
|-------------------------------------------------------------|------|----------------|------|
| Supply voltage range, $V_{CC}$                              | -0.5 | 7              | V    |
| Input voltage range, $V_I$ <sup>(2)</sup>                   | -0.5 | 7              | V    |
| Output voltage range, $V_O$ <sup>(2)</sup>                  | -0.5 | $V_{CC} + 0.5$ | V    |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                 |      | -20            | mA   |
| Output clamp current, $I_O$ ( $V_O < 0$ or $V_O > V_{CC}$ ) |      | ±20            | mA   |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )  |      | ±25            | mA   |
| Continuous current through $V_{CC}$ or GND                  |      | ±50            | mA   |
| Storage temperature range, $T_{stg}$                        | -65  | 150            | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|                                     | VALUE                                                                 | UNIT  |
|-------------------------------------|-----------------------------------------------------------------------|-------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 |
|                                     | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±1000 |
|                                     |                                                                       | V     |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

|                     |                                    | SN54AHCT02 |          | SN74AHCT02 |          | UNIT |
|---------------------|------------------------------------|------------|----------|------------|----------|------|
|                     |                                    | MIN        | MAX      | MIN        | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 4.5        | 5.5      | 4.5        | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2          |          | 2          |          | V    |
| $V_{IL}$            | Low-level input voltage            |            | 0.8      |            | 0.8      | V    |
| $V_I$               | Input voltage                      | 0          | 5.5      | 0          | 5.5      | V    |
| $V_O$               | Output voltage                     | 0          | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |            | -8       |            | -8       | mA   |
| $I_{OL}$            | Low-level output current           |            | 8        |            | 8        | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |            | 20       |            | 20       | ns/V |
| $T_A$               | Operating free-air temperature     | -55        | 125      | -40        | 125      | °C   |

### 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | SNx4AHCT02 |         |         |         |         | UNIT |
|-------------------------------|----------------------------------------|------------|---------|---------|---------|---------|------|
|                               |                                        | D          | DB      | NS      | PW      | RGY     |      |
|                               |                                        | 14 PINS    | 14 PINS | 14 PINS | 14 PINS | 14 PINS |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance | 86         | 96      | 76      | 113     | 87.1    | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS                                             | VCC          | TA = 25°C |     |      | SN54AHCT02 |                   | SN74AHCT02 |      | UNIT |
|---------------------------------|-------------------------------------------------------------|--------------|-----------|-----|------|------------|-------------------|------------|------|------|
|                                 |                                                             |              | MIN       | TYP | MAX  | MIN        | MAX               | MIN        | MAX  |      |
| VOH                             | I <sub>OH</sub> = -50 µA                                    | 4.5 V        | 4.4       | 4.5 |      | 4.4        |                   | 4.4        |      | V    |
|                                 | I <sub>OH</sub> = -8 mA                                     |              | 3.94      |     |      | 3.8        |                   | 3.8        |      |      |
| VOL                             | I <sub>OL</sub> = 50 µA                                     | 4.5 V        |           |     | 0.1  |            | 0.1               |            | 0.1  | V    |
|                                 | I <sub>OL</sub> = 8 mA                                      |              |           |     | 0.36 |            | 0.44              |            | 0.44 |      |
| I <sub>I</sub>                  | V <sub>I</sub> = 5.5 V or GND                               | 0 V to 5.5 V |           |     | ±0.1 |            | ±1 <sup>(1)</sup> |            | ±1   | µA   |
| I <sub>CC</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V        |           |     | 2    |            | 20                |            | 20   | µA   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | One input at 3.4 V,<br>Other inputs at GND<br>or VCC        | 5.5 V        |           |     | 1.35 |            | 1.5               |            | 1.5  | mA   |
| C <sub>i</sub>                  | V <sub>I</sub> = VCC or GND                                 | 5 V          |           | 4   | 10   |            |                   |            | 10   | pF   |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.6 Switching Characteristics

over operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted). See [Figure 6-1](#)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | TA = 25°C |                    |                    | SN54AHCT02       |                    | SN74AHCT02 |     | UNIT |
|------------------|-----------------|----------------|------------------------|-----------|--------------------|--------------------|------------------|--------------------|------------|-----|------|
|                  |                 |                |                        | MIN       | TYP                | MAX                | MIN              | MAX                | MIN        | MAX |      |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 15 pF |           | 2.4 <sup>(1)</sup> | 5.5 <sup>(1)</sup> | 1 <sup>(1)</sup> | 6.5 <sup>(1)</sup> | 1          | 6.5 | ns   |
| t <sub>PHL</sub> |                 |                |                        |           | 3.5 <sup>(1)</sup> | 5.5 <sup>(1)</sup> | 1 <sup>(1)</sup> | 6.5 <sup>(1)</sup> | 1          | 6.5 |      |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 50 pF |           | 3.4                | 7.5                | 1                | 8.5                | 1          | 8.5 | ns   |
| t <sub>PHL</sub> |                 |                |                        |           | 4.5                | 7.5                | 1                | 8.5                | 1          | 8.5 |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.7 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                        | SN74AHCT02 |      |     | UNIT |
|------------------------------------------------------------------|------------|------|-----|------|
|                                                                  | MIN        | TYP  | MAX |      |
| V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub> |            | 0.8  |     | V    |
| V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub> |            | -0.8 |     | V    |
| V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub> |            | 4.7  |     | V    |
| V <sub>IH(D)</sub> High-level dynamic input voltage              |            | 2    |     | V    |
| V <sub>IL(D)</sub> Low-level dynamic input voltage               |            | 0.8  |     | V    |

(1) Characteristics are for surface-mount packages only.

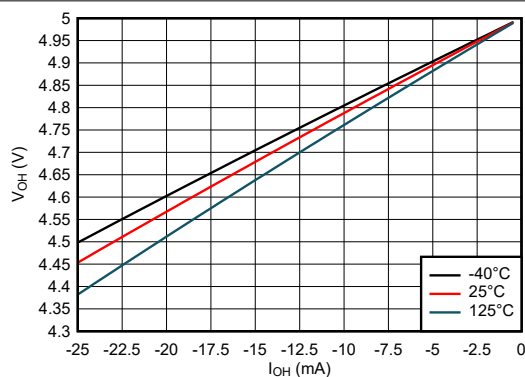
## 5.8 Operating Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

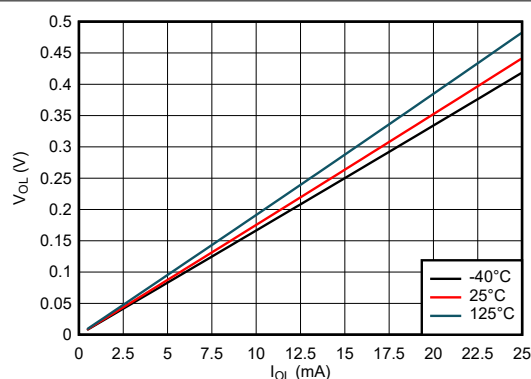
| PARAMETER                                     | TEST CONDITIONS    | TYP | UNIT |
|-----------------------------------------------|--------------------|-----|------|
| C <sub>pd</sub> Power dissipation capacitance | No load, f = 1 MHz | 17  | pF   |

## 5.9 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

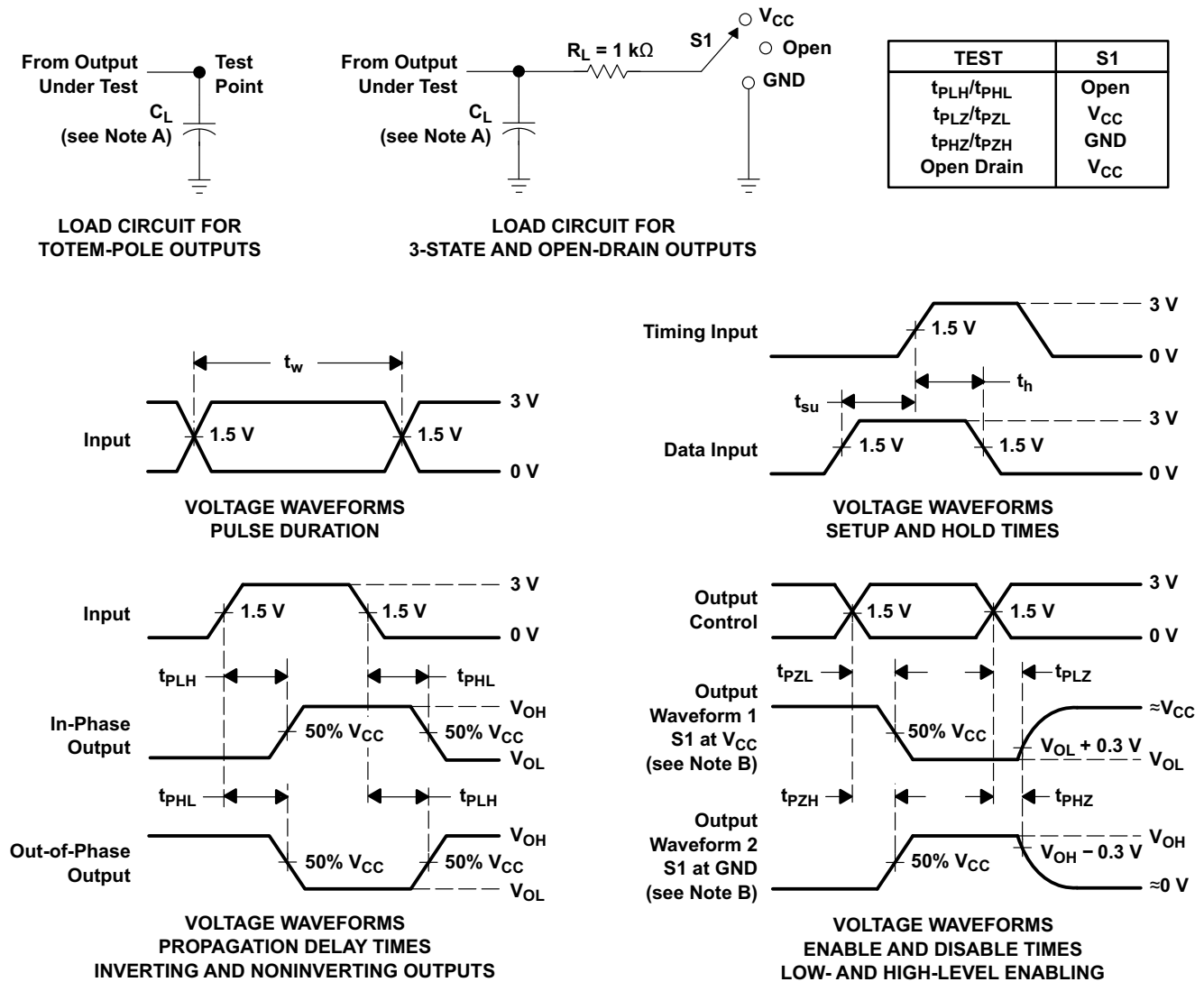


**Figure 5-1. Output Voltage vs Current in HIGH State; 5-V Supply**



**Figure 5-2. Output Voltage vs Current in LOW State; 5-V Supply**

## 6 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

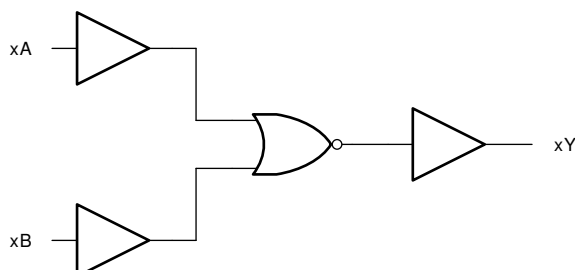
**Figure 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

This device contains four independent 2-input NOR Gates. Each gate performs the Boolean function  $Y = \overline{A + B}$  in positive logic.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

#### 7.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

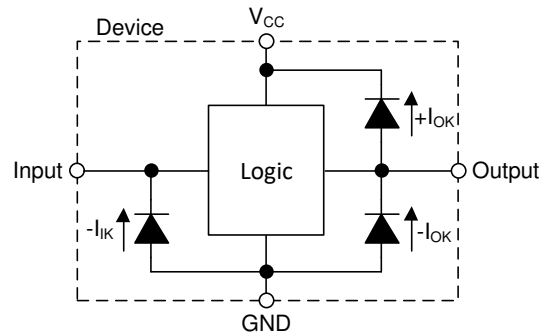
Unused push-pull CMOS outputs should be left disconnected.

#### 7.3.3 Clamp Diode Structure

As [Figure 7-1](#) shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS <sup>(1)</sup> |   | OUTPUT Y |
|-----------------------|---|----------|
| A                     | B |          |
| H                     | X | L        |
| X                     | H | L        |
| L                     | L | H        |

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

In this application, two 2-input NOR gates are used to create an SR latch as shown in [Figure 8-1](#). The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SNx4AHCT02 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs HIGH, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a HIGH signal to the R input which returns the Q output back to LOW.

The user can add a small RC to the feedback path of the NOR gates to default the output to a certain state, which can create slow transition rates. This fact makes the SNx4AHCT02 suitable for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

### 8.2 Typical Application

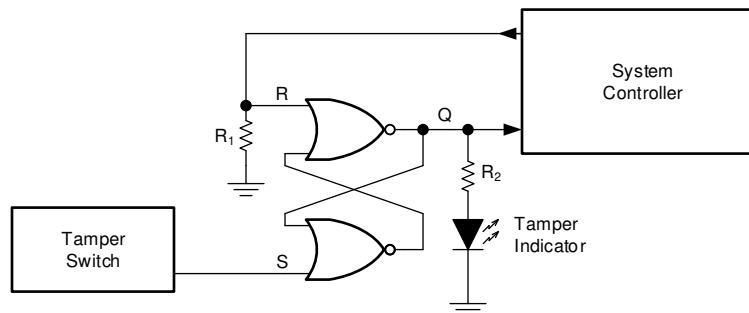


Figure 8-1. Typical Application Block Diagram

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4AHCT02 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SNx4AHCT02 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SNx4AHCT02 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OL}$ . When outputting in the HIGH state, the output

voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4AHCT02 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

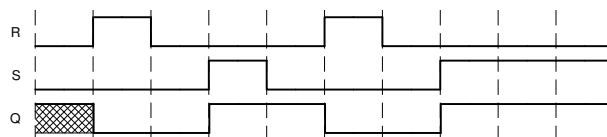
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50\text{pF}$ . This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4AHCT02 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 8.2.3 Application Curves



**Figure 8-2. Application Timing Diagram**

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

#### 8.4.2 Layout Example

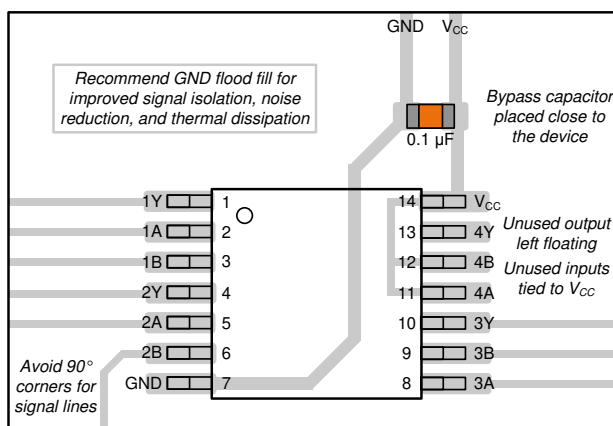


Figure 8-3. Example Layout for the SNx4AHCT02

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision M (May 2023) to Revision N (February 2024)</b> | <b>Page</b> |
|-------------------------------------------------------------------------|-------------|
| • Updated RθJA values: RGY = 47 to 87.1, all values in °C/W .....       | <b>4</b>    |

| <b>Changes from Revision L (July 2003) to Revision M (May 2023)</b>                                   | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------|-------------|
| • Updated the <i>Features</i> section.....                                                            | <b>1</b>    |
| • Added the <i>Applications</i> section.....                                                          | <b>1</b>    |
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | <b>1</b>    |
| • Updated the <i>Device Information</i> table to include <i>Channel Count</i> .....                   | <b>1</b>    |
| • Added the <i>BQA</i> package to the data sheet.....                                                 | <b>1</b>    |
| • Added the <i>Pin Configuration and Functions</i> section.....                                       | <b>3</b>    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                      |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------------|
| <a href="#">5962-9757101Q2A</a> | Active        | Production           | LCCC (FK)   20   | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9757101Q2A<br>SNJ54AHCT<br>02FK |
| <a href="#">5962-9757101QCA</a> | Active        | Production           | CDIP (J)   14    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9757101QC<br>A<br>SNJ54AHCT02J      |
| <a href="#">5962-9757101QDA</a> | Active        | Production           | CFP (W)   14     | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9757101QD<br>A<br>SNJ54AHCT02W      |
| <a href="#">SN74AHCT02BQAR</a>  | Active        | Production           | WQFN (BQA)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AHCT02                                   |
| <a href="#">SN74AHCT02D</a>     | Obsolete      | Production           | SOIC (D)   14    | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | AHCT02                                   |
| <a href="#">SN74AHCT02DBR</a>   | Active        | Production           | SSOP (DB)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB02                                     |
| <a href="#">SN74AHCT02DGV</a>   | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB02                                     |
| <a href="#">SN74AHCT02DR</a>    | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AHCT02                                   |
| <a href="#">SN74AHCT02N</a>     | Active        | Production           | PDIP (N)   14    | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74AHCT02N                              |
| <a href="#">SN74AHCT02NSR</a>   | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AHCT02                                   |
| <a href="#">SN74AHCT02PW</a>    | Obsolete      | Production           | TSSOP (PW)   14  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HB02                                     |
| <a href="#">SN74AHCT02PWR</a>   | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | HB02                                     |
| <a href="#">SN74AHCT02RGYR</a>  | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-2-260C-1 YEAR               | -40 to 85    | HB02                                     |
| <a href="#">SNJ54AHCT02FK</a>   | Active        | Production           | LCCC (FK)   20   | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9757101Q2A<br>SNJ54AHCT<br>02FK |
| <a href="#">SNJ54AHCT02J</a>    | Active        | Production           | CDIP (J)   14    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9757101QC<br>A<br>SNJ54AHCT02J      |
| <a href="#">SNJ54AHCT02W</a>    | Active        | Production           | CFP (W)   14     | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9757101QD<br>A<br>SNJ54AHCT02W      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHCT02, SN74AHCT02 :**

- Catalog : [SN74AHCT02](#)
- Automotive : [SN74AHCT02-Q1](#), [SN74AHCT02-Q1](#)
- Military : [SN54AHCT02](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT02BQAR | WQFN         | BQA             | 14   | 3000 | 180.0              | 12.4               | 2.8     | 3.3     | 1.1     | 4.0     | 12.0   | Q1            |
| SN74AHCT02DBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74AHCT02DGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHCT02DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74AHCT02NSR  | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74AHCT02PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHCT02PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHCT02RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT02BQAR | WQFN         | BQA             | 14   | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHCT02DBR  | SSOP         | DB              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHCT02DGVR | TVSOP        | DGV             | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHCT02DR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74AHCT02NSR  | SOP          | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHCT02PWR  | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74AHCT02PWR  | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHCT02RGYR | VQFN         | RGY             | 14   | 3000 | 360.0       | 360.0      | 36.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9757101Q2A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-9757101QDA | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74AHCT02N     | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AHCT02N     | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54AHCT02FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54AHCT02W    | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

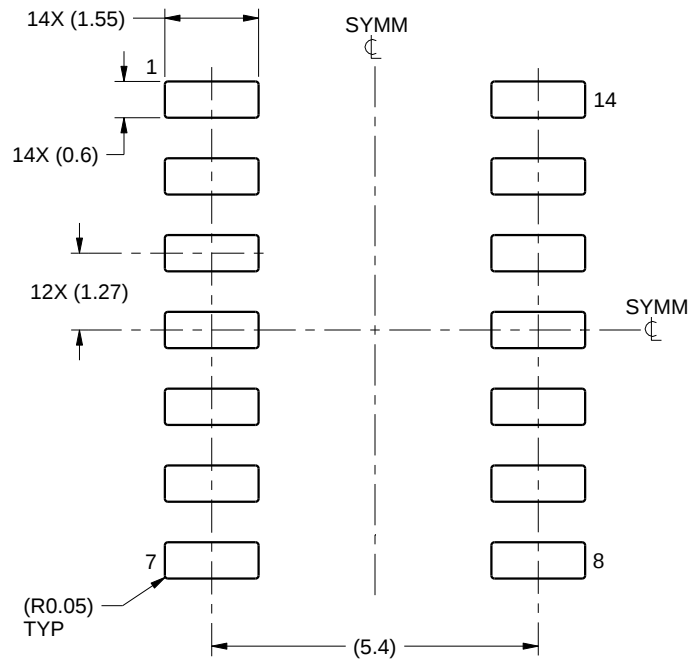
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

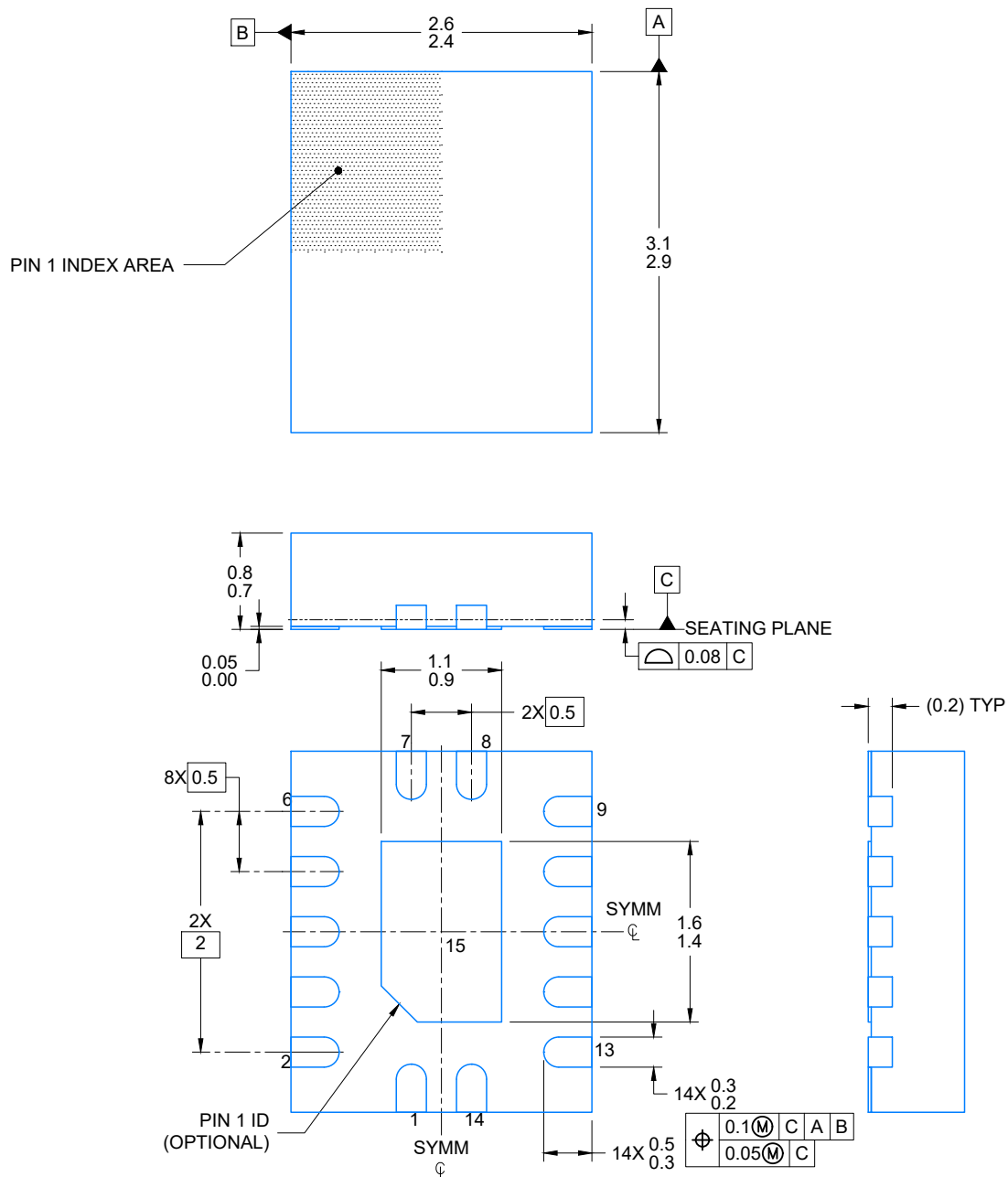
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A

**WQFN - 0.8 mm max height**

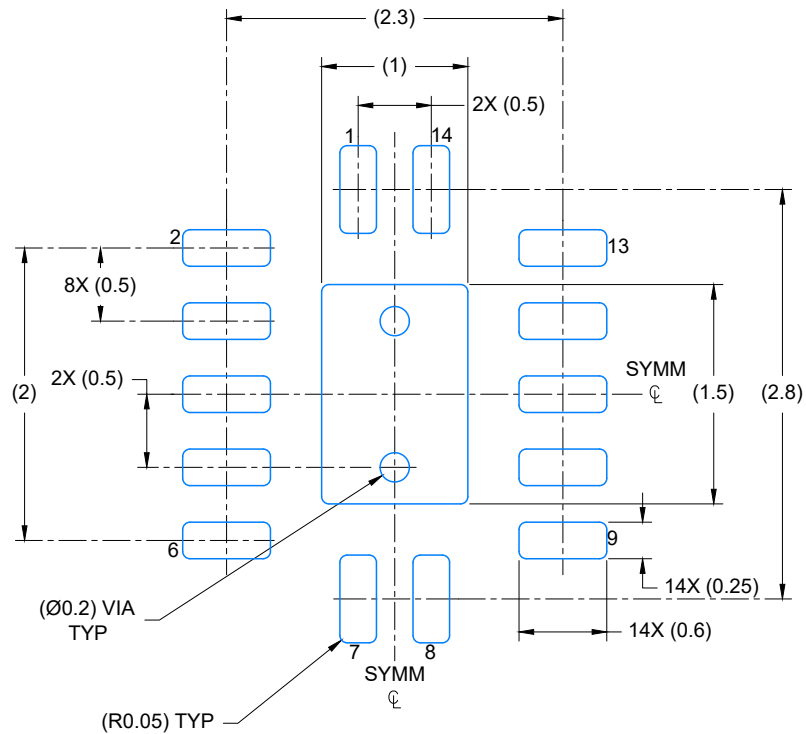
PLASTIC QUAD FLAT PACK-NO LEAD



4224636/A 11/2018

NOTES:

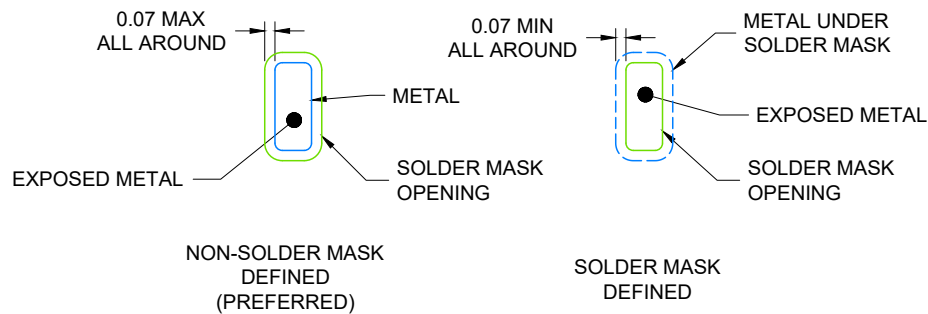
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

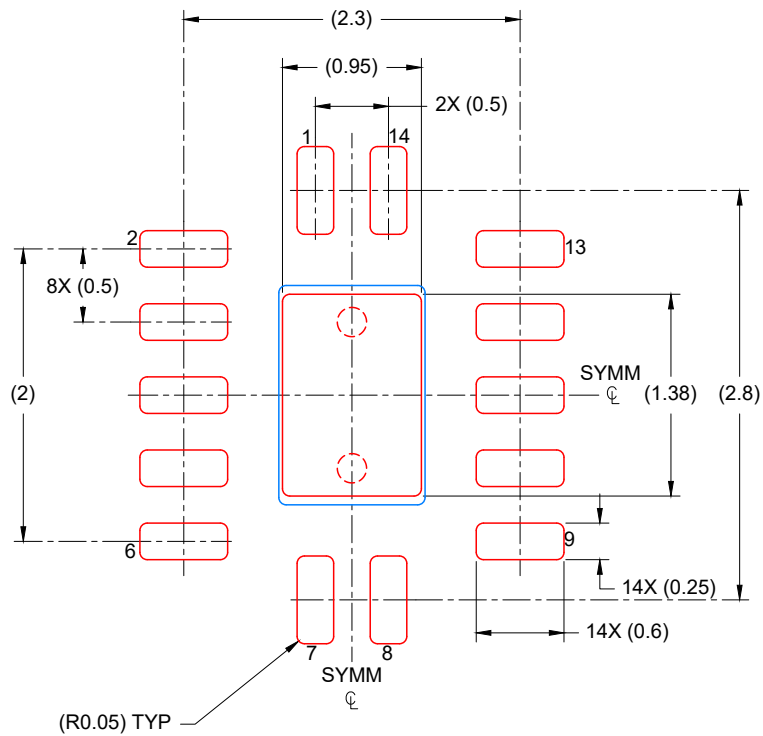
SCALE: 20X



4224636/A 11/2018

## NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

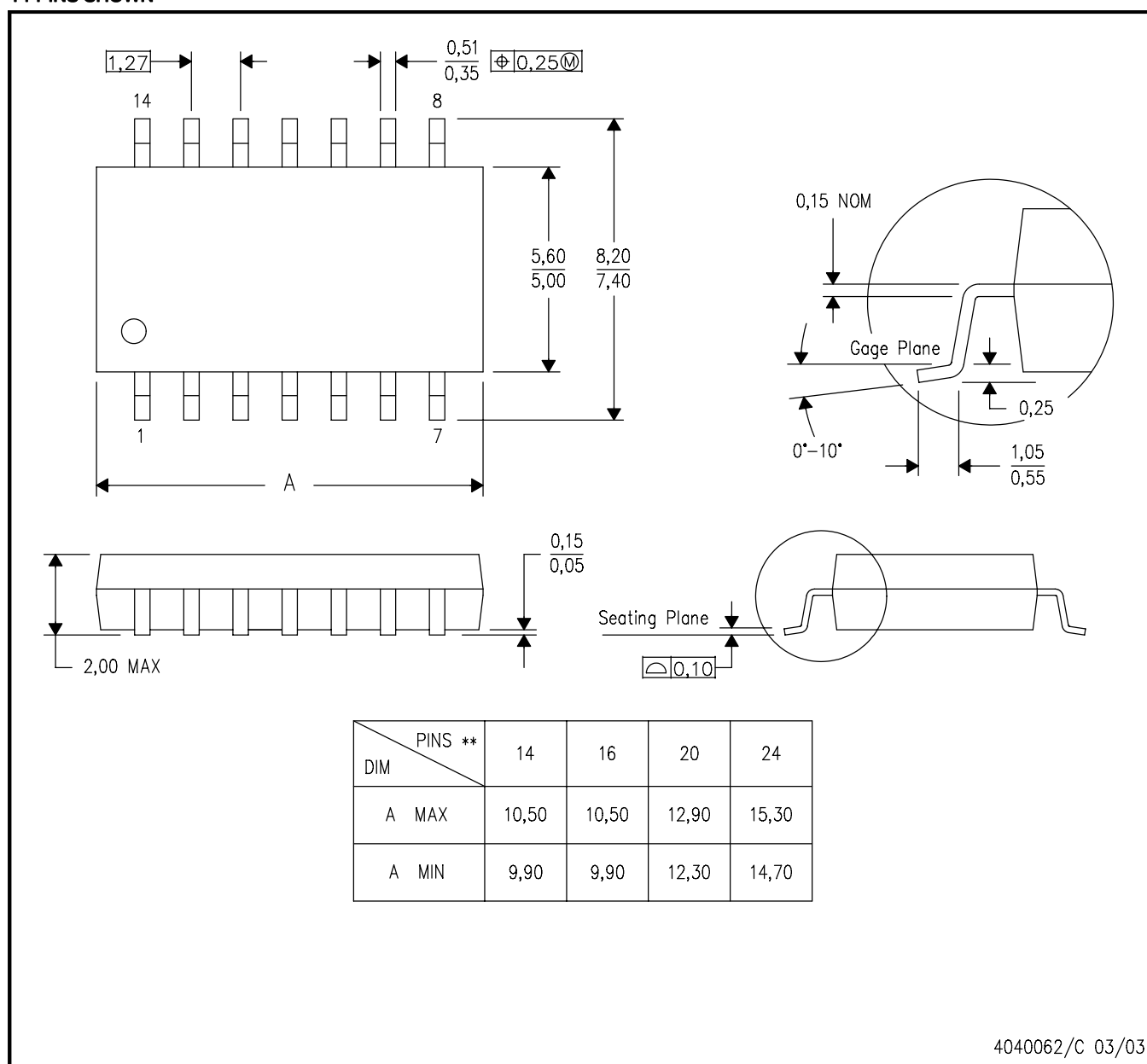
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14



4220762/A 05/2024

## NOTES:

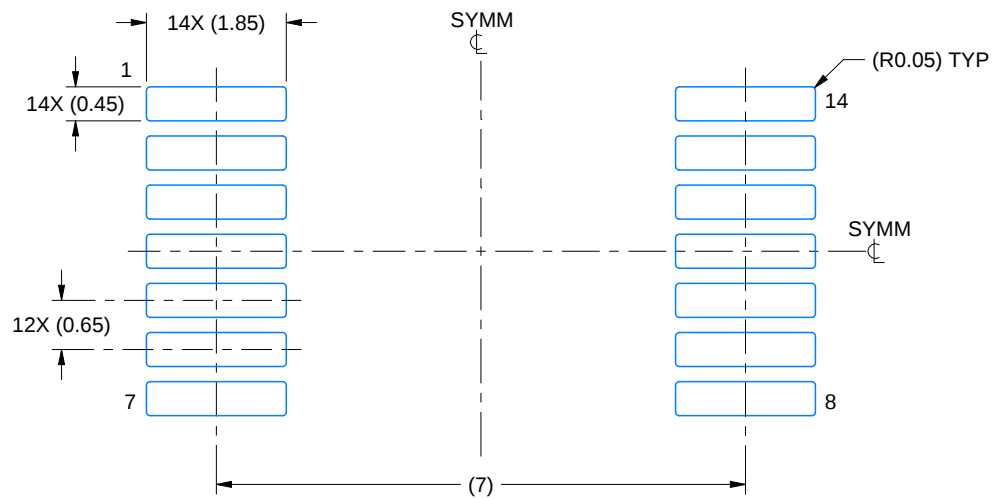
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

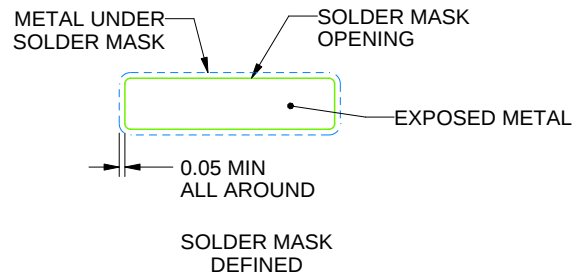
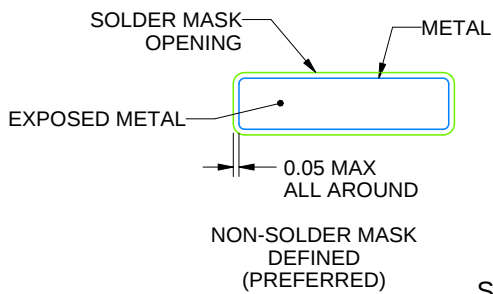
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

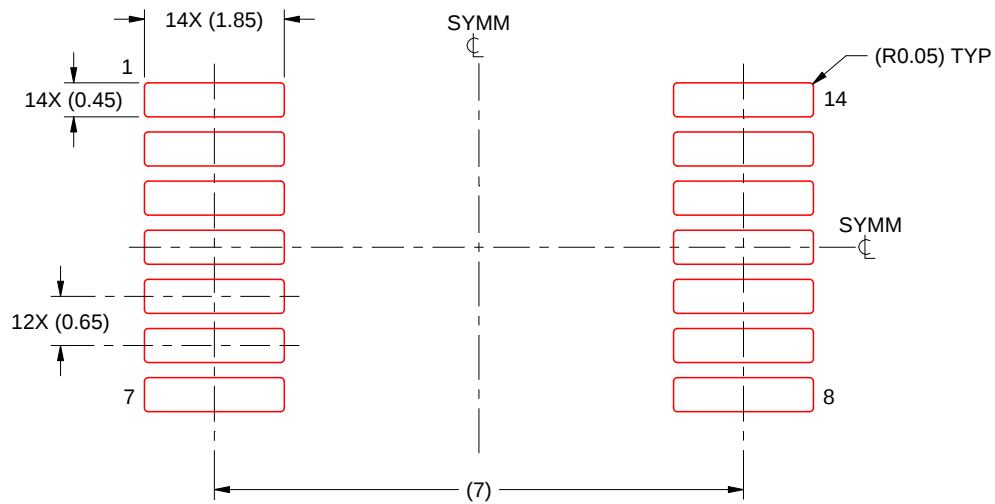
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

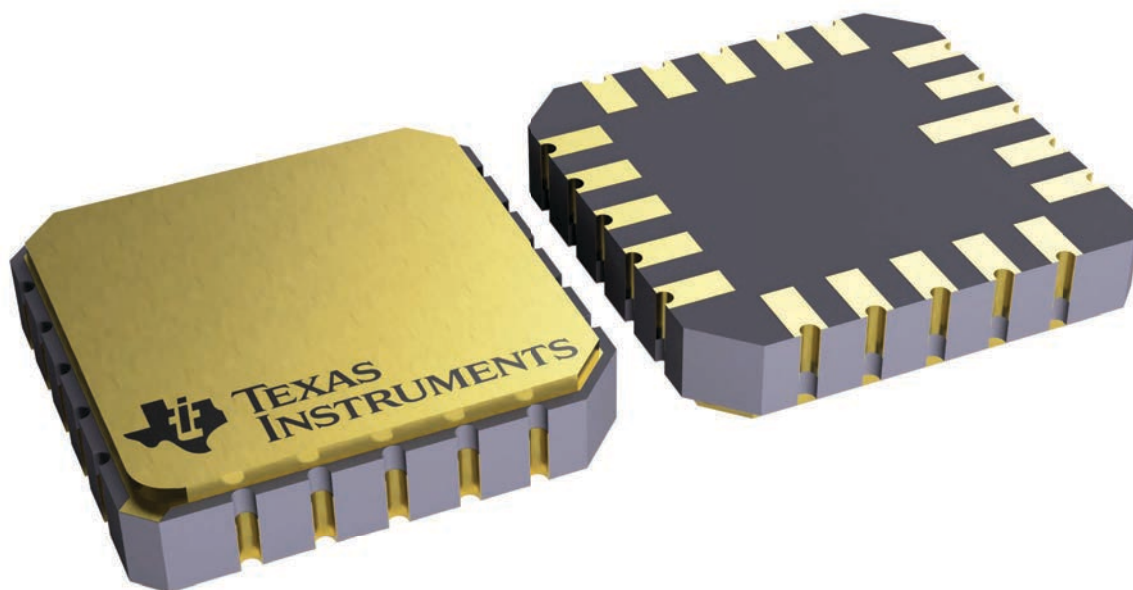
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



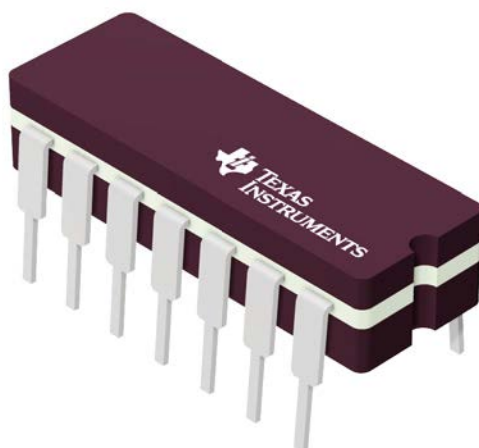
4229370VA\

**J 14**

## GENERIC PACKAGE VIEW

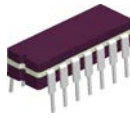
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

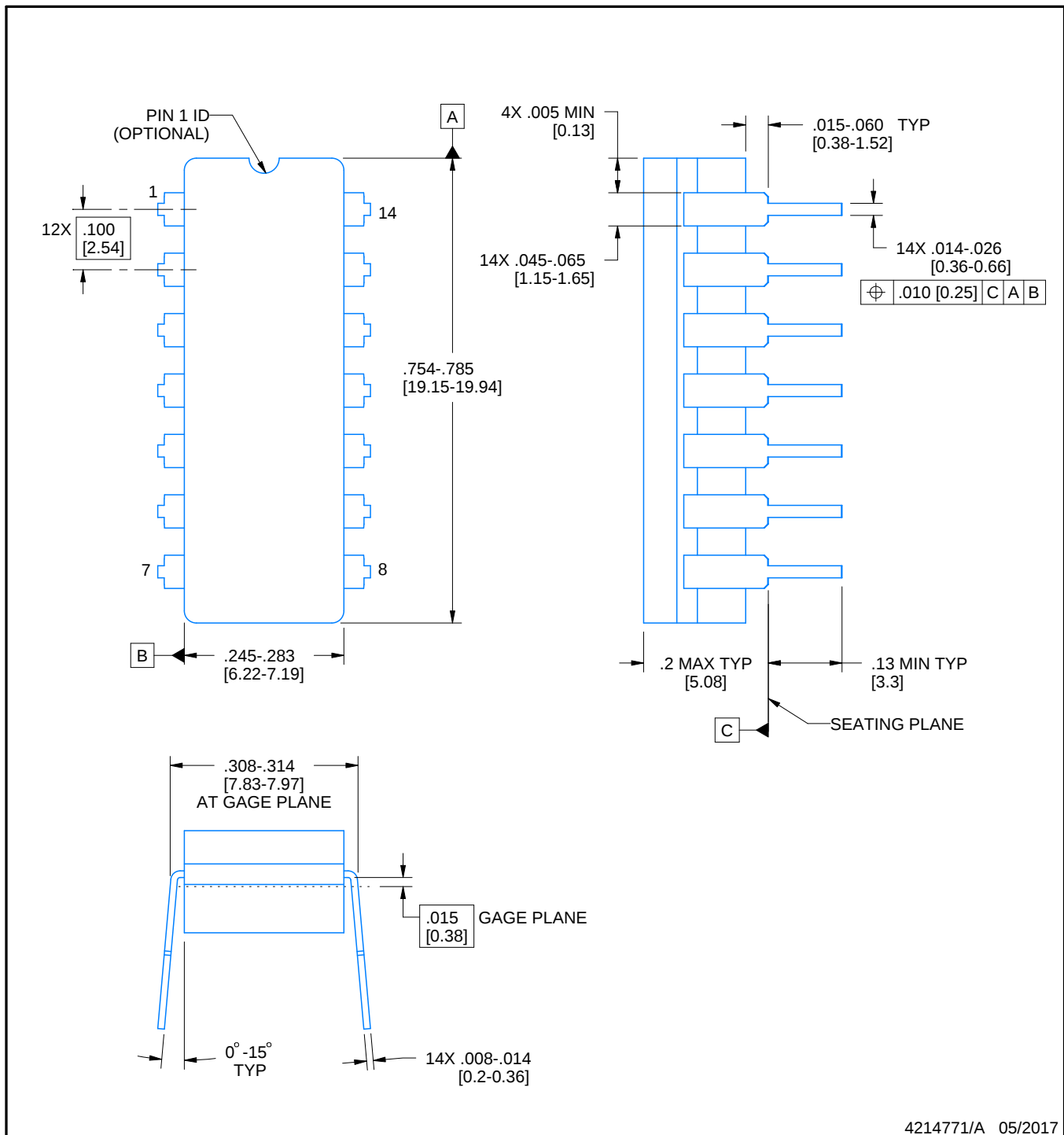


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

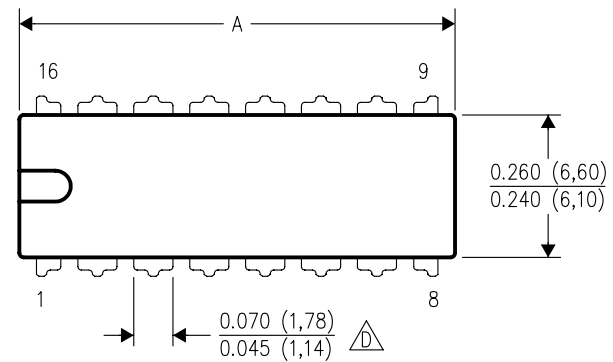
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



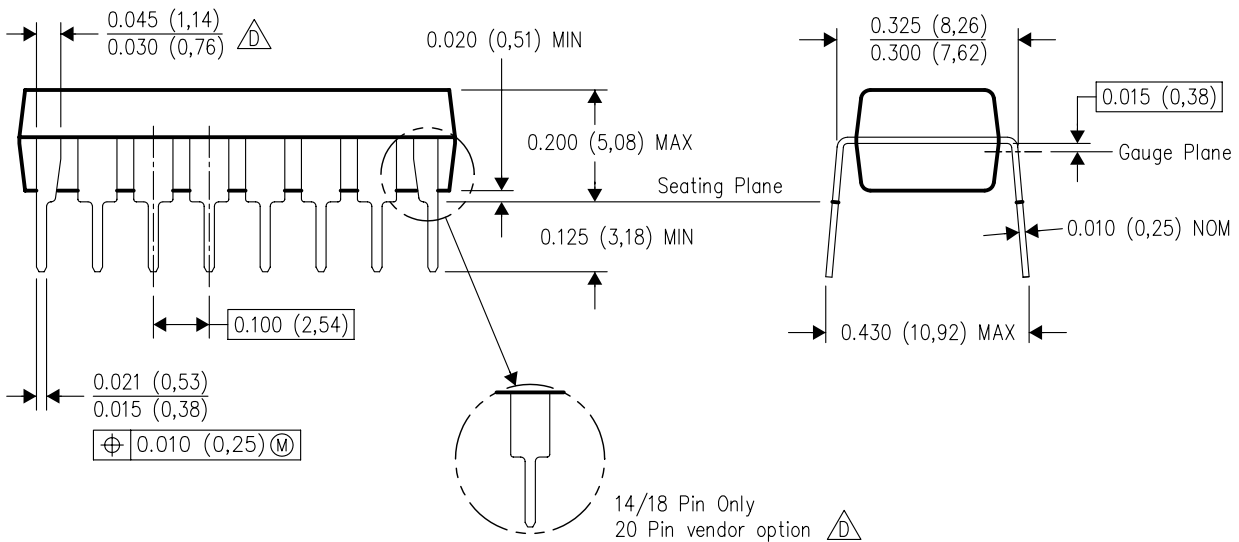
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE

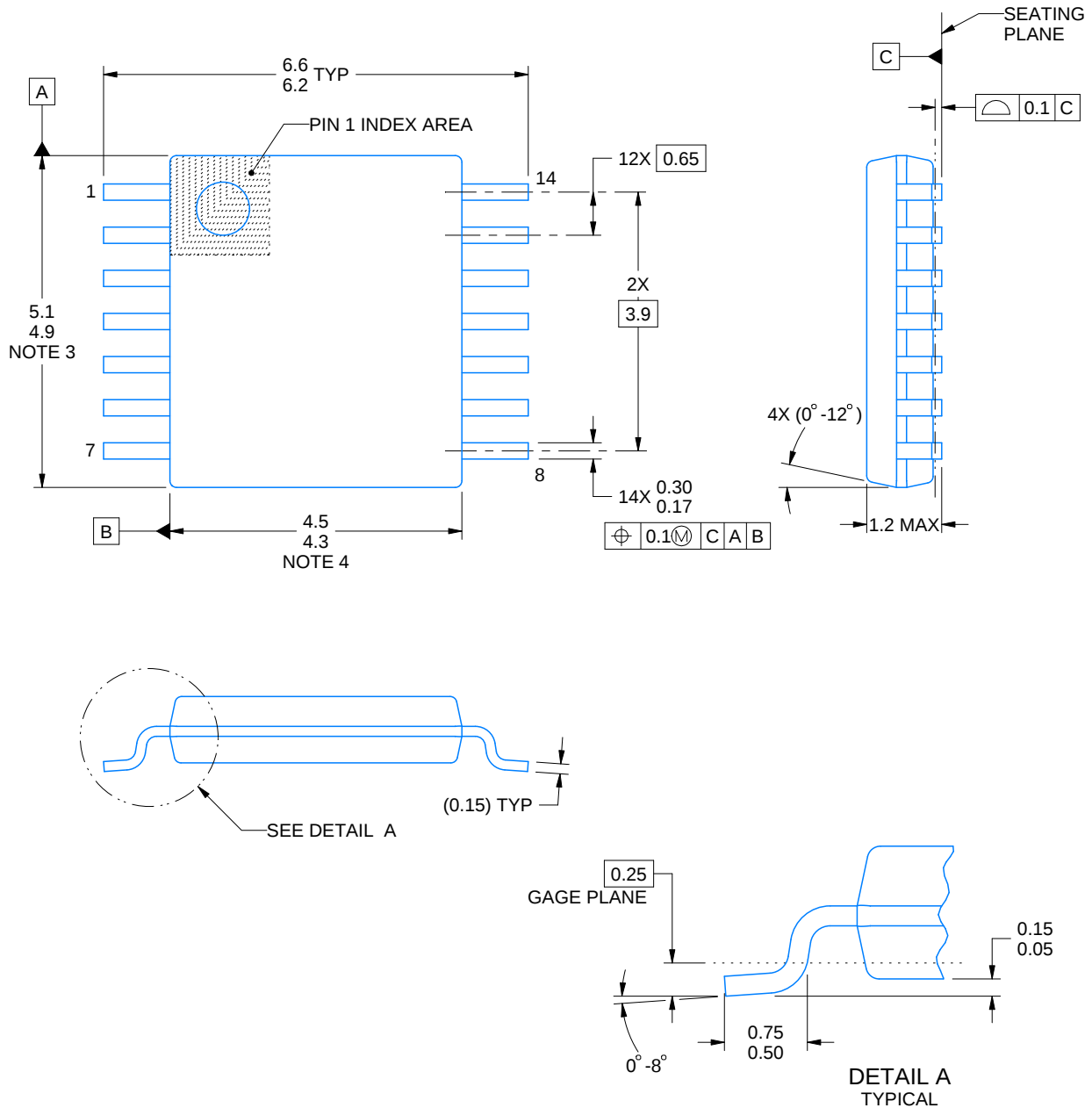
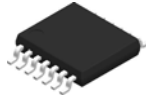


| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

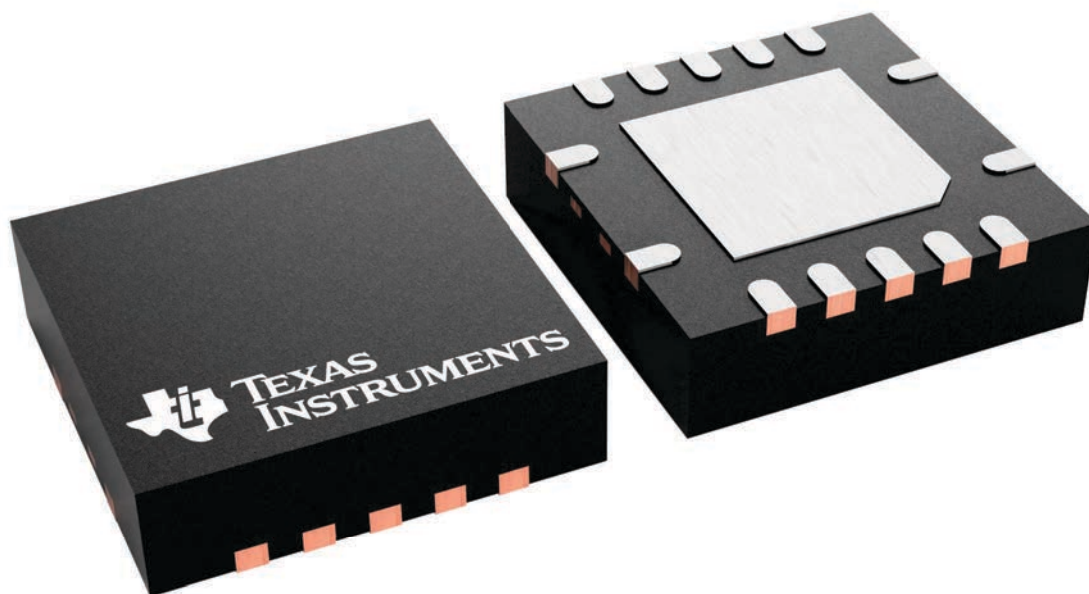
**RGY 14**

**VQFN - 1 mm max height**

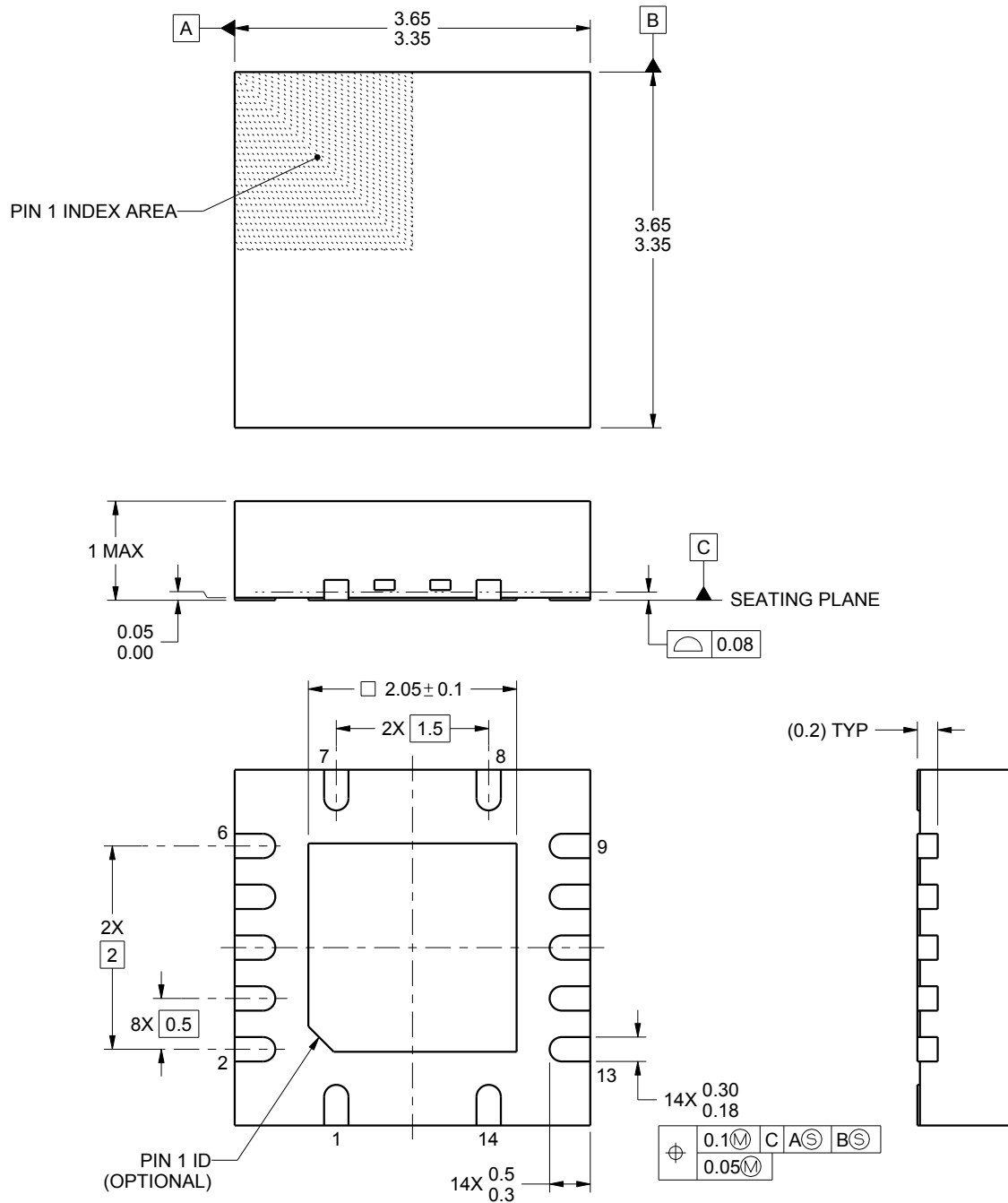
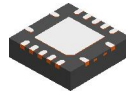
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A



4219040/A 09/2015

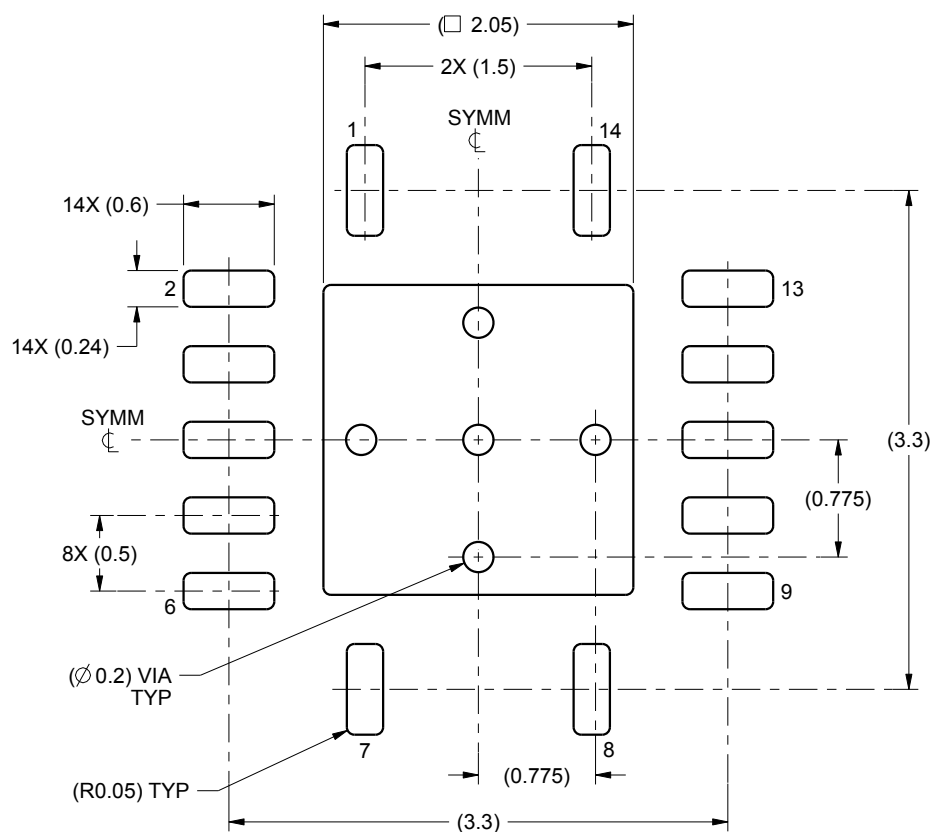
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

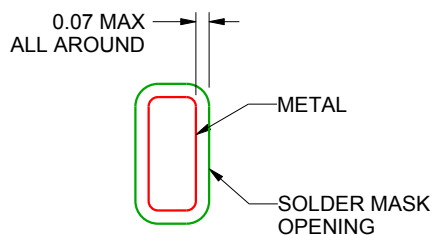
**RGY0014A**

## VQFN - 1 mm max height

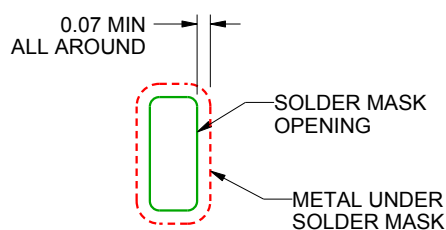
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



NON SOLDER MASK  
DEFINED  
(PREFERRED)



SOLDER MASK  
DEFINED

## SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

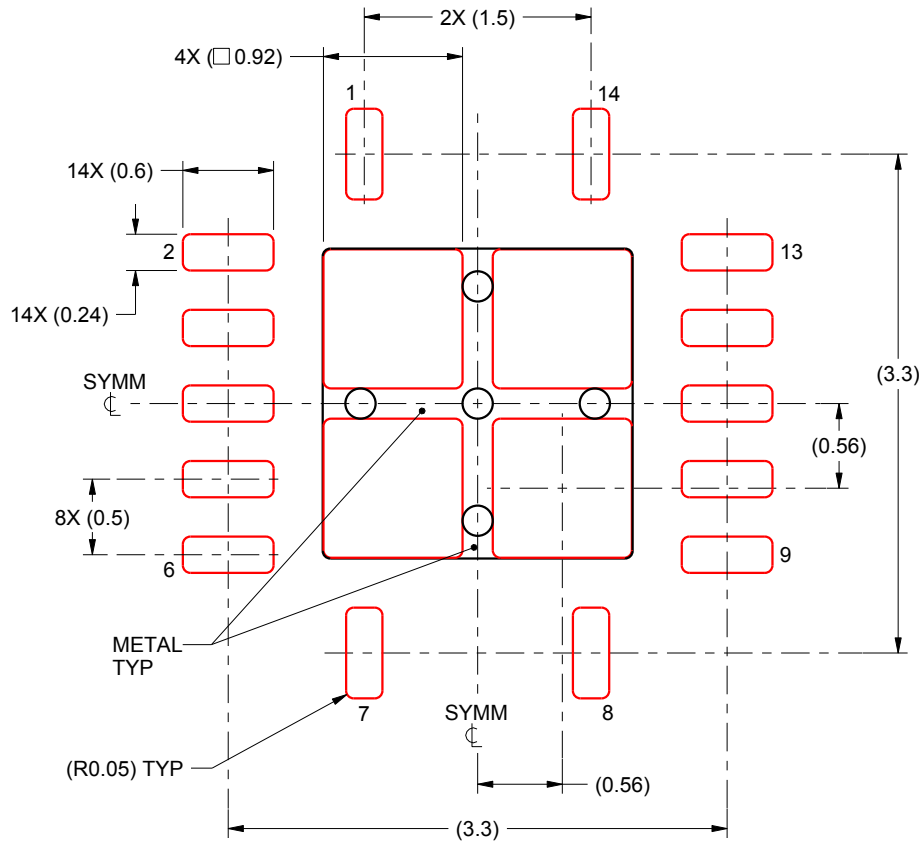
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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