LCD Segment Drivers

Multi-function LCD Segment Drivers

BU97550KV-M **MAX 528 Segment(66SEG x 8COM)**

General Description

The BU97550KV-M is 1/8, 1/7, 1/5, 1/4, 1/3, or Static general-purpose LCD driver.
The BU97550KV-M can drive up to 528 LCD Segments directly. The BU97550KV-M can also control up to 9 General-Purpose/PWM output ports.
These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 528 Segments
- Display Duty Static, 1/3, 1/4, 1/5, 1/7, 1/8 Selectable
- Bias: 1/2, 1/3, 1/4 Selectable
- Interface: 3wire Serial Interface

Features

- AEC-Q100 Qualified (Note)
- Key Input Function for Up to 30 Keys (A key scan is performed only when a key is pressed.)
- Either 1/8, 1/7, 1/5, 1/4, 1/3 or Static
  Can be Selected with The Serial Control Data.
  1/8 duty drive: Up to 528 Segments can be driven
  1/7 duty drive: Up to 469 Segments can be driven
  1/5 duty drive: Up to 345 Segments can be driven
  1/4 duty drive: Up to 280 Segments can be driven
  1/3 duty drive: Up to 210 Segments can be driven
  Static drive: Up to 70 Segments can be driven
- Serial Data Control of Frame Frequency for Common and Segment output Waveforms.
- Serial Data Control of Switching Between The Segment output Port, PWM output Port and General-Purpose output Port Functions.(Max 9 ports)
- Built-in Oscillation circuit
- Integrated Voltage Detected Type Power on Reset(VDET) circuit
- No External Component
- Low Power Consumption Design
- Supports Line and Frame Inversion

(Note) Grade 3

Applications

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

Package

W (Typ) x D (Typ) x H (Max)



VQFP80
14.00mm x 14.00mm x 1.60mm

Typical Application Circuit

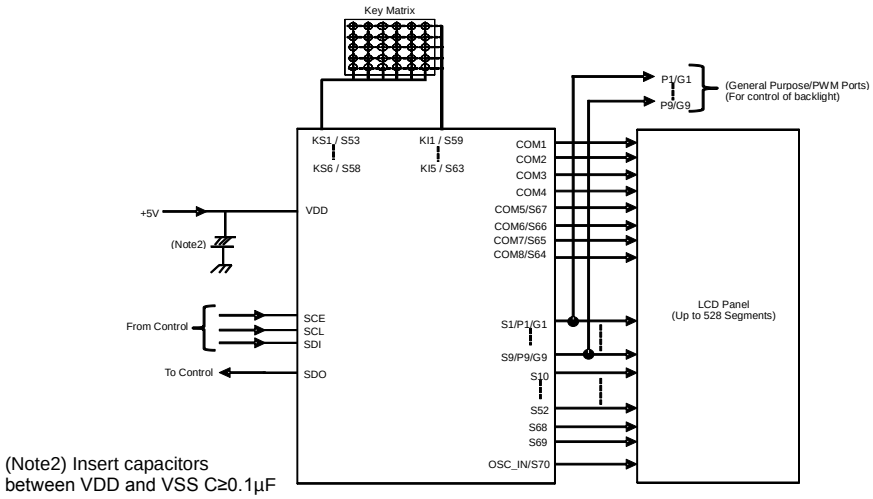


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

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Block Diagram

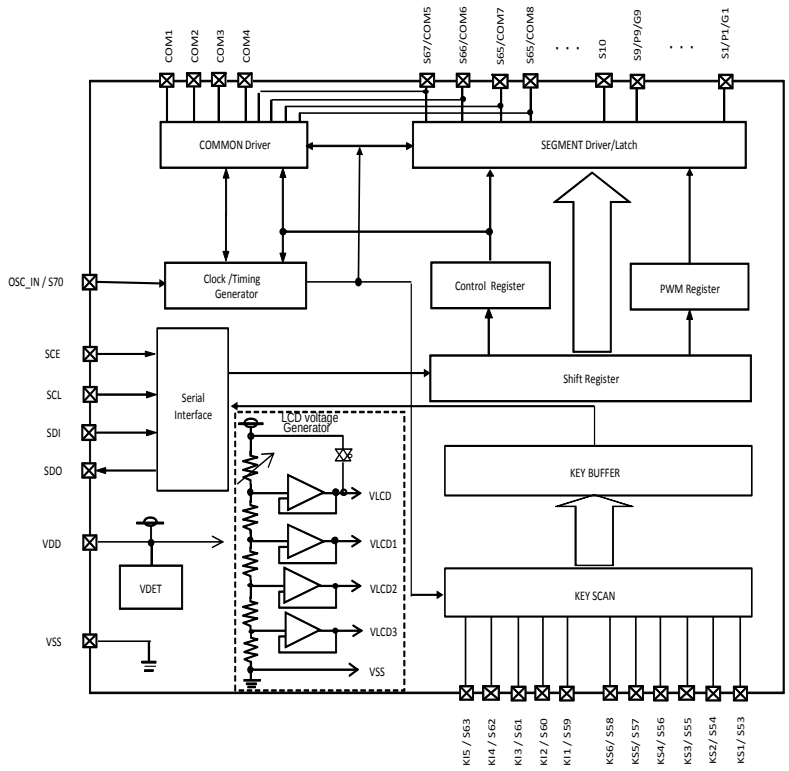


Figure 2. Block Diagram

Pin Arrangement

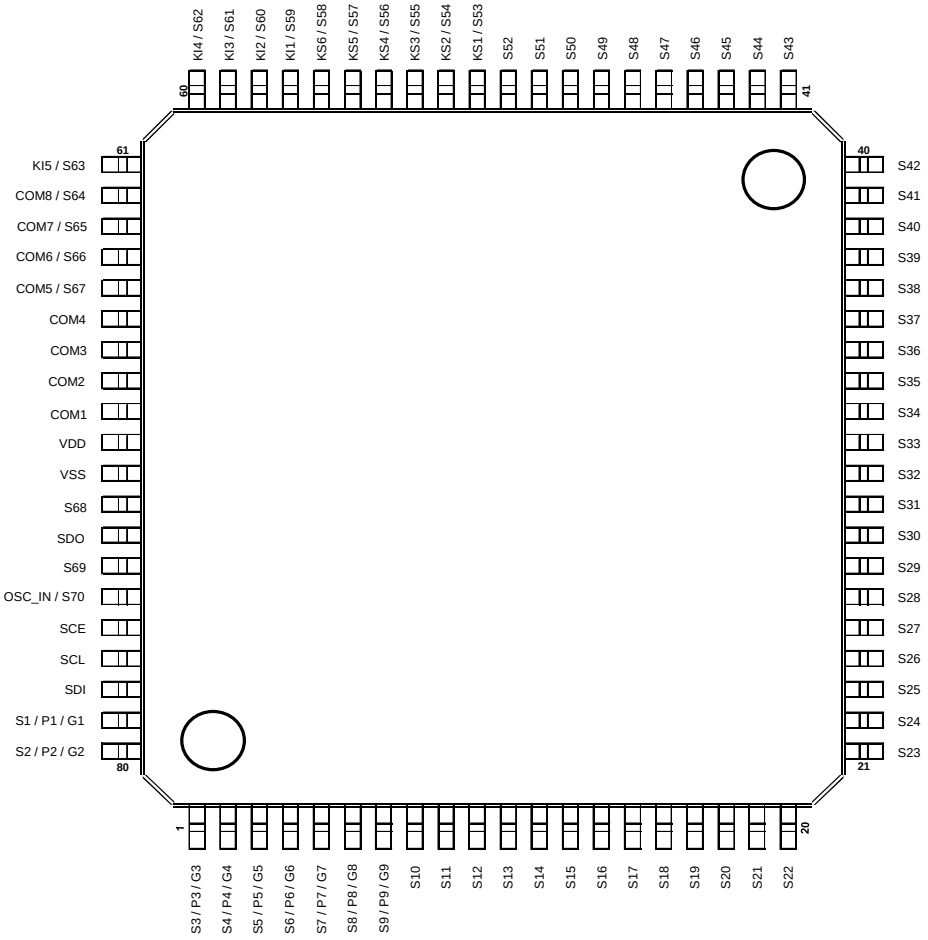


Figure 3. Pin Configuration (TOP VIEW)

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Absolute Maximum Ratings (VSS = 0V)

Parameter	Symbol	Pin	Rating	Unit
Maximum Supply Voltage	VDD	VDD	-0.3 to +7.0	V
Input Voltage	V_{IN1}	SCE, SCL, SDI	-0.3 to +7.0	V
	V_{IN2}	KI1 to KI5	-0.3 to +7.0	V
Allowable Loss	Pd		1.2 (Note3)	W
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

(Note3) When use more than Ta=25°C, subtract 12mW per degree. (Using ROHM standard board)
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommend Operating Conditions (Ta = -40°C to +85°C, VSS = 0V)

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	V_{H1}	SCE, SCL, SDI		-	0.03 VDD	-	V
	V_{H2}	KI1 to KI5		-	0.1 VDD	-	
Power-on Detection Voltage	V_{DET}	VDD		1.3	1.8	2.2	V
"H" Level Input Voltage	V_{IH1}	SCE, SCL, SDI	4.5V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	V_{IH2}	SCE, SCL, SDI	2.7V ≤ VDD < 4.5V	0.8VDD	-	VDD	
	V_{IH3}	KI1 to KI5		0.7VDD	-	VDD	
"L" Level Input Voltage	V_{IL1}	SCE, SCL, SDI KI1 to KI5		0	-	0.2VDD	V
Input Floating Voltage	V_{IF}	KI1 to KI5		-	-	0.05VDD	V
Pull-down Resistance	R_{PD}	KI1 to KI5	VDD=5.0V	50	100	250	kΩ
Output Off Leakage Current	I_{OFFH}	SDO	V_O=6.0V	-	-	6.0	µA
"H" Level Input Current	I_{IH1}	SCE, SCL, SDI	V_I = 5.5V	-	-	5.0	µA
"L" Level Input Current	I_{IL1}	SCE, SCL, SDI	V_I = 0V	-5.0	-	-	µA
"H" Level Output Voltage	V_{OH1}	S1 to S70	I_O = -20µA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	V_{OH2}	COM1 to COM8	I_O = -100µA, VDD=1.00*VDD	VDD-0.9	-	-	
	V_{OH3}	P1/G1 to P9/G9	I_O = -1mA	VDD-0.9	-	-	
	V_{OH4}	KS1 to KS6	I_O = -500µA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	V_{OL1}	S1 to S70	I_O = 20µA	-	-	0.9	V
	V_{OL2}	COM1 to COM8	I_O = 100µA	-	-	0.9	
	V_{OL3}	P1/G1 to P9/G9	I_O = 1mA	-	-	0.9	
	V_{OL4}	KS1 to KS6	I_O = 25µA	0.2	0.5	1.5	
	V_{OL5}	SDO	I_O = 1mA	-	0.1	0.5	
Middle Level Output Voltage	V_{MID1}	S1 to S70	1/2 bias I_O = ±20µA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	V
	V_{MID2}	COM1 to COM8	1/2 bias I_O = ±100µA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	
	V_{MID3}	S1 to S70	1/3 bias I_O = ±20µA VLCD=1.00*VDD	2/3 VDD -0.9	-	2/3 VDD +0.9	
	V_{MID4}	S1 to S70	1/3 bias I_O = ±20µA VLCD=1.00*VDD	1/3 VDD -0.9	-	1/3 VDD +0.9	
	V_{MID5}	COM1 to COM8	1/3 bias I_O = ±100µA VLCD=1.00*VDD	2/3 VDD -0.9	-	2/3 VDD +0.9	
	V_{MID6}	COM1 to COM8	1/3 bias I_O = ±100µA VLCD=1.00*VDD	1/3 VDD -0.9	-	1/3 VDD +0.9	
	V_{MID7}	S1 to S70	1/4 bias I_O = ±20µA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	
	V_{MID8}	COM1 to COM8	1/4 bias I_O = ±100µA VLCD=1.00*VDD	3/4 VDD -0.9	-	3/4 VDD +0.9	
	V_{MID9}	COM1 to COM8	1/4 bias I_O = ±100µA VLCD=1.00*VDD	1/4 VDD -0.9	-	1/4 VDD +0.9	

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Electrical Characteristics – continued

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Current Consumption	I_{DD1}	VDD	Power-saving mode	-	-	15	µA
	I_{DD2}	VDD	VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	105	220	
	I_{DD3}	VDD	VDD = 5.0V Output open,1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	130	270	
	I_{DD4}	VDD	VDD = 5.0V Output open,1/4 bias Frame frequency=80Hz VLCD=1.00*VDD	-	160	330	

Oscillation Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
scillator Frequency 1	f_{OSC1}	-	VDD = 2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	f_{OSC2}	-	VDD = 5.0V	540	600	660	kHz
Oscillator Frequency 3	f_{OSC3}	-	VDD = 6.0V	562	625	688	kHz
External Clock Frequency(Note4)	f_{OSC4}	OSC_IN/S70	External clock mode (OC=1)	30	-	1000	kHz
External Clock Rise Time	tr			-	160	-	ns
External Clock Fall Time	tf			-	160	-	ns
External Clock Duty	t_{DTY}			30	50	70	%

(Note4) Frame frequency is decided external frequency and dividing ratio of FC0 to FC3 setting.

[Reference Data]

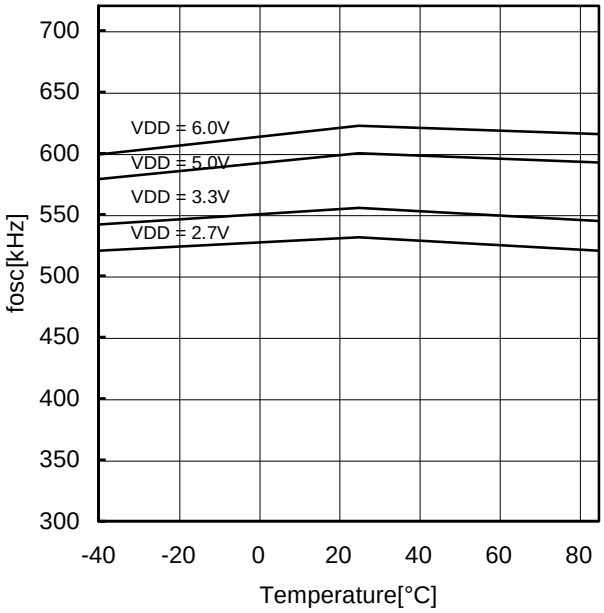


Figure 4. Frame Frequency Typical Temperature Characteristics

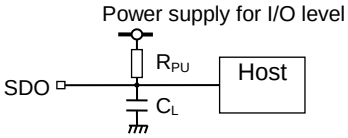
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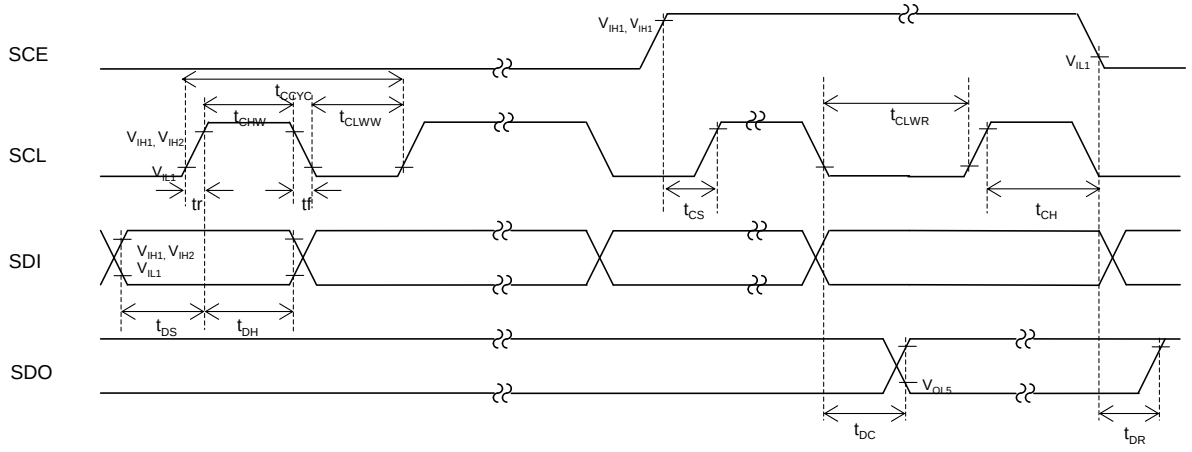
MPU Interface Characteristics (Ta=-40 to +85°C, VDD = 2.7V to 6.0V, VSS=0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	t_{DS}	SCL, SDI		120	-	-	ns
Data Hold Time	t_{DH}	SCL, SDI		120	-	-	ns
SCE Wait Time	t_{CP}	SCE, SCL		120	-	-	ns
SCE Setup Time	t_{CS}	SCE, SCL		120	-	-	ns
SCE Hold Time	t_{CH}	SCE, SCL		120	-	-	ns
Clock Cycle Time	t_{CCYC}	SCL		320	-	-	ns
High-level Clock Pulse Width	t_{CHW}	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	t_{CLWW}	SCL		120	-	-	ns
Low-level Clock Pulse Width (Read)	t_{CLWR}	SCL	R_{PU}=4.7kΩ C_L=10pF(Note5)	1.6	-	-	µs
Rise Time	tr	SCE, SCL, SDI		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI		-	160	-	ns
SDO Output Delay Time	t_{DC}	SDO	R_{PU}=4.7kΩ C_L=10pF(Note5)	-	-	1.5	µs
SDO Rise Time	t_{DR}	SDO	R_{PU}=4.7kΩ C_L=10pF(Note5)	-	-	1.5	µs

(Note5) Since SDO is an open-drain output, "t_{DC}" and "t_{DR}" depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.
R_{PU}: 1kΩ≤RPU≤10kΩ is recommended.
C_L: A parasitic capacitance in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

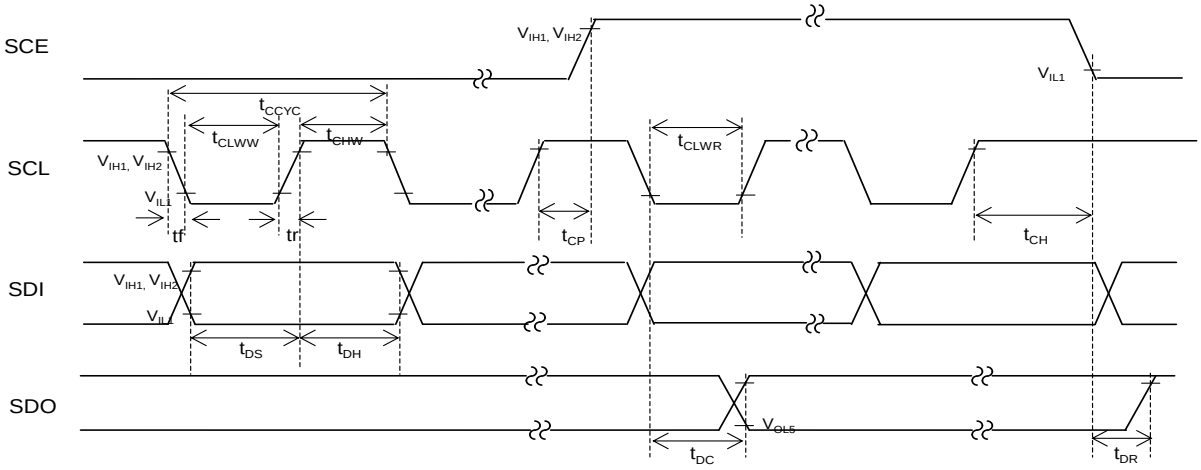


Figure 5. Serial Interface Timing

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Pin Description

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S9/P9/G9	79,80, 1 to 7	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S9/P9/G9 pins can also be used as General-Purpose or PWM output when so set up by the control data.	-	O	OPEN
S10 to S52 S68, S69	8 to 50 72, 74	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S53 to KS6/S58	51 to 56	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S53 to KS6/S58 pins can be used as Segment outputs when so specified by the control data.	-	O	OPEN
KI1/S59 to KI5/S63	57 to 61	Key scan inputs These pins have built-in pull-down resistors. The KI1/S59 to KI5/S63 pins can be used as Segment outputs when so specified by the control data.	-	I/O	OPEN
COM1 to COM4	66 to 69	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
COM5/S67 COM6/S66 COM7/S65 COM8/S64	65 64 63 62	Common / Segment output for LCD driving Assigned as Common output in 1/8, 1/7 and 1/5 Duty modes and Segment output in Static, 1/3 and 1/4 Duty modes.	-	O	OPEN
OSC_IN/S70	75	Segment output for displaying the display data transferred by serial data input. The OSC_IN/S70 pin can be used as external frequency input pin when set up by the control data.	-	I/O	OPEN
		Serial data transfer inputs. Must be connected to the controller.			
SCE	76	SCE: Chip enable	H	I	-
SCL	77	SCL: Synchronization clock	↑	I	-
SDI	78	SDI: Transfer data	-	I	-
SDO	73	Output data	-	O	OPEN
VDD	70	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	71	Power supply pin. Must be connected to ground.	-	-	-

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IO Equivalent Circuit

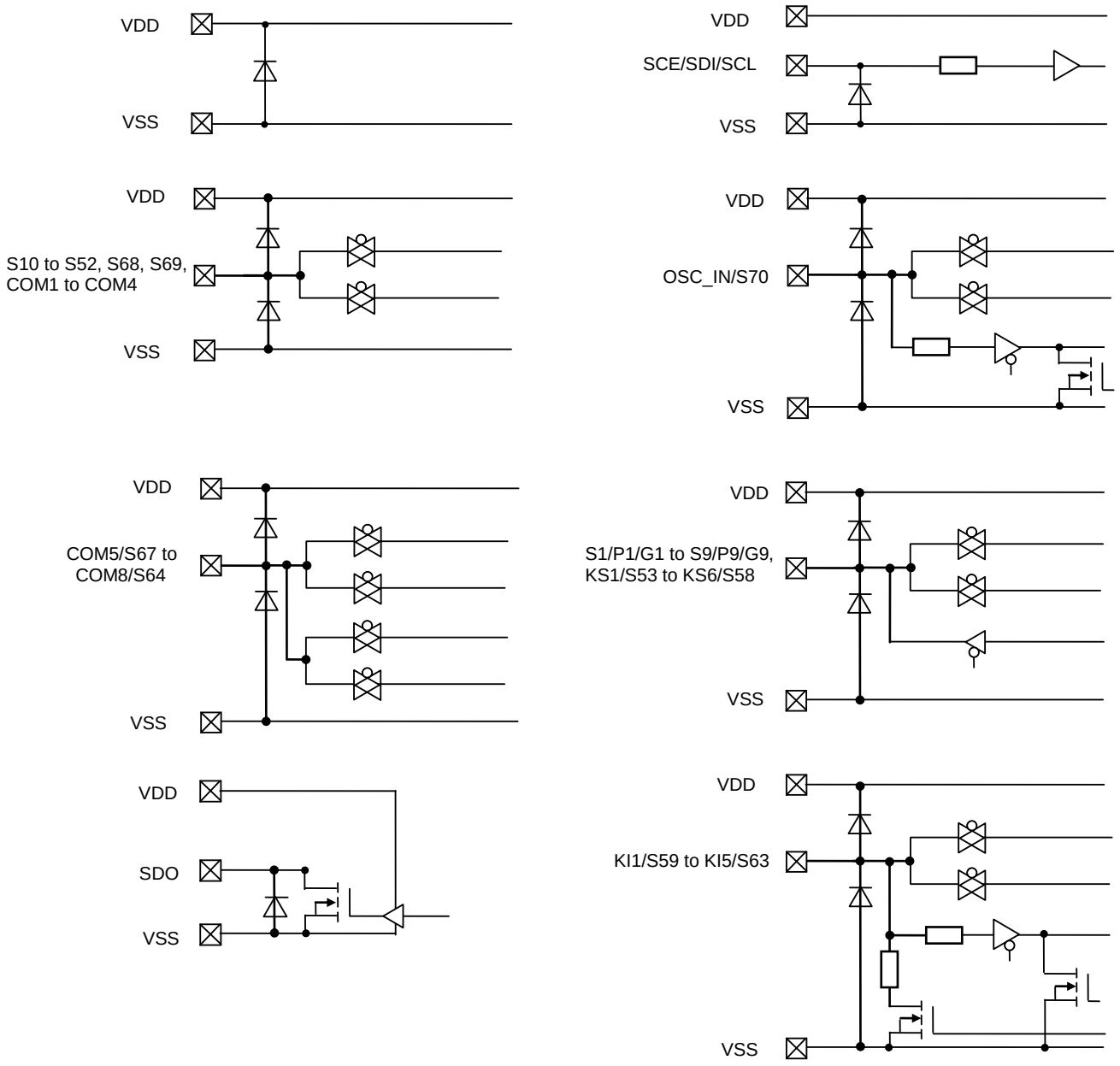


Figure 6. I/O Equivalent Circuit

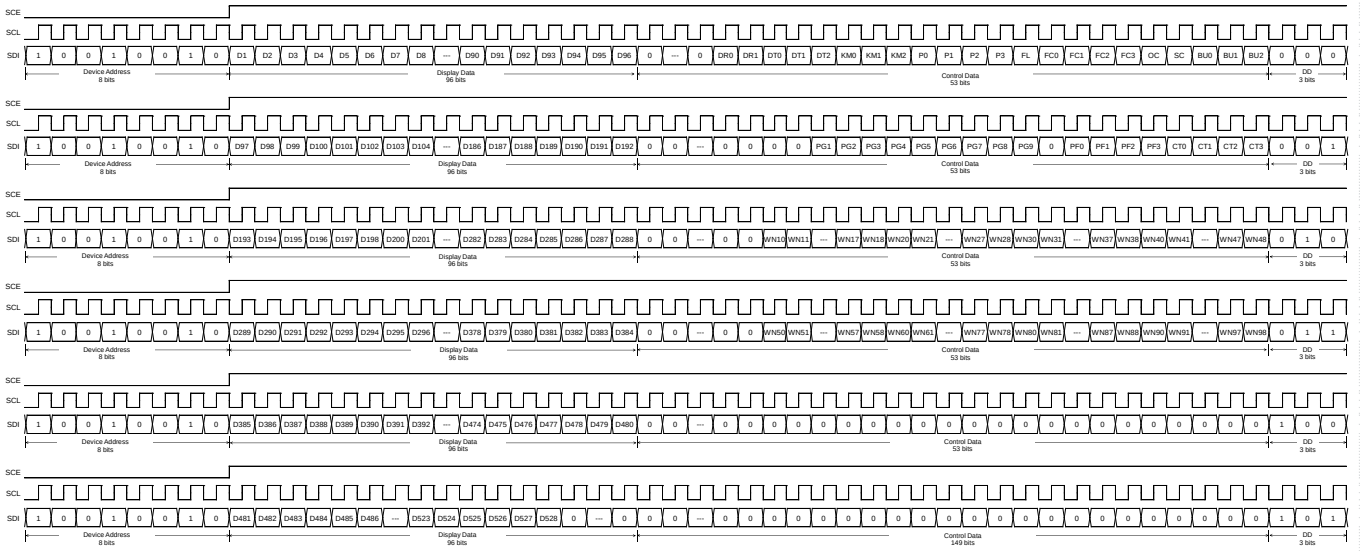
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Serial Data Transfer Formats

1. 1/8 Duty

(1) When SCL is stopped at the low level



(Note6)

Figure 7. 3-SPI Data Transfer Format

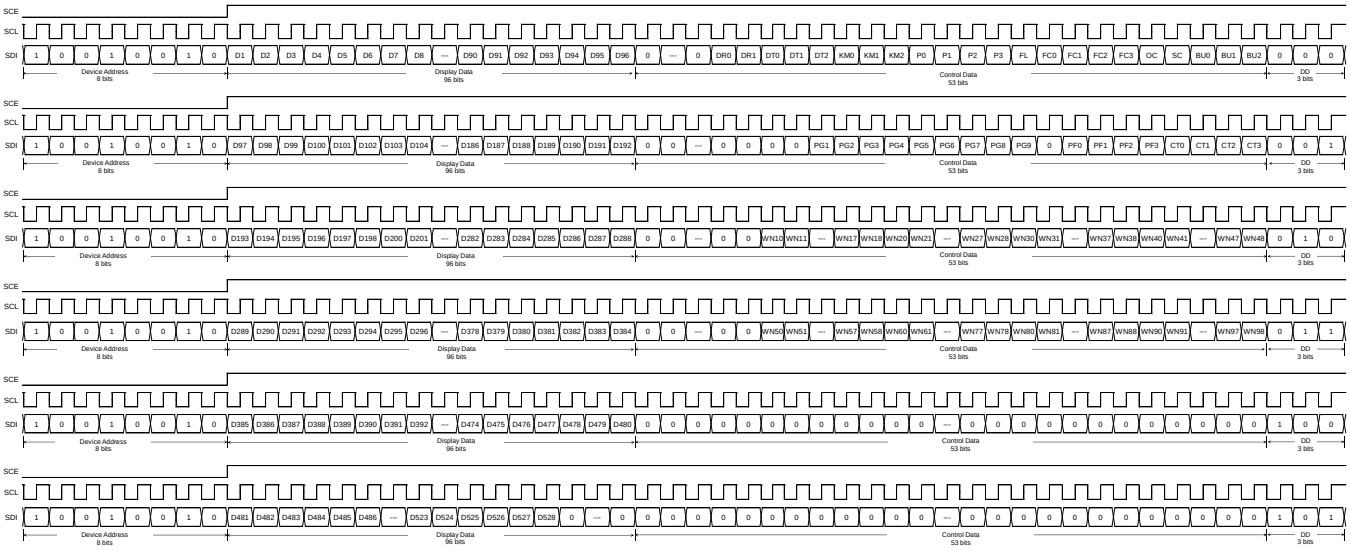
(Note6) DD is direction data.

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note7)

Figure 8. 3-SPI Data Transfer Format

(Note7) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D528……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38,W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

When it is coincident with device code, BU97550KV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 160bit (Device code: 8bit, Display data and Control data: 149bit, DD: 3bit).

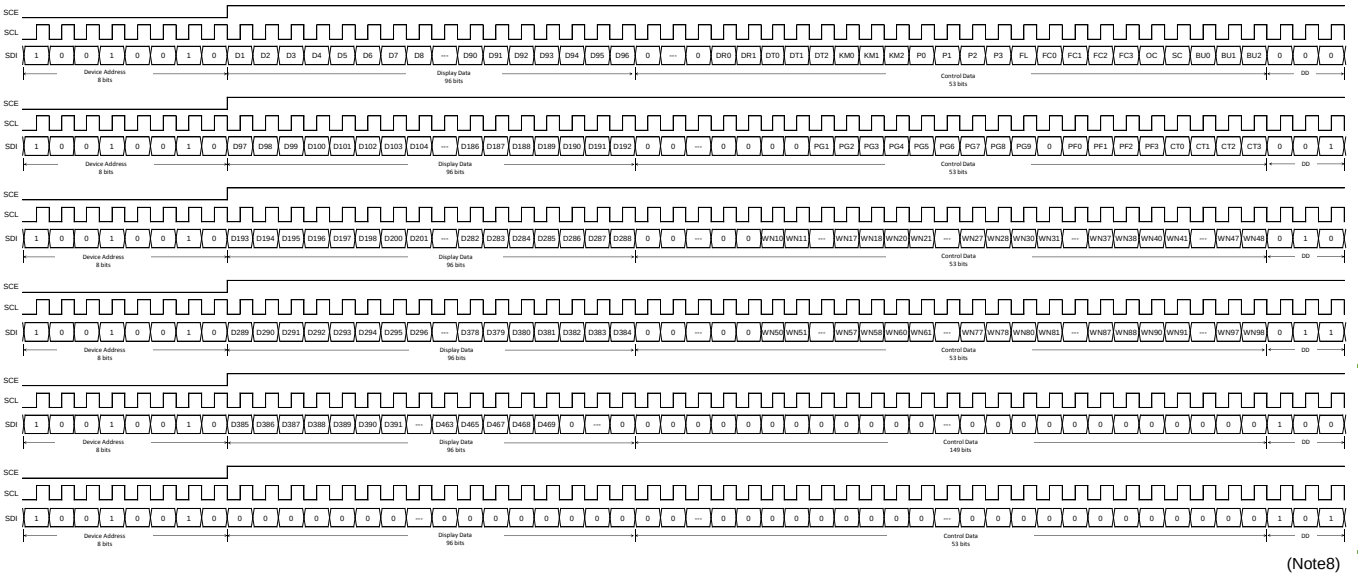
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Serial Data Transfer Formats – continued

2. 1/7 Duty

(1) When SCL is stopped at the low level



(Note8)

Figure 9. 3-SPI Data Transfer Format

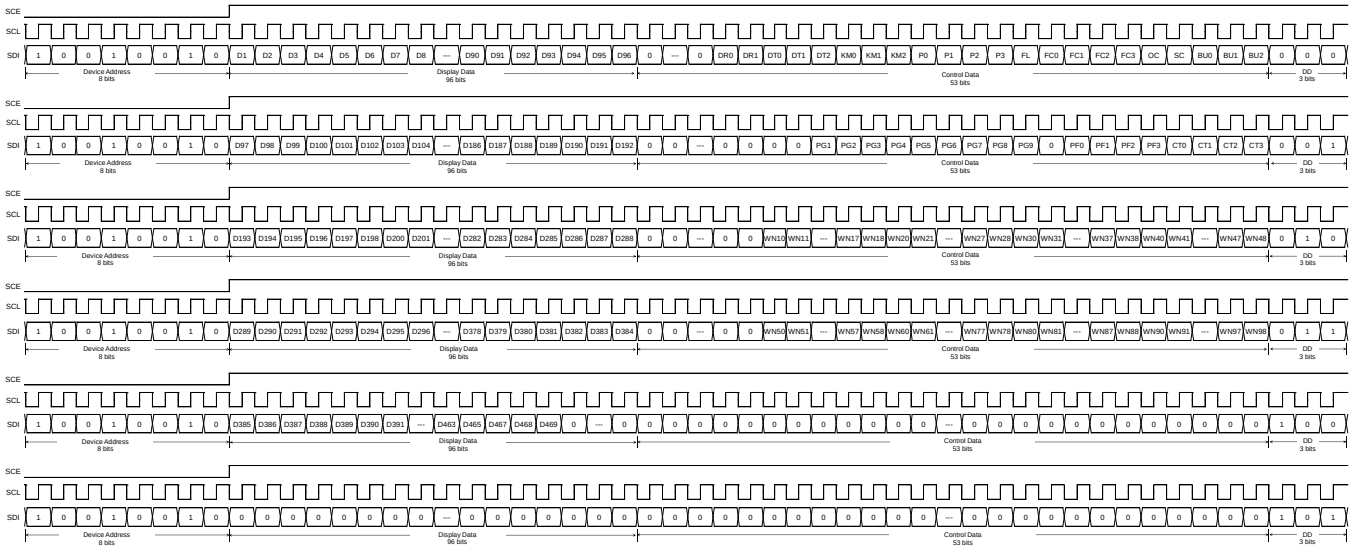
(Note8) DD is direction data.

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note9)

Figure 10. 3-SPI Data Transfer Format

(Note9) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D469……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38,W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

When it is coincident with device code, BU97550KV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 160bit (Device code: 8bit, Display data and Control data: 149bit, DD: 3bit).

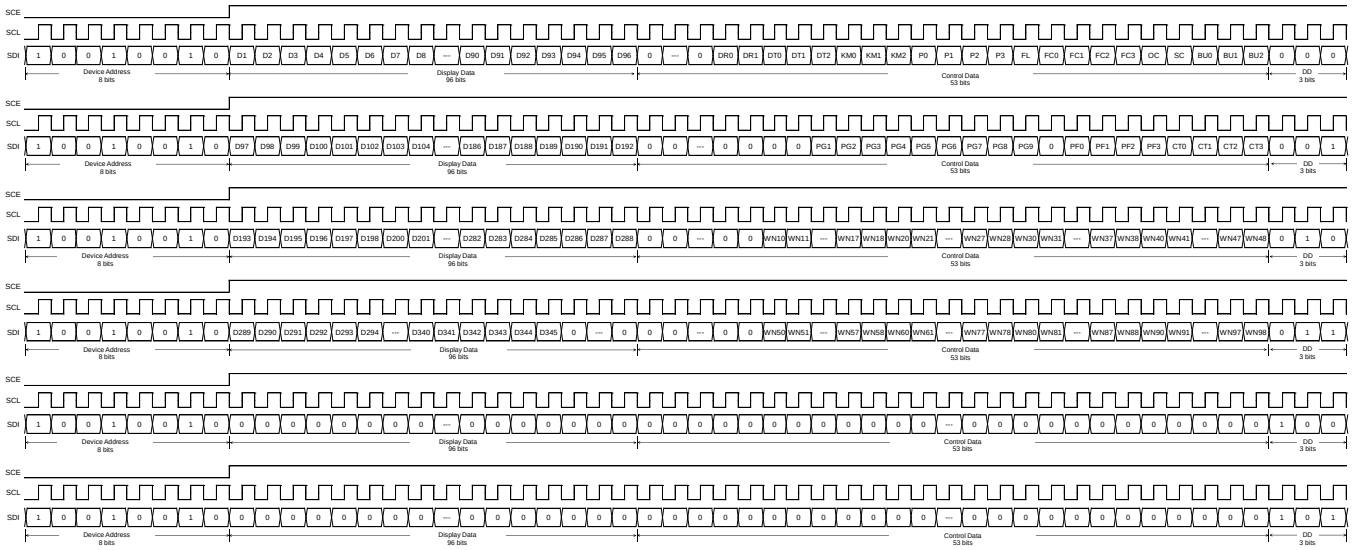
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Serial Data Transfer Formats – continued

3. 1/5 Duty

(1) When SCL is stopped at the low level



(Note10)

Figure 11. 3-SPI Data Transfer Format

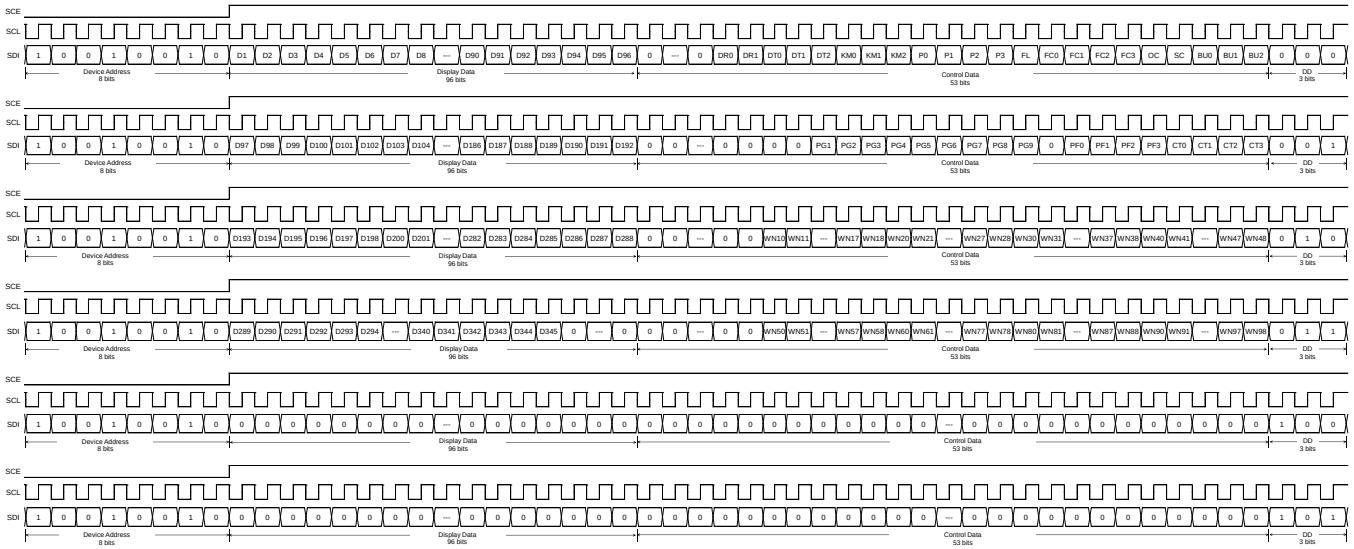
(Note10) DD is direction data.

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note11)

Figure 12. 3-SPI Data Transfer Format

(Note11) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D345……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

When it is coincident with device code, BU97550KV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 160bit (Device code: 8bit, Display data and Control data: 149bit, DD: 3bit).

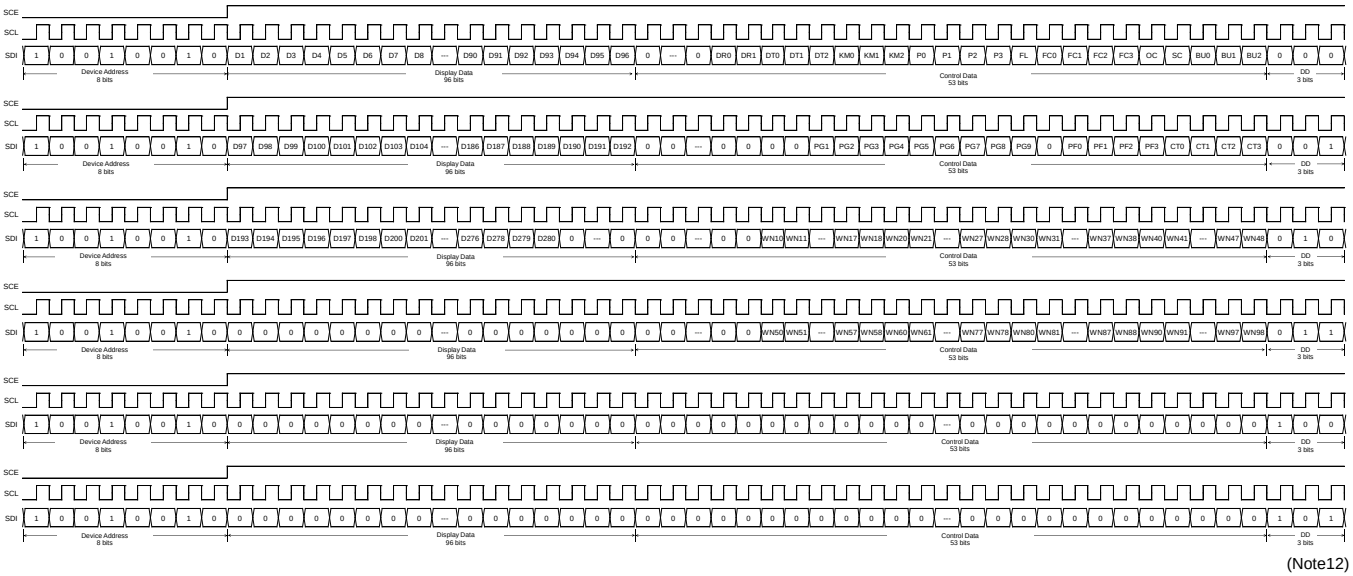
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Serial Data Transfer Formats – continued

4. 1/4 Duty

(1) When SCL is stopped at the low level



(Note12)

Figure 13. 3-SPI Data Transfer Format

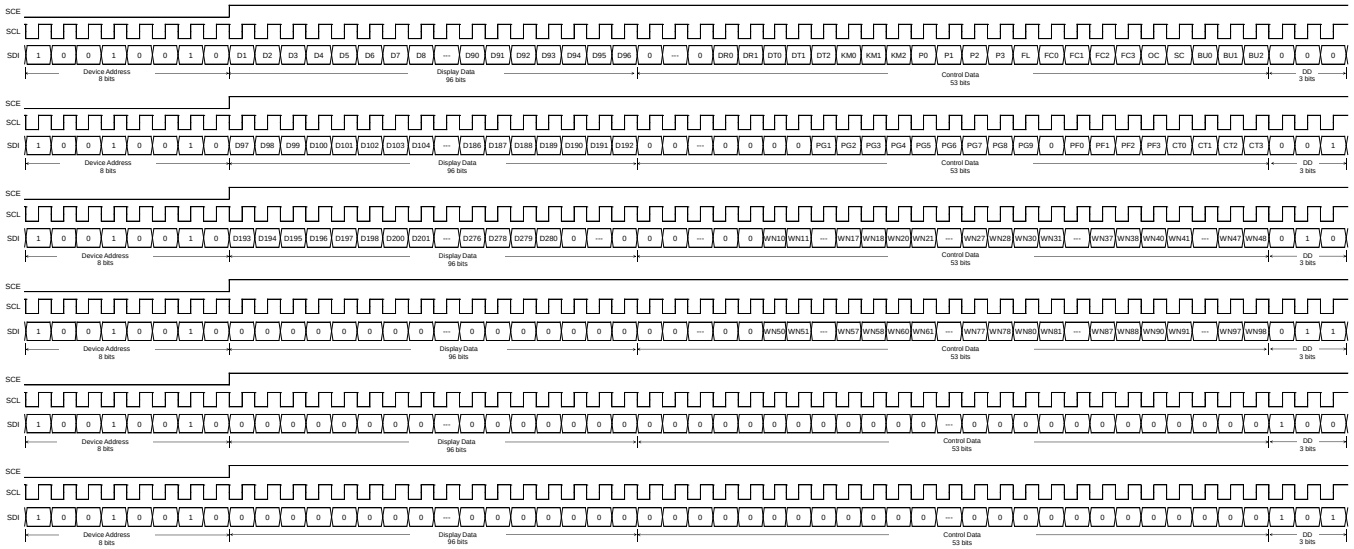
(Note12) DD is direction data.

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note13)

Figure 14. 3-SPI Data Transfer Format

(Note13) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D280……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

When it is coincident with device code, BU97550KV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 160bit (Device code: 8bit, Display data and Control data: 149bit, DD: 3bit).

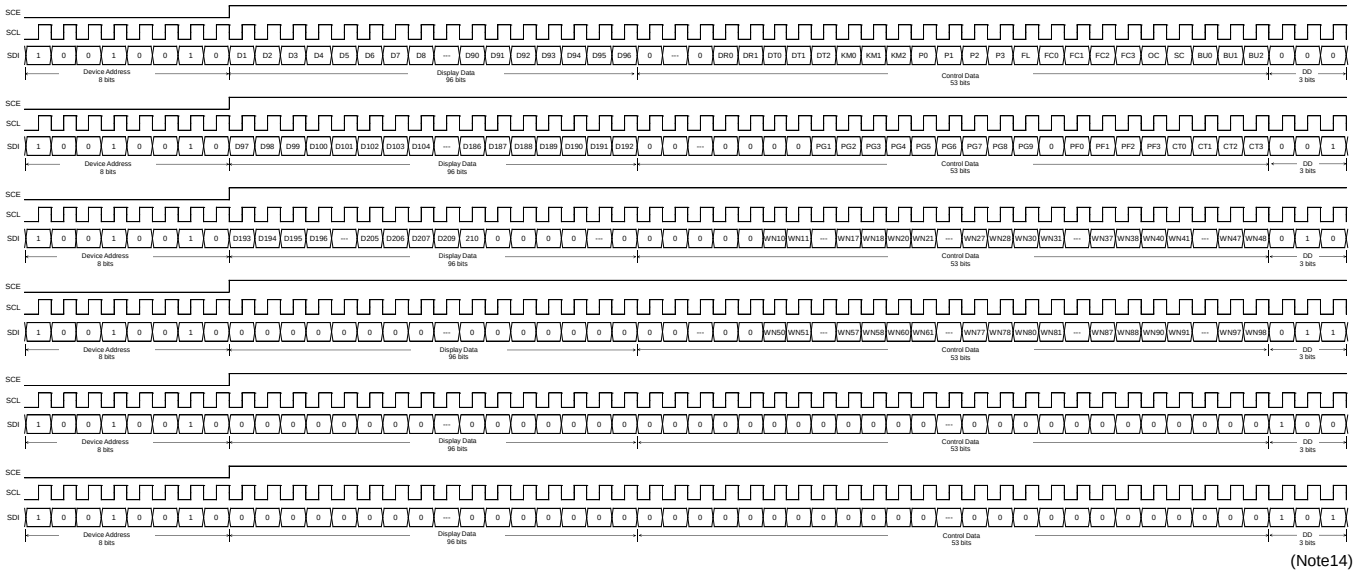
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Serial Data Transfer Formats – continued

5. 1/3 Duty

(1) When SCL is stopped at the low level



(Note14)

Figure 15. 3-SPI Data Transfer Format

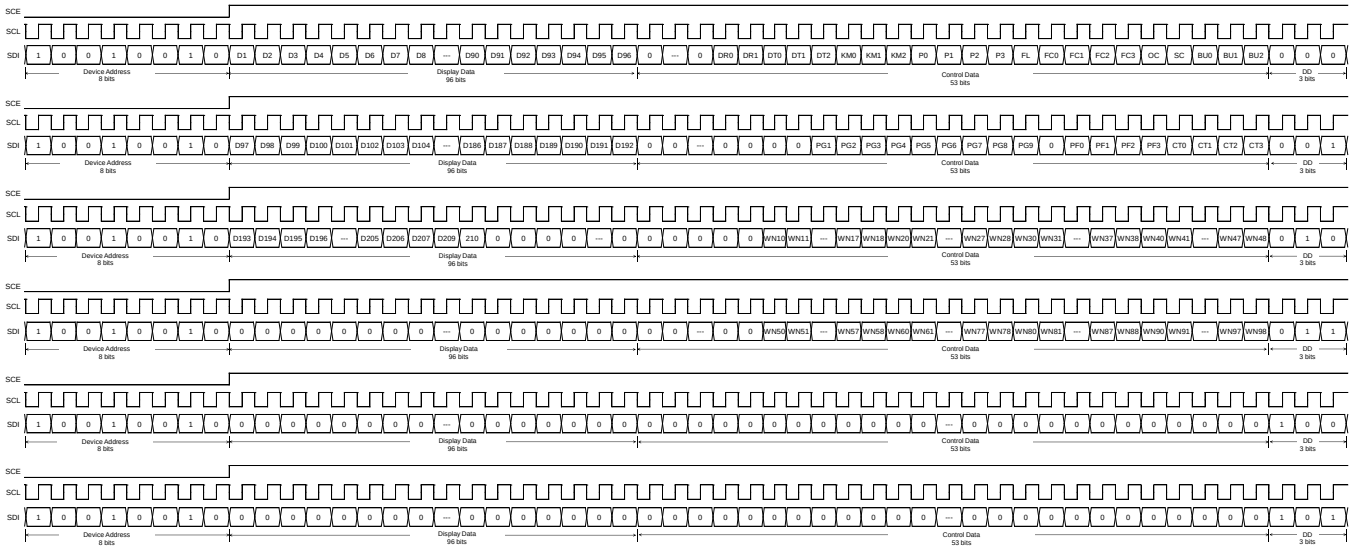
(Note14) DD is direction data.

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note15)

Figure 16. 3-SPI Data Transfer Format

(Note15) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D210……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

When it is coincident with device code, BU97550KV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 160bit (Device code: 8bit, Display data and Control data: 149bit, DD: 3bit).

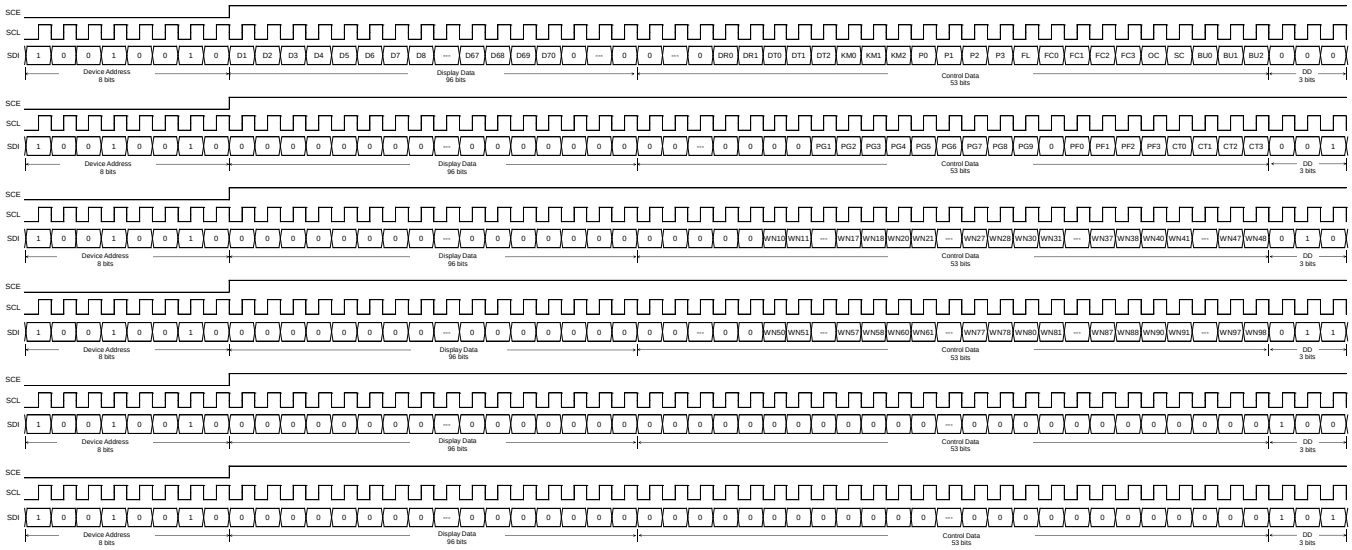
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Serial Data Transfer Formats – continued

6. Static

(1) When SCL is stopped at the low level



(Note16)

Figure 17. 3-SPI Data Transfer Format

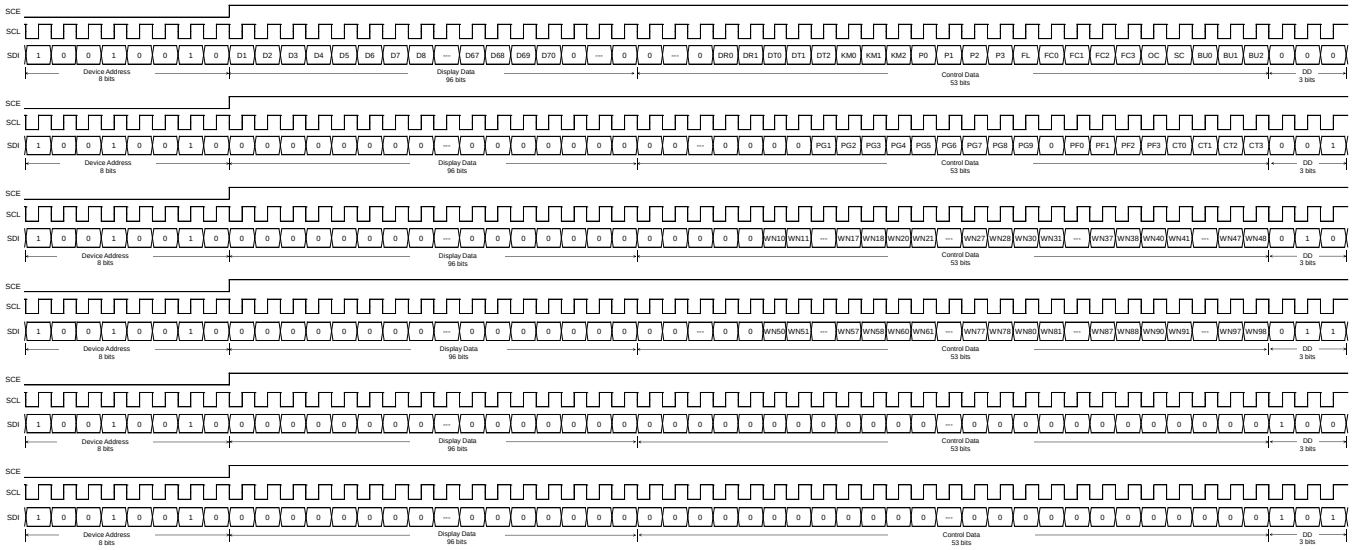
(Note16) DD is direction data.

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note17)

Figure 18. 3-SPI Data Transfer Format

(Note17) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D70 ……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

When it is coincident with device code, BU97550KV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 160bit (Device code: 8bit, Display data and Control data: 149bit, DD: 3bit).

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Control Data Functions

1. KM0, KM1 and KM2: Key Scan output port/Segment output port switching control data

These control data bits switch the functions of the KS1/S53 to KS6/S58 output pins between key scan output and Segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input keys	Reset condition
			KS1/S53	KS2/S54	KS3/S55	KS4/S56	KS5/S57	KS6/S58		
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30	-
0	0	1	S53	KS2	KS3	KS4	KS5	KS6	25	-
0	1	0	S53	S54	KS3	KS4	KS5	KS6	20	-
0	1	1	S53	S54	S55	KS4	KS5	KS6	15	-
1	0	0	S53	S54	S55	S56	KS5	KS6	10	-
1	0	1	S53	S54	S55	S56	S57	KS6	5	-
1	1	0	S53	S54	S55	S56	S57	S58	0	-
1	1	1	S53	S54	S55	S56	S57	S58	0	○

2. P0, P1, P2 and P3: Segment/PWM/General-Purpose output port switching control data

These control bits are used to select the function of the S1/P1/G1 to S9/P9/G9 output Pins (Segment output Pins or PWM output Pins or General-Purpose output Pins).

P0	P1	P2	P3	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	S7/P7/G7	S8/P8/G8	S9/P9/G9	Reset condition
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
0	0	0	1	P1/G1	S2	S3	S4	S5	S6	S7	S8	S9	-
0	0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	S7	S8	S9	-
0	0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	S7	S8	S9	-
0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	S7	S8	S9	-
0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	S7	S8	S9	-
0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S7	S8	S9	-
0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S8	S9	-
1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	S9	-
1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	P9/G9	-
1	0	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	0	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	○

PWM output or General-Purpose output is selected by PGx(x=1 to 9) control data bit.

When the General-Purpose output Port Function is selected, the correspondence between the output Pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data					
	1/8 Duty mode	1/7 Duty mode	1/5 Duty mode	1/4 Duty mode	1/3 Duty mode	Static
S1/P1/G1	D1	D1	D1	D1	D1	D1
S2/P2/G2	D9	D8	D6	D5	D4	D2
S3/P3/G3	D17	D15	D11	D9	D7	D3
S4/P4/G4	D25	D22	D16	D13	D10	D4
S5/P5/G5	D33	D29	D21	D17	D13	D5
S6/P6/G6	D41	D36	D26	D21	D16	D6
S7/P7/G7	D49	D43	D31	D25	D19	D7
S8/P8/G8	D57	D50	D36	D29	D22	D8
S9/P9/G9	D65	D57	D41	D33	D25	D9

When the General-Purpose output Port Function is selected, the respective output pin outputs a “H” level when its corresponding display data is set to “1”. Likewise, it will output a “L” level, if its corresponding display data is set to “0”. For example, at 1/4 Duty mode, S4/P4/G4 is used as a General-Purpose output Port, if its corresponding display data D13 is set to “1”, then S4/P4/G4 will output “H” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “L” level.

3. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode	Reset condition
0	Line Inversion	○
1	Frame Inversion	-

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Control Data Functions – continued

4. DR: 1/4 bias drive, 1/3 bias drive, 1/2 bias drive or 1/1 bias drive switching control data

This control data bit selects either 1/4 bias drive, 1/3 bias drive, 1/2 bias drive or 1/1 bias drive.

DR0	DR1	Bias drive scheme	Reset condition
0	0	1/3 Bias	○
0	1	1/1 Bias	-
1	0	1/4 Bias	-
1	1	1/2 Bias	-

5. DT: 1/8 duty drive, 1/7 duty drive, 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or Static switching control data

These control data bits select either 1/8 duty drive, 1/7 duty drive, 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or Static

DT0	DT1	DT2	Duty drive scheme	Reset condition
0	0	0	Static drive	-
0	0	1	1/3 duty drive	-
0	1	0	1/4 duty drive	○
0	1	1	1/5 duty drive	-
1	0	0	1/7 duty drive	-
1	0	1	1/8 duty drive	-
1	1	0	1/4 duty drive	-
1	1	1	1/4 duty drive	-

6. FC0, FC1, FC2 and FC3: Common/Segment output waveform frame frequency setting control data

These control data bits set the frame frequency for Common and Segment output waveforms.

FC0	FC1	FC2	FC3	Frame Frequency fo(Hz)	Reset condition
0	0	0	0	fosc(Note18) / 12288	○
0	0	0	1	fosc / 10752	-
0	0	1	0	fosc / 9216	-
0	0	1	1	fosc / 7680	-
0	1	0	0	fosc / 6144	-
0	1	0	1	fosc / 4608	-
0	1	1	0	fosc / 3840	-
0	1	1	1	fosc / 3072	-
1	0	0	0	fosc / 2880	-
1	0	0	1	fosc / 2688	-
1	0	1	0	fosc / 2496	-
1	0	1	1	fosc / 2304	-
1	1	0	0	fosc / 2112	-
1	1	0	1	fosc / 1920	-
1	1	1	0	fosc / 1728	-
1	1	1	1	fosc / 1536	-

(Note18)fosc: Internal Oscillation Frequency (600 [kHz] Typ)

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Control Data Functions – continued

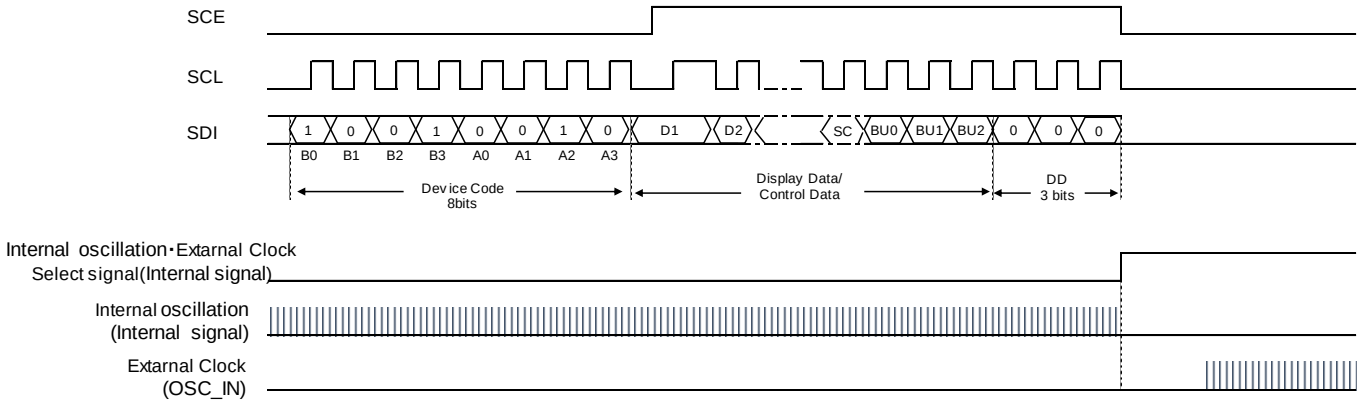
7. OC: Internal oscillator operating mode/External clock operating mode switching control data

This control data bit selects oscillation mode.

OC	Operating mode	In/Out pin(OSC/S70) status	Reset condition
0	Internal oscillator	S70 (Segment output)	○
1	External Clock	OSC_IN (clock input)	-

<External Clock input timing function>

Internal oscillation / external clock select signal behavior is below.
Input external clock after serial data sending.



8. SC: Segment on/off control data

This control data bit controls the on/off state of the Segments.

SC	Display state	Reset condition
0	ON	-
1	OFF	○

Note that when the Segments are turned off by setting SC to “1”, the Segments are turned off by outputting Segment off waveforms from the Segment output pins.

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Control Data Functions – continued

9. BU0, BU1 and BU2: Normal mode/Power-saving mode control data

These control data bits select either normal mode or Power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs	Output Pin States During Key Scan Standby						Reset condition
					Common outputs	KS1	KS2	KS3	KS4	KS5	KS6	
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H	-
0	0	1	Power-saving	Stopped	Low(VSS)	L	L	L	L	L	H	-
0	1	0				L	L	L	L	H	H	-
0	1	1				L	L	L	H	H	H	-
1	0	0				L	L	H	H	H	H	-
1	0	1				L	H	H	H	H	H	-
1	1	0				H	H	H	H	H	H	-
1	1	1				H	H	H	H	H	H	○

Power-saving mode status: S1/P1/G1 to S9/P9/G9 = active only General-Purpose output
S10 to OSC_IN/S70 = low (VSS)
COM1 to COM8 = low (VSS)
Shut off current to the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible when at Power-saving mode.

10. PG1, PG2, PG3, PG4, PG5, PG6, PG7, PG8 and PG9: PWM/ General-Purpose output port control data

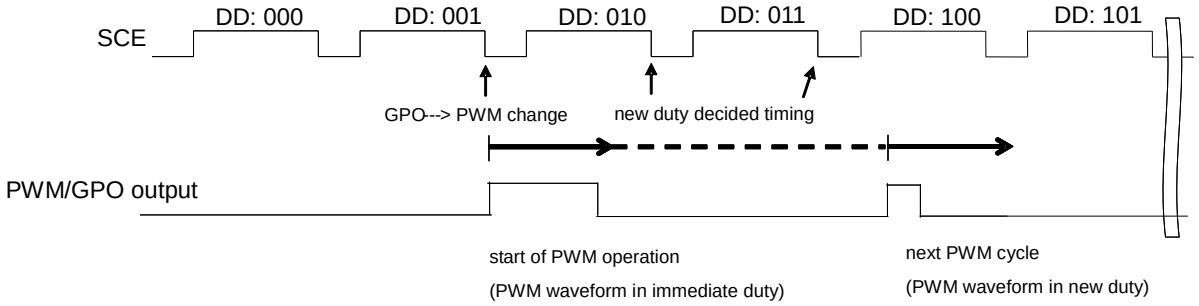
This control data bit select either PWM output or General-Purpose output of Sx/Px/Gx pins. (x=1 to 9)

PGx(x=1 to 9)	Mode	Reset condition
0	PWM output	○
1	General-Purpose output	-

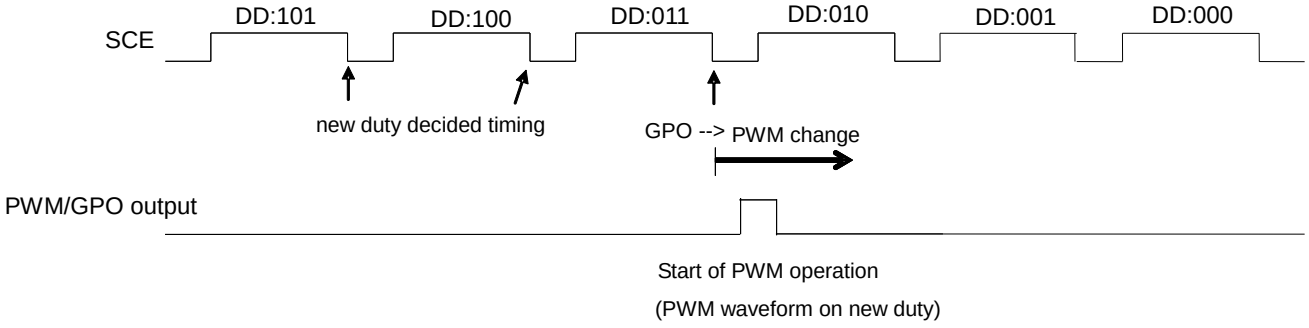
[PWM<->GPO Changing function]

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 001 during GPO → PWM change.
- Please take care of reflect timing of new duty setting of DD: 010 and DD: 011 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



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Control Data Functions – continued

11. PF0, PF1, PF2, and PF3: PWM output waveform frame frequency setting control data

These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM output Frame Frequency fp(Hz)	Reset condition
0	0	0	0	fosc / 4096	○
0	0	0	1	fosc / 3840	-
0	0	1	0	fosc / 3584	-
0	0	1	1	fosc / 3328	-
0	1	0	0	fosc / 3072	-
0	1	0	1	fosc / 2816	-
0	1	1	0	fosc / 2560	-
0	1	1	1	fosc / 2304	-
1	0	0	0	fosc / 2048	-
1	0	0	1	fosc / 1792	-
1	0	1	0	fosc / 1536	-
1	0	1	1	fosc / 1280	-
1	1	0	0	fosc / 1024	-
1	1	0	1	fosc / 768	-
1	1	1	0	fosc / 512	-
1	1	1	1	fosc / 256	-

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Control Data Functions – continued

12. CT0, CT1, CT2 and CT3: Display Contrast setting control data

These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive bias voltage for VLCD Level	Reset condition
0	0	0	0	1.000*VDD	○
0	0	0	1	0.975*VDD	-
0	0	1	0	0.950*VDD	-
0	0	1	1	0.925*VDD	-
0	1	0	0	0.900*VDD	-
0	1	0	1	0.875*VDD	-
0	1	1	0	0.850*VDD	-
0	1	1	1	0.825*VDD	-
1	0	0	0	0.800*VDD	-
1	0	0	1	0.775*VDD	-
1	0	1	0	0.750*VDD	-
1	0	1	1	0.725*VDD	-
1	1	0	0	0.700*VDD	-
1	1	0	1	0.675*VDD	-
1	1	1	0	0.650*VDD	-
1	1	1	1	0.625*VDD	-

Avoid setting VLCD voltage under 2.5V.
And ensure “VDD – VLCD > 0.6V” condition is satisfied.
Unstable IC output voltage may result if the above conditions are not satisfied.

The relationship of LCD display contrast setting and VLCD voltage

CT Setting	formula	VDD= 6.000	VDD= 5.500	VDD= 5.000	VDD= 4.500	VDD= 4.000	VDD= 3.000	[V]
0	VDD	VLCD= 6.000	VLCD= 5.500	VLCD= 5.000	VLCD= 4.500	VLCD= 4.000	VLCD= 3.000	[V]
1	0.975*VDD	VLCD= 5.850	VLCD= 5.363	VLCD= 4.875	VLCD= 4.388	VLCD= 3.900	VLCD= 2.925	[V]
2	0.950*VDD	VLCD= 5.700	VLCD= 5.225	VLCD= 4.750	VLCD= 4.275	VLCD= 3.800	VLCD= 2.850	[V]
3	0.925*VDD	VLCD= 5.550	VLCD= 5.088	VLCD= 4.625	VLCD= 4.163	VLCD= 3.700	VLCD= 2.775	[V]
4	0.900*VDD	VLCD= 5.400	VLCD= 4.950	VLCD= 4.500	VLCD= 4.050	VLCD= 3.600	VLCD= 2.700	[V]
5	0.875*VDD	VLCD= 5.250	VLCD= 4.813	VLCD= 4.375	VLCD= 3.938	VLCD= 3.500	VLCD= 2.625	[V]
6	0.850*VDD	VLCD= 5.100	VLCD= 4.675	VLCD= 4.250	VLCD= 3.825	VLCD= 3.400	VLCD= 2.550	[V]
7	0.825*VDD	VLCD= 4.950	VLCD= 4.538	VLCD= 4.125	VLCD= 3.713	VLCD= 3.300	VLCD= 2.475	[V]
8	0.800*VDD	VLCD= 4.800	VLCD= 4.400	VLCD= 4.000	VLCD= 3.600	VLCD= 3.200	VLCD= 2.400	[V]
9	0.775*VDD	VLCD= 4.650	VLCD= 4.263	VLCD= 3.875	VLCD= 3.488	VLCD= 3.100	VLCD= 2.325	[V]
10	0.750*VDD	VLCD= 4.500	VLCD= 4.125	VLCD= 3.750	VLCD= 3.375	VLCD= 3.000	VLCD= 2.250	[V]
11	0.725*VDD	VLCD= 4.350	VLCD= 3.988	VLCD= 3.625	VLCD= 3.263	VLCD= 2.900	VLCD= 2.175	[V]
12	0.700*VDD	VLCD= 4.200	VLCD= 3.850	VLCD= 3.500	VLCD= 3.150	VLCD= 2.800	VLCD= 2.100	[V]
13	0.675*VDD	VLCD= 4.050	VLCD= 3.713	VLCD= 3.375	VLCD= 3.038	VLCD= 2.700	VLCD= 2.025	[V]
14	0.650*VDD	VLCD= 3.900	VLCD= 3.575	VLCD= 3.250	VLCD= 2.925	VLCD= 2.600	VLCD= 1.950	[V]
15	0.625*VDD	VLCD= 3.750	VLCD= 3.438	VLCD= 3.125	VLCD= 2.813	VLCD= 2.500	VLCD= 1.875	[V]

Disabled

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Control Data Functions – continued

13. W10 to W18(Note19), W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88 and W90 to W98: PWM output waveform duty setting control data. These control data bits set the high level pulse width (duty) for PWM output waveforms.

n = 1 to 9, Tp = 1/fp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM duty	Reset condition
0	0	0	0	0	0	0	0	0	(0/256) x Tp	○
0	0	0	0	0	0	0	0	1	(1/256) x Tp	-
0	0	0	0	0	0	0	1	0	(2/256) x Tp	-
0	0	0	0	0	0	0	1	1	(3/256) x Tp	-
0	0	0	0	0	0	1	0	0	(4/256) x Tp	-
0	0	0	0	0	0	1	0	1	(5/256) x Tp	-
0	0	0	0	0	0	1	1	0	(6/256) x Tp	-
0	0	0	0	0	0	1	1	1	(7/256) x Tp	-
0	0	0	0	0	1	0	0	0	(8/256) x Tp	-
0	0	0	0	0	1	0	0	1	(9/256) x Tp	-
0	0	0	0	0	1	0	1	0	(10/256) x Tp	-
0	0	0	0	0	1	0	1	1	(11/256) x Tp	-
0	0	0	0	0	1	1	0	0	(12/256) x Tp	-
0	0	0	0	0	1	1	0	1	(13/256) x Tp	-
0	0	0	0	0	1	1	1	0	(14/256) x Tp	-
0	0	0	0	0	1	1	1	1	(15/256) x Tp	-
0	0	0	0	1	0	0	0	0	(16/256) x Tp	-
0	0	0	0	1	0	0	0	1	(17/256) x Tp	-
0	0	0	0	1	0	0	1	0	(18/256) x Tp	-
0	0	0	0	1	0	0	1	1	(19/256) x Tp	-
0	0	0	0	1	0	1	0	0	(20/256) x Tp	-
…	…	…	…	…	…	…	…	…	…	-
0	1	1	1	0	1	0	1	1	(235/256) x Tp	-
0	1	1	1	0	1	1	0	0	(236/256) x Tp	-
0	1	1	1	0	1	1	0	1	(237/256) x Tp	-
0	1	1	1	0	1	1	1	0	(238/256) x Tp	-
0	1	1	1	0	1	1	1	1	(239/256) x Tp	-
0	1	1	1	1	0	0	0	0	(240/256) x Tp	-
0	1	1	1	1	0	0	0	1	(241/256) x Tp	-
0	1	1	1	1	0	0	1	0	(242/256) x Tp	-
0	1	1	1	1	0	0	1	1	(243/256) x Tp	-
0	1	1	1	1	0	1	0	0	(244/256) x Tp	-
0	1	1	1	1	0	1	0	1	(245/256) x Tp	-
0	1	1	1	1	0	1	1	0	(246/256) x Tp	-
0	1	1	1	1	0	1	1	1	(247/256) x Tp	-
0	1	1	1	1	1	0	0	0	(248/256) x Tp	-
0	1	1	1	1	1	0	0	1	(249/256) x Tp	-
0	1	1	1	1	1	0	1	0	(250/256) x Tp	-
0	1	1	1	1	1	0	1	1	(251/256) x Tp	-
0	1	1	1	1	1	1	0	0	(252/256) x Tp	-
0	1	1	1	1	1	1	0	1	(253/256) x Tp	-
0	1	1	1	1	1	1	1	0	(254/256) x Tp	-
0	1	1	1	1	1	1	1	1	(255/256) x Tp	-
1	0	0	0	0	0	0	0	0	(256/256) x Tp	-
1	0	0	0	0	0	0	0	1	(256/256) x Tp	-
1	0	0	0	0	0	0	1	0	(256/256) x Tp	-
1	0	0	0	0	0	0	1	1	(256/256) x Tp	-
…	…	…	…	…	…	…	…	…	…	-
1	1	1	1	1	1	1	0	0	(256/256) x Tp	-
1	1	1	1	1	1	1	0	1	(256/256) x Tp	-
1	1	1	1	1	1	1	1	0	(256/256) x Tp	-
1	1	1	1	1	1	1	1	1	(256/256) x Tp	-

(Note19) W10 to W18:S1/P1/G1 PWM duty data
W20 to W28:S2/P2/G2 PWM duty data
W30 to W38:S3/P3/G3 PWM duty data
W40 to W48:S4/P4/G4 PWM duty data
W50 to W58:S5/P5/G5 PWM duty data
W60 to W68:S6/P6/G6 PWM duty data
W70 to W78:S7/P7/G7 PWM duty data
W80 to W88:S8/P8/G8 PWM duty data
W90 to W98:S9/P9/G9 PWM duty data

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Display Data and Output Pin Correspondence

1. 1/8 Duty

Output Pin(Note20)	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
S1/P1/G1	D1	D2	D3	D4	D5	D6	D7	D8
S2/P2/G2	D9	D10	D11	D12	D13	D14	D15	D16
S3/P3/G3	D17	D18	D19	D20	D21	D22	D23	D24
S4/P4/G4	D25	D26	D27	D28	D29	D30	D31	D32
S5/P5/G5	D33	D34	D35	D36	D37	D38	D39	D40
S6/P6/G6	D41	D42	D43	D44	D45	D46	D47	D48
S7/P7/G7	D49	D50	D51	D52	D53	D54	D55	D56
S8/P8/G8	D57	D58	D59	D60	D61	D62	D63	D64
S9/P9/G9	D65	D66	D67	D68	D69	D70	D71	D72
S10	D73	D74	D75	D76	D77	D78	D79	D80
S11	D81	D82	D83	D84	D85	D86	D87	D88
S12	D89	D90	D91	D92	D93	D94	D95	D96
S13	D97	D98	D99	D100	D101	D102	D103	D104
S14	D105	D106	D107	D108	D109	D110	D111	D112
S15	D113	D114	D115	D116	D117	D118	D119	D120
S16	D121	D122	D123	D124	D125	D126	D127	D128
S17	D129	D130	D131	D132	D133	D134	D135	D136
S18	D137	D138	D139	D140	D141	D142	D143	D144
S19	D145	D146	D147	D148	D149	D150	D151	D152
S20	D153	D154	D155	D156	D157	D158	D159	D160
S21	D161	D162	D163	D164	D165	D166	D167	D168
S22	D169	D170	D171	D172	D173	D174	D175	D176
S23	D177	D178	D179	D180	D181	D182	D183	D184
S24	D185	D186	D187	D188	D189	D190	D191	D192
S25	D193	D194	D195	D196	D197	D198	D199	D200
S26	D201	D202	D203	D204	D205	D206	D207	D208
S27	D209	D210	D211	D212	D213	D214	D215	D216
S28	D217	D218	D219	D220	D221	D222	D223	D224
S29	D225	D226	D227	D228	D229	D230	D231	D232
S30	D233	D234	D235	D236	D237	D238	D239	D240
S31	D241	D242	D243	D244	D245	D246	D247	D248
S32	D249	D250	D251	D252	D253	D254	D255	D256
S33	D257	D258	D259	D260	D261	D262	D263	D264
S34	D265	D266	D267	D268	D269	D270	D271	D272
S35	D273	D274	D275	D276	D277	D278	D279	D280
S36	D281	D282	D283	D284	D285	D286	D287	D288
S37	D289	D290	D291	D292	D293	D294	D295	D296
S38	D297	D298	D299	D300	D301	D302	D303	D304
S39	D305	D306	D307	D308	D309	D310	D311	D312
S40	D313	D314	D315	D316	D317	D318	D319	D320
S41	D321	D322	D323	D324	D325	D326	D327	D328
S42	D329	D330	D331	D332	D333	D334	D335	D336
S43	D337	D338	D339	D340	D341	D342	D343	D344
S44	D345	D346	D347	D348	D349	D350	D351	D352
S45	D353	D354	D355	D356	D357	D358	D359	D360
S46	D361	D362	D363	D364	D365	D366	D367	D368
S47	D369	D370	D371	D372	D373	D374	D375	D376
S48	D377	D378	D379	D380	D381	D382	D383	D384
S49	D385	D386	D387	D388	D389	D390	D391	D392
S50	D393	D394	D395	D396	D397	D398	D399	D400
S51	D401	D402	D403	D404	D405	D406	D407	D408
S52	D409	D410	D411	D412	D413	D414	D415	D416
KS1/S53	D417	D418	D419	D420	D421	D422	D423	D424
KS2/S54	D425	D426	D427	D428	D429	D430	D431	D432
KS3/S55	D433	D434	D435	D436	D437	D438	D439	D440
KS4/S56	D441	D442	D443	D444	D445	D446	D447	D448
KS5/S57	D449	D450	D451	D452	D453	D454	D455	D456
KS6/S58	D457	D458	D459	D460	D461	D462	D463	D464
KI1/S59	D465	D466	D467	D468	D469	D470	D471	D472
KI2/S60	D473	D474	D475	D476	D477	D478	D479	D480
KI3/S61	D481	D482	D483	D484	D485	D486	D487	D488
KI4/S62	D489	D490	D491	D492	D493	D494	D495	D496
KI5/S63	D497	D498	D499	D500	D501	D502	D503	D504

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Display Data and Output Pin Correspondence – continued

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
COM8/S64								
COM7/S65								
COM6/S66								
COM5/S67								
S68	D505	D506	D507	D508	D509	D510	D511	D512
S69	D513	D514	D515	D516	D517	D518	D519	D520
OSC_IN/S70	D521	D522	D523	D524	D525	D526	D527	D528

(Note20) The Segment output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, KI1/S59 to KI5/S63 and OSC_IN/S70. Also, COM8/S64, COM7/S65, COM6/S66, COM5/S67 pins are used as Common outputs.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data								State of S21 output Pin
D161	D162	D163	D164	D165	D166	D167	D168	
0	0	0	0	0	0	0	0	LCD Segments corresponding to COM1 to COM8 are OFF.
0	0	0	0	0	0	0	1	LCD Segment corresponding to COM8 is ON.
0	0	0	0	0	0	1	0	LCD Segment corresponding to COM7 is ON.
0	0	0	0	0	0	1	1	LCD Segments corresponding to COM7 and COM8 are ON.
0	0	0	0	0	1	0	0	LCD Segment corresponding to COM6 is ON.
0	0	0	0	0	1	0	1	LCD Segments corresponding to COM6 and COM8 are ON.
0	0	0	0	0	1	1	0	LCD Segments corresponding to COM6 and COM7 are ON.
0	0	0	0	0	1	1	1	LCD Segments corresponding to COM6, COM7 and COM8 are ON.
0	0	0	0	1	0	0	0	LCD Segment corresponding to COM5 is ON.
0	0	0	0	1	0	0	1	LCD Segments corresponding to COM5 and COM8 are ON.
0	0	0	0	1	0	1	0	LCD Segments corresponding to COM5 and COM7 are ON.
0	0	0	0	1	0	1	1	LCD Segments corresponding to COM5, COM7 and COM8 are ON.
0	0	0	0	1	1	0	0	LCD Segments corresponding to COM5 and COM6 are ON.
0	0	0	0	1	1	0	1	LCD Segments corresponding to COM5, COM6, and COM8 are ON.
0	0	0	0	1	1	1	0	LCD Segments corresponding to COM5, COM6, and COM7 are ON.
0	0	0	0	1	1	1	1	LCD Segments corresponding to COM5, COM6, COM7 and COM8 are ON.
0	0	0	1	0	0	0	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	0	0	0	1	LCD Segments corresponding to COM4 and COM8 are ON.
0	0	0	1	0	0	1	0	LCD Segments corresponding to COM4 and COM7 are ON.
0	0	0	1	0	0	1	1	LCD Segments corresponding to COM4, COM7 and COM8 are ON.
0	0	0	1	0	1	0	0	LCD Segments corresponding to COM4 and COM6 are ON.
0	0	0	1	0	1	0	1	LCD Segments corresponding to COM4, COM6 and COM8 are ON.
0	0	0	1	0	1	1	0	LCD Segments corresponding to COM4, COM6 and COM7 are ON.
0	0	0	1	0	1	1	1	LCD Segments corresponding to COM4, COM6, COM7 and COM8 are ON.
0	0	0	1	1	0	0	0	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	0	1	1	0	0	1	LCD Segments corresponding to COM4, COM5 and COM8 are ON.
0	0	0	1	1	0	1	0	LCD Segments corresponding to COM4, COM5 and COM7 are ON.
0	0	0	1	1	0	1	1	LCD Segments corresponding to COM4, COM5, COM7 and COM8 are ON.
0	0	0	1	1	1	0	0	LCD Segments corresponding to COM4, COM5 and COM6 are ON.
0	0	0	1	1	1	0	1	LCD Segments corresponding to COM4, COM5, COM6 and COM8 are ON.
0	0	0	1	1	1	1	0	LCD Segments corresponding to COM4, COM5, COM6 and COM7 are ON.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	LCD Segments corresponding to COM1 to COM8 are ON.

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Display Data and Output Pin Correspondence – continued

2. 1/7 Duty

Output Pin(Note21)	COM1	COM2	COM3	COM4	COM5	COM6	COM7
S1/P1/G1	D1	D2	D3	D4	D5	D6	D7
S2/P2/G2	D8	D9	D10	D11	D12	D13	D14
S3/P3/G3	D15	D16	D17	D18	D19	D20	D21
S4/P4/G4	D22	D23	D24	D25	D26	D27	D28
S5/P5/G5	D29	D30	D31	D32	D33	D34	D35
S6/P6/G6	D36	D37	D38	D39	D40	D41	D42
S7/P7/G7	D43	D44	D45	D46	D47	D48	D49
S8/P8/G8	D50	D51	D52	D53	D54	D55	D56
S9/P9/G9	D57	D58	D59	D60	D61	D62	D63
S10	D64	D65	D66	D67	D68	D69	D70
S11	D71	D72	D73	D74	D75	D76	D77
S12	D78	D79	D80	D81	D82	D83	D84
S13	D85	D86	D87	D88	D89	D90	D91
S14	D92	D93	D94	D95	D96	D97	D98
S15	D99	D100	D101	D102	D103	D104	D105
S16	D106	D107	D108	D109	D110	D111	D112
S17	D113	D114	D115	D116	D117	D118	D119
S18	D120	D121	D122	D123	D124	D125	D126
S19	D127	D128	D129	D130	D131	D132	D133
S20	D134	D135	D136	D137	D138	D139	D140
S21	D141	D142	D143	D144	D145	D146	D147
S22	D148	D149	D150	D151	D152	D153	D154
S23	D155	D156	D157	D158	D159	D160	D161
S24	D162	D163	D164	D165	D166	D167	D168
S25	D169	D170	D171	D172	D173	D174	D175
S26	D176	D177	D178	D179	D180	D181	D182
S27	D183	D184	D185	D186	D187	D188	D189
S28	D190	D191	D192	D193	D194	D195	D196
S29	D197	D198	D199	D200	D201	D202	D203
S30	D204	D205	D206	D207	D208	D209	D210
S31	D211	D212	D213	D214	D215	D216	D217
S32	D218	D219	D220	D221	D222	D223	D224
S33	D225	D226	D227	D228	D229	D230	D231
S34	D232	D233	D234	D235	D236	D237	D238
S35	D239	D240	D241	D242	D243	D244	D245
S36	D246	D247	D248	D249	D250	D251	D252
S37	D253	D254	D255	D256	D257	D258	D259
S38	D260	D261	D262	D263	D264	D265	D266
S39	D267	D268	D269	D270	D271	D272	D273
S40	D274	D275	D276	D277	D278	D279	D280
S41	D281	D282	D283	D284	D285	D286	D287
S42	D288	D289	D290	D291	D292	D293	D294
S43	D295	D296	D297	D298	D299	D300	D301
S44	D302	D303	D304	D305	D306	D307	D308
S45	D309	D310	D311	D312	D313	D314	D315
S46	D316	D317	D318	D319	D320	D321	D322
S47	D323	D324	D325	D326	D327	D328	D329
S48	D330	D331	D332	D333	D334	D335	D336
S49	D337	D338	D339	D340	D341	D342	D343
S50	D344	D345	D346	D347	D348	D349	D350
S51	D351	D352	D353	D354	D355	D356	D357
S52	D358	D359	D360	D361	D362	D363	D364
KS1/S53	D365	D366	D367	D368	D369	D370	D371
KS2/S54	D372	D373	D374	D375	D376	D377	D378
KS3/S55	D379	D380	D381	D382	D383	D384	D385
KS4/S56	D386	D387	D388	D389	D390	D391	D392
KS5/S57	D393	D394	D395	D396	D397	D398	D399
KS6/S58	D400	D401	D402	D403	D404	D405	D406
KI1/S59	D407	D408	D409	D410	D411	D412	D413
KI2/S60	D414	D415	D416	D417	D418	D419	D420
KI3/S61	D421	D422	D423	D424	D425	D426	D427
KI4/S62	D428	D429	D430	D431	D432	D433	D434
KI5/S63	D435	D436	D437	D438	D439	D440	D441

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Display Data and Output Pin Correspondence – continued

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7
COM8 / S64	D442	D443	D444	D445	D446	D447	D448
COM7 / S65							
COM6 / S66							
COM5 / S67							
S68	D449	D450	D451	D452	D453	D454	D455
S69	D456	D457	D458	D459	D460	D461	D462
OSC_IN/S70	D463	D464	D465	D466	D467	D468	D469

(Note21) The Segment output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, KI1/S59 to KI5/S63 and OSC_IN/S70. Also, COM7/S65, COM6/S66, COM5/S67 pins are used as Common outputs.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data							State of S21 output Pin
D141	D142	D143	D144	D145	D146	D147	
0	0	0	0	0	0	0	LCD Segments corresponding to COM1 to COM7 are OFF.
0	0	0	0	0	0	1	LCD Segment corresponding to COM7 is ON.
0	0	0	0	0	1	0	LCD Segment corresponding to COM6 is ON.
0	0	0	0	0	1	1	LCD Segments corresponding to COM6 and COM7 are ON.
0	0	0	0	1	0	0	LCD Segment corresponding to COM5 is ON.
0	0	0	0	1	0	1	LCD Segments corresponding to COM5 and COM7 are ON.
0	0	0	0	1	1	0	LCD Segments corresponding to COM5 and COM6 are ON.
0	0	0	0	1	1	1	LCD Segments corresponding to COM5, COM6 and COM7 are ON.
0	0	0	1	0	0	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	0	0	1	LCD Segments corresponding to COM4 and COM7 are ON.
0	0	0	1	0	1	0	LCD Segments corresponding to COM4 and COM6 are ON
0	0	0	1	0	1	1	LCD Segments corresponding to COM4, COM6 and COM7 are ON.
0	0	0	1	1	0	0	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	0	1	1	0	1	LCD Segments corresponding to COM4, COM5, and COM7 are ON.
0	0	0	1	1	1	0	LCD Segments corresponding to COM4, COM5, and COM6 are ON.
0	0	0	1	1	1	1	LCD Segments corresponding to COM4, COM5, COM6 and COM7 are ON.
0	0	1	0	0	0	0	LCD Segment corresponding to COM3 is ON.
0	0	1	0	0	0	1	LCD Segments corresponding to COM3 and COM7 are ON.
0	0	1	0	0	1	0	LCD Segments corresponding to COM3 and COM6 are ON.
0	0	1	0	0	1	1	LCD Segments corresponding to COM3, COM6 and COM7 are ON.
0	0	1	0	1	0	0	LCD Segments corresponding to COM3 and COM5 are ON.
0	0	1	0	1	0	1	LCD Segments corresponding to COM3, COM5 and COM7 are ON.
0	0	1	0	1	1	0	LCD Segments corresponding to COM3, COM5 and COM6 are ON.
0	0	1	0	1	1	1	LCD Segments corresponding to COM3, COM5, COM6 and COM7 are ON.
0	0	1	1	0	0	0	LCD Segments corresponding to COM3 and COM4 are ON.
0	0	1	1	0	0	1	LCD Segments corresponding to COM3, COM4 and COM7 are ON.
0	0	1	1	0	1	0	LCD Segments corresponding to COM3, COM4 and COM6 are ON.
0	0	1	1	0	1	1	LCD Segments corresponding to COM3, COM4, COM6 and COM7 are ON.
0	0	1	1	1	0	0	LCD Segments corresponding to COM3, COM4 and COM5 are ON.
0	0	1	1	1	0	1	LCD Segments corresponding to COM3, COM4, COM5 and COM7 are ON.
0	0	1	1	1	1	0	LCD Segments corresponding to COM3, COM4, COM5 and COM6 are ON.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	LCD Segments corresponding to COM1 to COM7 are ON.

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Display Data and Output Pin Correspondence – continued

3. 1/5 duty

Output Pin(Note22)	COM1	COM2	COM3	COM4	COM5
S1/P1/G1	D1	D2	D3	D4	D5
S2/P2/G2	D6	D7	D8	D9	D10
S3/P3/G3	D11	D12	D13	D14	D15
S4/P4/G4	D16	D17	D18	D19	D20
S5/P5/G5	D21	D22	D23	D24	D25
S6/P6/G6	D26	D27	D28	D29	D30
S7/P7/G7	D31	D32	D33	D34	D35
S8/P8/G8	D36	D37	D38	D39	D40
S9/P9/G9	D41	D42	D43	D44	D45
S10	D46	D47	D48	D49	D50
S11	D51	D52	D53	D54	D55
S12	D56	D57	D58	D59	D60
S13	D61	D62	D63	D64	D65
S14	D66	D67	D68	D69	D70
S15	D71	D72	D73	D74	D75
S16	D76	D77	D78	D79	D80
S17	D81	D82	D83	D84	D85
S18	D86	D87	D88	D89	D90
S19	D91	D92	D93	D94	D95
S20	D96	D97	D98	D99	D100
S21	D101	D102	D103	D104	D105
S22	D106	D107	D108	D109	D110
S23	D111	D112	D113	D114	D115
S24	D116	D117	D118	D119	D120
S25	D121	D122	D123	D124	D125
S26	D126	D127	D128	D129	D130
S27	D131	D132	D133	D134	D135
S28	D136	D137	D138	D139	D140
S29	D141	D142	D143	D144	D145
S30	D146	D147	D148	D149	D150
S31	D151	D152	D153	D154	D155
S32	D156	D157	D158	D159	D160
S33	D161	D162	D163	D164	D165
S34	D166	D167	D168	D169	D170
S35	D171	D172	D173	D174	D175
S36	D176	D177	D178	D179	D180
S37	D181	D182	D183	D184	D185
S38	D186	D187	D188	D189	D190
S39	D191	D192	D193	D194	D195
S40	D196	D197	D198	D199	D200
S41	D201	D202	D203	D204	D205
S42	D206	D207	D208	D209	D210
S43	D211	D212	D213	D214	D215
S44	D216	D217	D218	D219	D220
S45	D221	D222	D223	D224	D225
S46	D226	D227	D228	D229	D230
S47	D231	D232	D233	D234	D235
S48	D236	D237	D238	D239	D240
S49	D241	D242	D243	D244	D245
S50	D246	D247	D248	D249	D250
S51	D251	D252	D253	D254	D255
S52	D256	D257	D258	D259	D260
KS1/S53	D261	D262	D263	D264	D265
KS2/S54	D266	D267	D268	D269	D270
KS3/S55	D271	D272	D273	D274	D275
KS4/S56	D276	D277	D278	D279	D280
KS5/S57	D281	D282	D283	D284	D285
KS6/S58	D286	D287	D288	D289	D290
KI1/S59	D291	D292	D293	D294	D295
KI2/S60	D296	D297	D298	D299	D300
KI3/S61	D301	D302	D303	D304	D305
KI4/S62	D306	D307	D308	D309	D310
KI5/S63	D311	D312	D313	D314	D315

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Display Data and Output Pin Correspondence – continued

Output Pin	COM1	COM2	COM3	COM4	COM5
COM8/S64	D316	D317	D318	D319	D320
COM7/S65	D321	D322	D323	D324	D325
COM6/S66	D326	D327	D328	D329	D330
COM5/S67					
S68	D331	D332	D333	D334	D335
S69	D336	D337	D338	D339	D340
OSC_IN/S70	D341	D342	D343	D344	D345

(Note22) The Segment output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, KI1/S59 to KI5/S63 and OSC_IN/S70. Also, COM5/S67 pins are used as Common outputs.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data					State of S21 output Pin
D101	D102	D103	D104	D105	
0	0	0	0	0	LCD Segments corresponding to COM1 to COM5 are OFF.
0	0	0	0	1	LCD Segment corresponding to COM5 is ON.
0	0	0	1	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	1	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	1	0	0	LCD Segment corresponding to COM3 is ON.
0	0	1	0	1	LCD Segments corresponding to COM3 and COM5 are ON.
0	0	1	1	0	LCD Segments corresponding to COM3 and COM4 are ON.
0	0	1	1	1	LCD Segments corresponding to COM3, COM4 and COM5 are ON.
0	1	0	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	0	1	LCD Segments corresponding to COM2 and COM5 are ON.
0	1	0	1	0	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	0	1	1	LCD Segments corresponding to COM2, COM4 and COM5 are ON.
0	1	1	0	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	0	1	LCD Segments corresponding to COM2, COM3, and COM5 are ON.
0	1	1	1	0	LCD Segments corresponding to COM2, COM3, and COM4 are ON.
0	1	1	1	1	LCD Segments corresponding to COM2, COM3, COM4 and COM5 are ON.
1	0	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	0	1	LCD Segments corresponding to COM1 and COM5 are ON.
1	0	0	1	0	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	0	1	1	LCD Segments corresponding to COM1, COM4 and COM5 are ON.
1	0	1	0	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	0	1	LCD Segments corresponding to COM1, COM3 and COM5 are ON.
1	0	1	1	0	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	0	1	1	1	LCD Segments corresponding to COM1, COM3, COM4 and COM5 are ON.
1	1	0	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	0	1	LCD Segments corresponding to COM1, COM2 and COM5 are ON.
1	1	0	1	0	LCD Segments corresponding to COM1, COM2 and COM4 are ON.
1	1	0	1	1	LCD Segments corresponding to COM1, COM2, COM4 and COM5 are ON.
1	1	1	0	0	LCD Segments corresponding to COM1, COM2 and COM3 are ON.
1	1	1	0	1	LCD Segments corresponding to COM1, COM2, COM3 and COM5 are ON.
1	1	1	1	0	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.
1	1	1	1	1	LCD Segments corresponding to COM1 to COM5 are ON.

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Display Data and Output Pin Correspondence – continued

4. 1/4 duty

Output Pin(Note23)	COM1	COM2	COM3	COM4
S1/P1/G1	D1	D2	D3	D4
S2/P2/G2	D5	D6	D7	D8
S3/P3/G3	D9	D10	D11	D12
S4/P4/G4	D13	D14	D15	D16
S5/P5/G5	D17	D18	D19	D20
S6/P6/G6	D21	D22	D23	D24
S7/P7/G7	D25	D26	D27	D28
S8/P8/G8	D29	D30	D31	D32
S9/P9/G9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
KS1/S53	D209	D210	D211	D212
KS2/S54	D213	D214	D215	D216
KS3/S55	D217	D218	D219	D220
KS4/S56	D221	D222	D223	D224
KS5/S57	D225	D226	D227	D228
KS6/S58	D229	D230	D231	D232
KI1/S59	D233	D234	D235	D236
KI2/S60	D237	D238	D239	D240
KI3/S61	D241	D242	D243	D244
KI4/S62	D245	D246	D247	D248
KI5/S63	D249	D250	D251	D252

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Display Data and Output Pin Correspondence – continued

Output Pin	COM1	COM2	COM3	COM4
COM8/S64	D253	D254	D255	D256
COM7/S65	D257	D258	D259	D260
COM6/S66	D261	D262	D263	D264
COM5/S67	D265	D266	D267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276
OSC_IN/S70	D277	D278	D279	D280

(Note23) The Segment output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, KI1/S59 to KI5/S63 and OSC_IN/S70.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data				State of S21 output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1 to COM4 are ON.

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Display Data and Output Pin Correspondence – continued

5. 1/3 duty

Output Pin(Note24)	COM1	COM2	COM3
S1/P1/G1	D1	D2	D3
S2/P2/G2	D4	D5	D6
S3/P3/G3	D7	D8	D9
S4/P4/G4	D10	D11	D12
S5/P5/G5	D13	D14	D15
S6/P6/G6	D16	D17	D18
S7/P7/G7	D19	D20	D21
S8/P8/G8	D22	D23	D24
S9/P9/G9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D85	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
KS1/S53	D157	D158	D159
KS2/S54	D160	D161	D162
KS3/S55	D163	D164	D165
KS4/S56	D166	D167	D168
KS5/S57	D169	D170	D171
KS6/S58	D172	D173	D174
KI1/S59	D175	D176	D177
KI2/S60	D178	D179	D180
KI3/S61	D181	D182	D183
KI4/S62	D184	D185	D186
KI5/S63	D187	D188	D189

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Display Data and Output Pin Correspondence – continued

Output Pin	COM1	COM2	COM3
COM8/S64	D190	D191	D192
COM7/S65	D193	D194	D195
COM6/S66	D196	D197	D198
COM5/S67	D199	D200	D201
S68	D202	D203	D204
S69	D205	D206	D207
OSC_IN/S70	D208	D209	D210

(Note24) The Segment output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, KI1/S59 to KI5/S63 and OSC_IN/S70.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data			State of S21 output Pin
D61	D62	D63	
0	0	0	LCD Segments corresponding to COM1 to COM3 are OFF.
0	0	1	LCD Segment corresponding to COM3 is ON.
0	1	0	LCD Segment corresponding to COM2 is ON.
0	1	1	LCD Segments corresponding to COM2 and COM3 are ON.
1	0	0	LCD Segment corresponding to COM1 is ON.
1	0	1	LCD Segments corresponding to COM1 and COM3 are ON.
1	1	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	1	LCD Segments corresponding to COM1 to COM3 are ON.

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Display Data and Output Pin Correspondence – continued

6. Static

Output Pin(Note25)	COM1
S1/P1/G1	D1
S2/P2/G2	D2
S3/P3/G3	D3
S4/P4/G4	D4
S5/P5/G5	D5
S6/P6/G6	D6
S7/P7/G7	D7
S8/P8/G8	D8
S9/P9/G9	D9
S10	D10
S11	D11
S12	D12
S13	D13
S14	D14
S15	D15
S16	D16
S17	D17
S18	D18
S19	D19
S20	D20
S21	D21
S22	D22
S23	D23
S24	D24
S25	D25
S26	D26
S27	D27
S28	D28
S29	D29
S30	D30
S31	D31
S32	D32
S33	D33
S34	D34
S35	D35
S36	D36
S37	D37
S38	D38
S39	D39
S40	D40
S41	D41
S42	D42
S43	D43
S44	D44
S45	D45
S46	D46
S47	D47
S48	D48
S49	D49
S50	D50
S51	D51
S52	D52
KS1/S53	D53
KS2/S54	D54
KS3/S55	D55
KS4/S56	D56
KS5/S57	D57
KS6/S58	D58
KI1/S59	D59
KI2/S60	D60
KI3/S61	D61
KI4/S62	D62
KI5/S63	D63

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Display Data and Output Pin Correspondence – continued

Output Pin	COM1
COM8/S64	D64
COM7/S65	D65
COM6/S66	D66
COM5/S67	D67
S68	D68
S69	D69
OSC_IN/S70	D70

(Note25) The Segment output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, KI1/S59 to KI5/S63 and OSC_IN/S70.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data D21	State of S21 output Pin
0	LCD Segment corresponding to COM1 is OFF.
1	LCD Segment corresponding to COM1 is ON.

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Serial Data Output

1. When SCL is stopped at the low level(Note26)

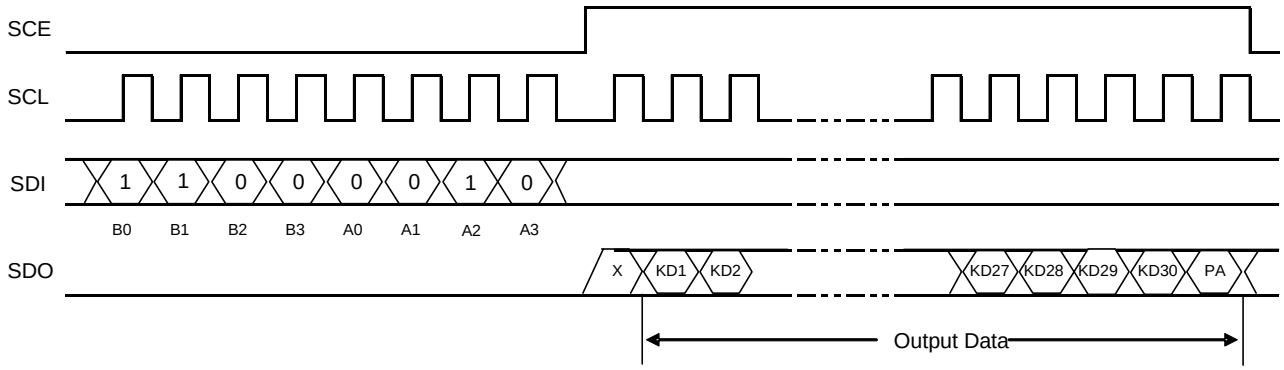


Figure 19. Serial Data Output Format

(Note26)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address

2. When SCL is stopped at the high level(Note27)

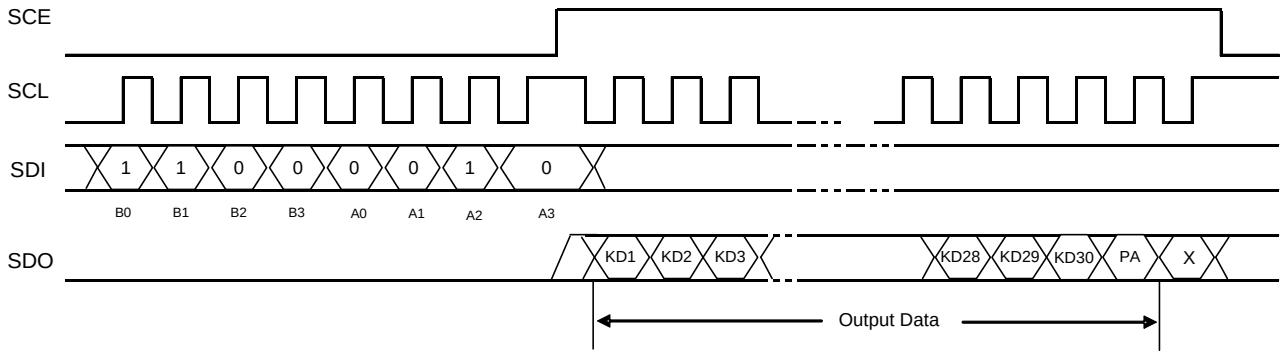


Figure 20. Serial Data Output Format

(Note27)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address
3. Serial Interface address: 43H
4. KD1 to KD30: Key data
5. PA: Power-saving acknowledge data
6. If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and Power-saving acknowledge data (PA) will be invalid.

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Output Data

1. KD1 to KD30: KEY DATA

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

Item	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

2. PA: Power-saving Acknowledge Data

This output data is set to the state of normal mode or Power-saving mode.
PA is set to 1 in the Power-saving mode and to 0 in the normal mode.

Power-saving Mode

Power-saving mode is activated when least one of control data BU0 or BU1 or BU2 is set to 1. All Segment and Common outputs will go low. The oscillation circuit will stop (It can be restarted by a key press), thus reducing power consumption. This mode can be disabled when control data bits BU0, BU1 and BU2 are all set to 0. However, note that the S1/P1/G1 to S9/P9/G9 outputs can still be used as General-Purpose output ports according to the state of the P0 to P2 control data bits, even in Power-saving mode. (See Control Data Functions.)

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Key Scan Operation Functions

1. Key Scan Timing

The key scan period is 4608T(s). To reliably determine the on/off state of the keys, the BU97550KV-M scans the keys twice and determines that a key has been pressed when the key data agrees. Then it outputs a key data read request (a low level on SDO) 9840T(s) after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the BU97550KV-M cannot detect a key press shorter than 9840T(s).

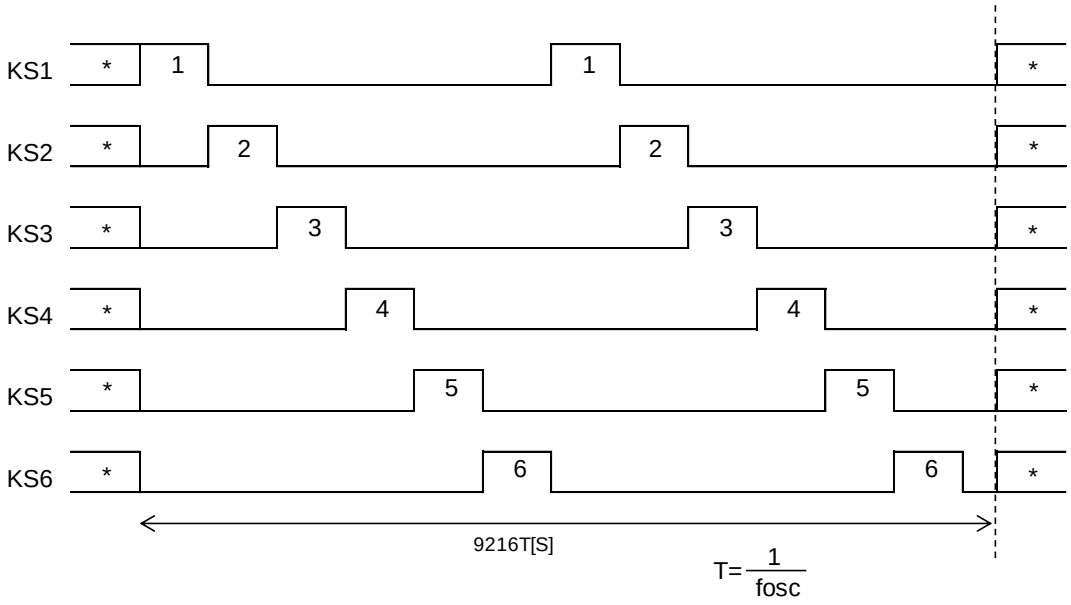


Figure 21. Key Scan Timing(Note28)

(Note28) In Power-saving mode, the “H” or “L” state of these pins is determined by the BU0 to BU2 bits in the control data. Key scan output signals are not output from pins that are set “L”.

2. In Normal Mode

The pins KS1 to KS6 output are set “H”.

When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than 9840T(s) (Where T=1/fosc) the BU97550KV-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set high.

After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97550KV-M performs another key scan. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1kΩ to 10kΩ).

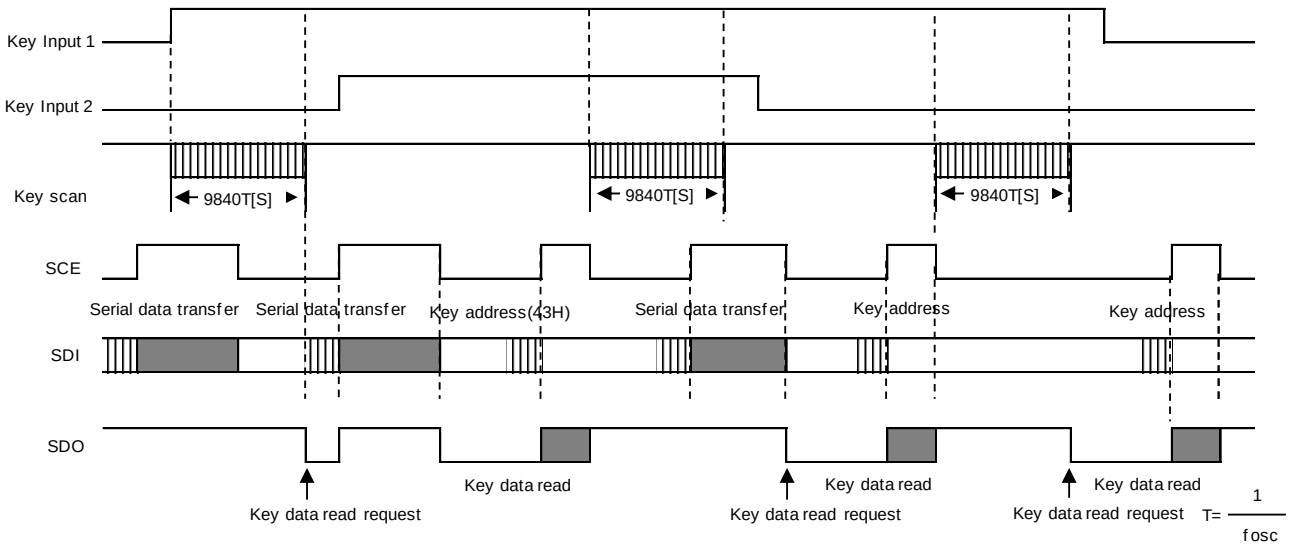


Figure 22. Key scan operation in normal mode

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Key Scan Operation Functions – continued

3. In Power-saving Mode

The pins KS1 to KS6 output high or low level by the BU0 to BU2 bits in the control data. (See the control data Functions for details.)

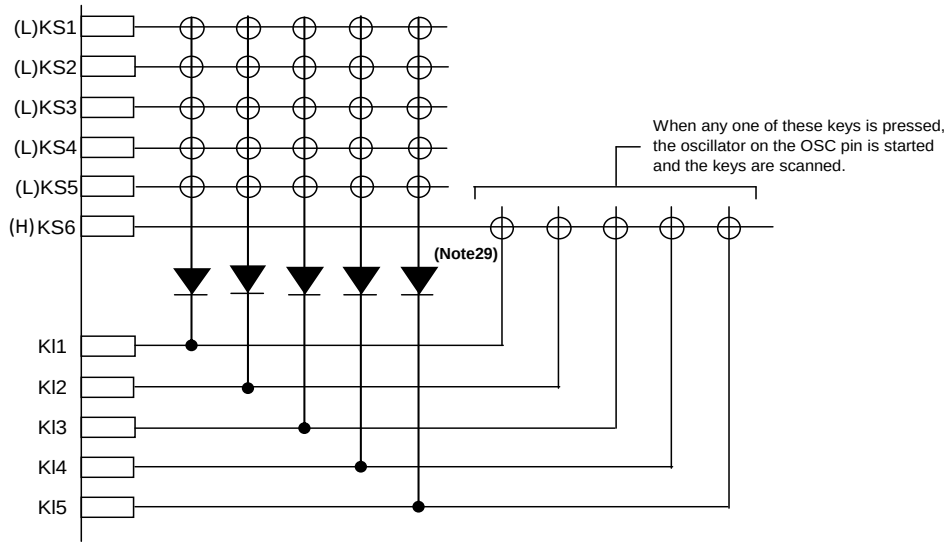
If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC_IN pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than 9840T(s)(Where T=1/fosc) the BU97550KV-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set high.

After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97550KV-M performs another key scan. However, this does not clear Power-saving mode. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1 kΩ to 10kΩ).

Power-saving mode key scan example

Example: BU0=0, BU1=0, BU2=1 (only KS6 high level output)



(Note 29)
These diodes are required to reliable recognize multiple key presses on the KS6 line when Power-saving mode state with only KS6 high, as in the above example.
That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.

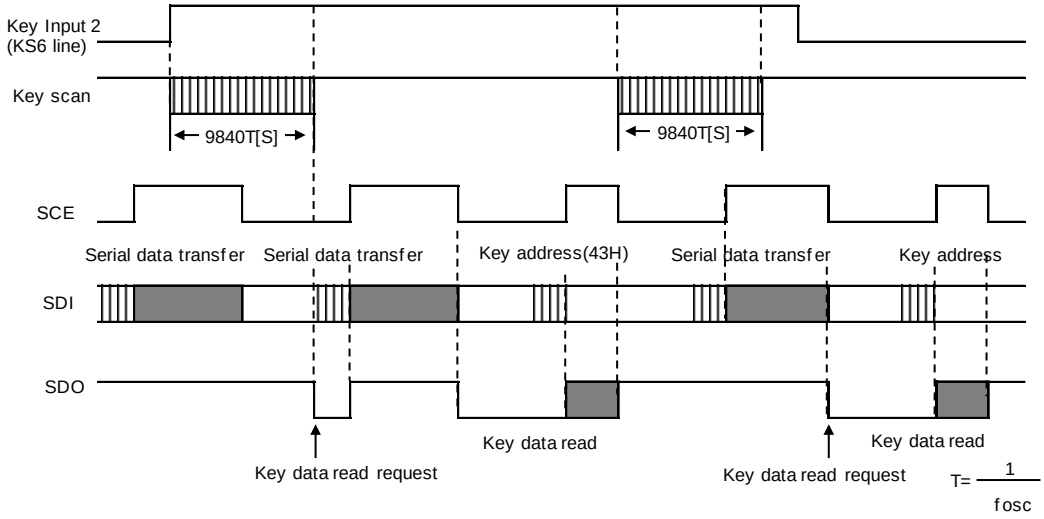


Figure 23. Key scan operation in Power-saving mode

4. Multiple Key Presses

Although the BU97550KV-M is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bit and ignore such data.

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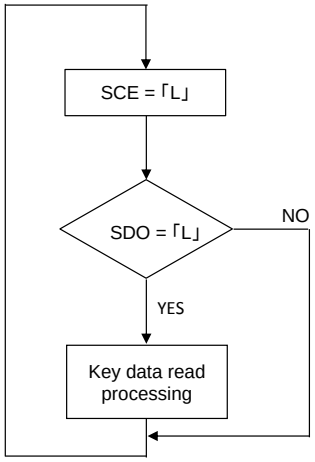
Key Scan Operation Functions – continued

5. Controller Key Data Read Techniques

When the controller receives a key data read request from BU97550KV-M, it performs a key data read acquisition operation using either the Timer Based Key Data Acquisition or the Interrupt Based Key Data Acquisition.

6. Timer Based Key Data Acquisition Technique

Under the Timer Based Key Data Acquisition Technique, the controller uses a timer to determine the states of the keys (on or off) and read the key data. Please refer to the flowchart below.



Key data read processing: Refer to “Serial Data Output”

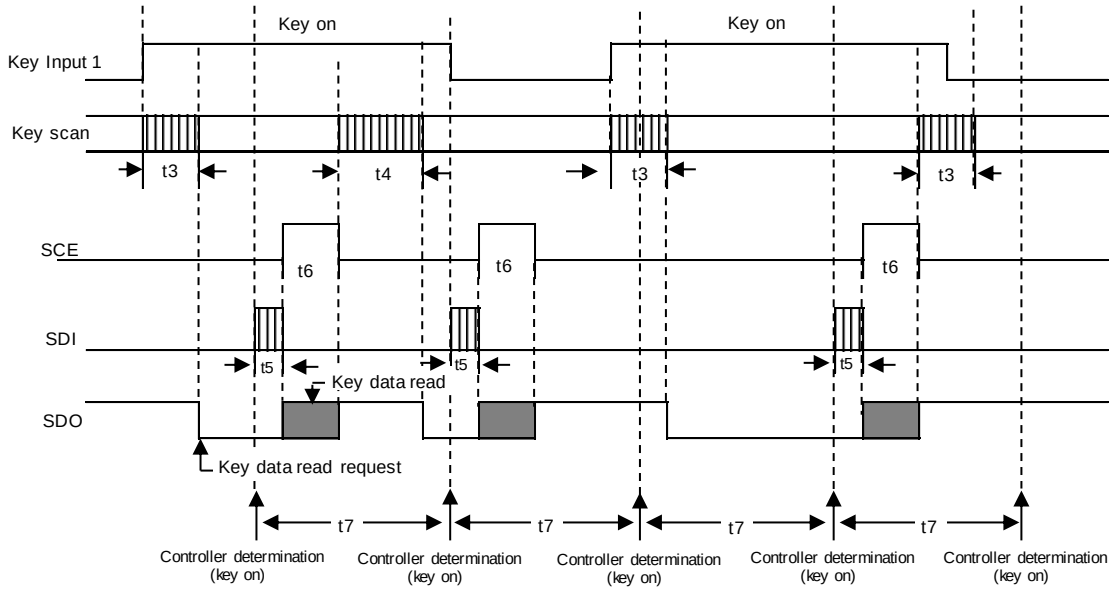
Figure 24. Flowchart

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low every t7 period without fail. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

The period t7 in this technique must satisfy the following condition.

t7>t4+t5+t6

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and Power-saving acknowledge data (PA) will be invalid.



t3: Key scan execution time when the key data agreed for two key scans. (9840T[s])

t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (19680T[s]) T = 1 / fosc

t5: Key address (43H) transfer time

t6: Key data read time

Figure 25. Timer based key data read operation

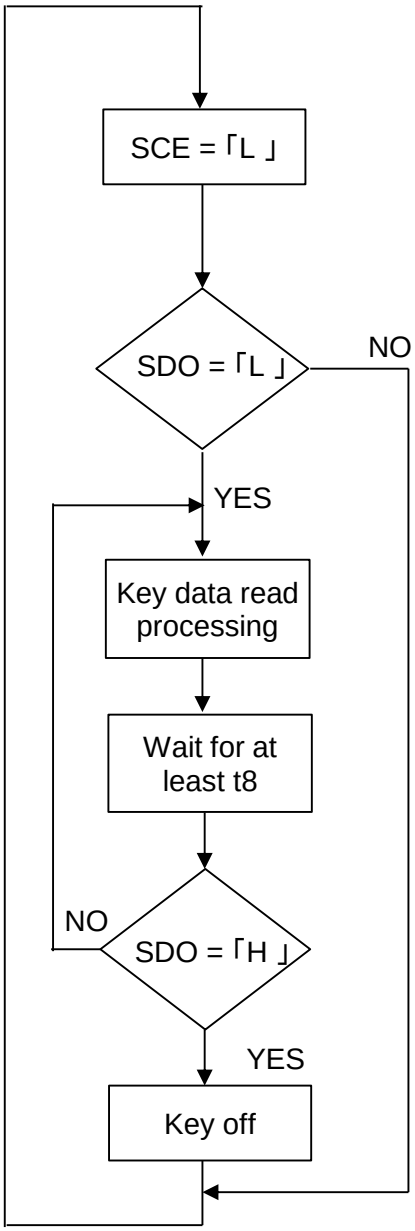
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Key Scan Operation Functions – continued

7. Interrupt Based Key Data Acquisition Technique

Under the Interrupt Based Key Data Acquisition Technique, the controller uses interrupts to determine the state of the keys (on or off) and read the key data. Please refer to the flow chart diagram below.



Key data read processing: Refer to “Serial Data Output”

Figure 26. Flowchart

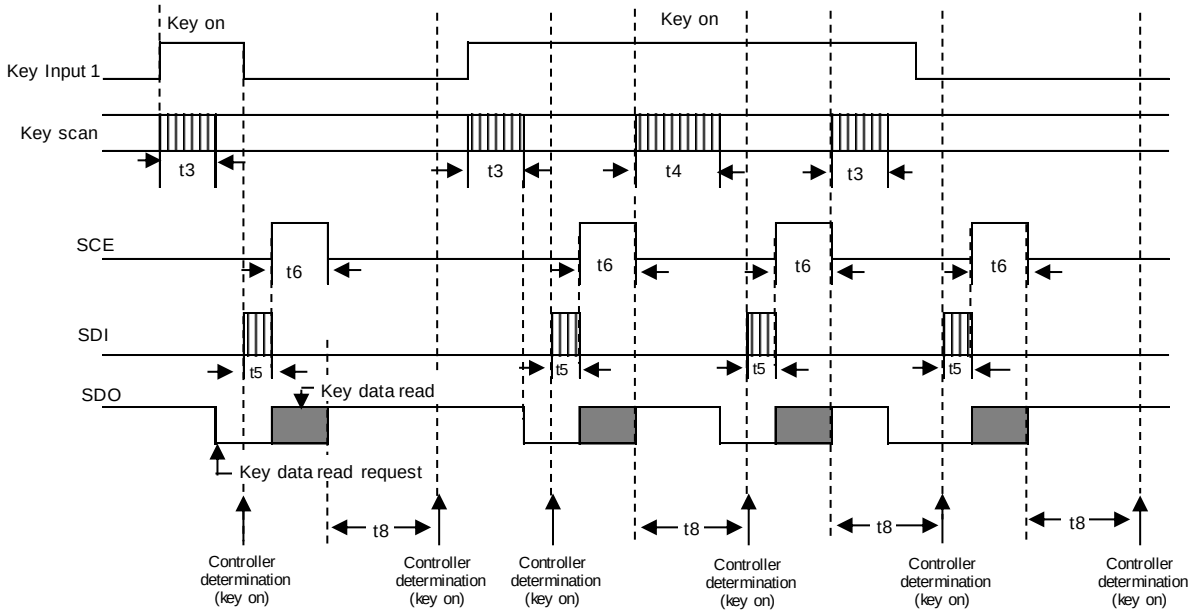
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Key Scan Operation Functions – continued

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the SDO state when SCE is low and reading the key data. The period t8 in this technique must satisfy t8 > t4.

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and power-saving acknowledge data (PA) will be invalid.



t3: Key scan execution time when the key data agreed for two key scans. (9840T[s])
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (19680T[s]) T = 1 / fosc
t5: Key address (43H) transfer time
t6: Key data read time

Figure 27. Interrupt Based Key Data Read Operation

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LCD Driving Waveforms

1. Line Inversion 1/8-Duty 1/4-Bias Drive Scheme

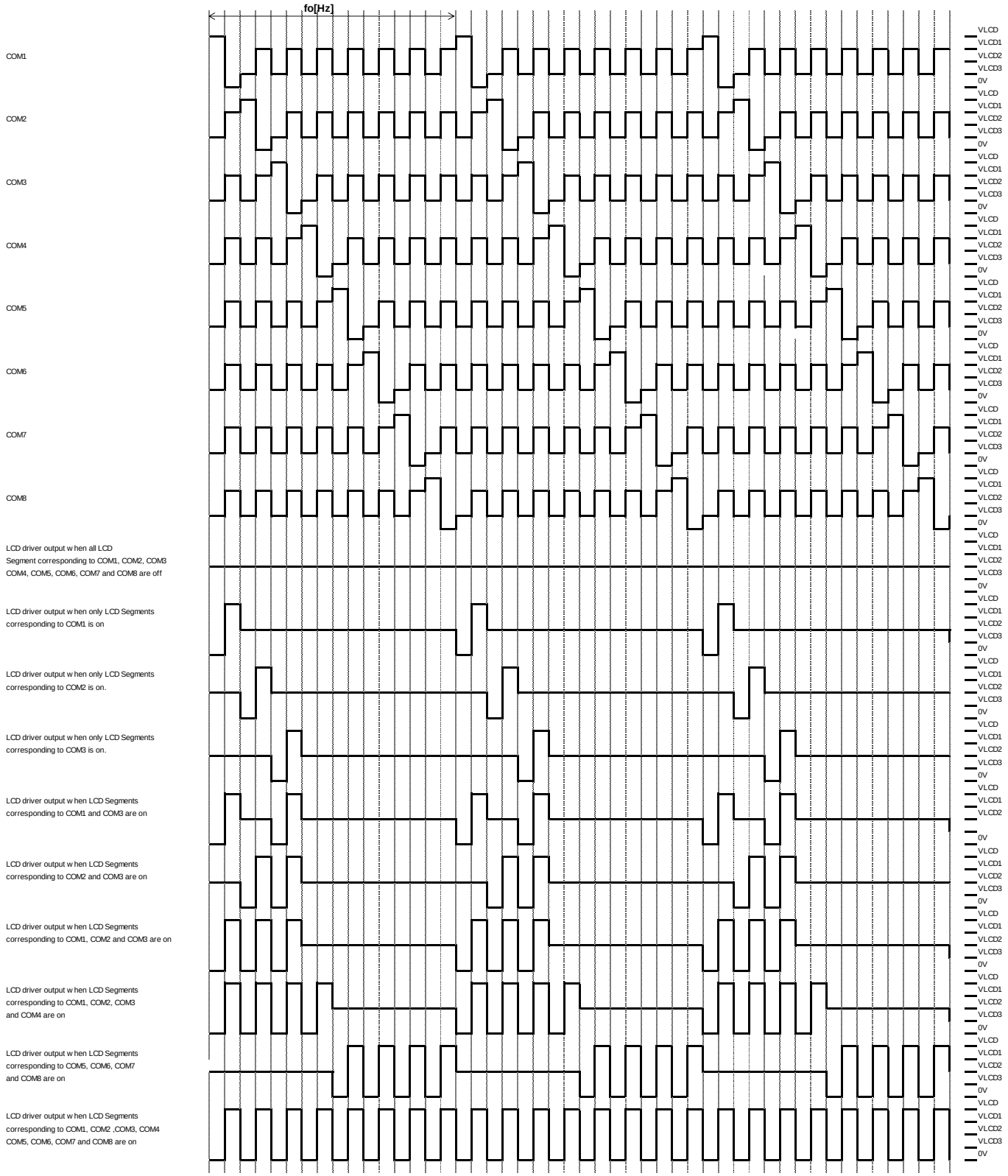


Figure 28. LCD Waveform (Line Inversion, 1/8 DUTY, 1/4 BIAS)

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LCD Driving Waveforms – continued

2. Line Inversion 1/8-Duty 1/3-Bias Drive Scheme

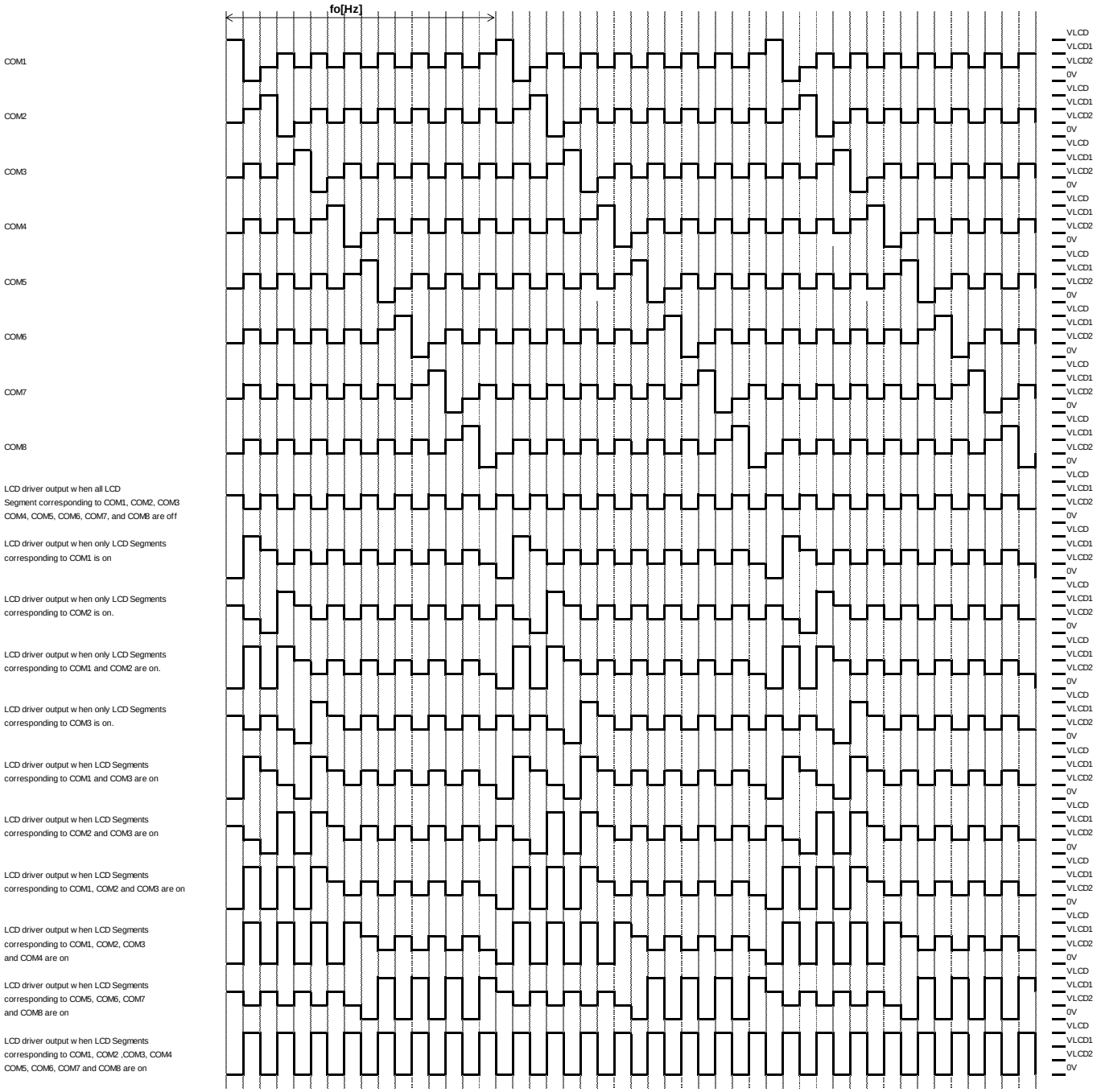


Figure 29. LCD Waveform (Line Inversion, 1/8 DUTY, 1/3 BIAS)

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LCD Driving Waveforms – continued

3. Line Inversion 1/8-Duty 1/2-Bias Drive Scheme

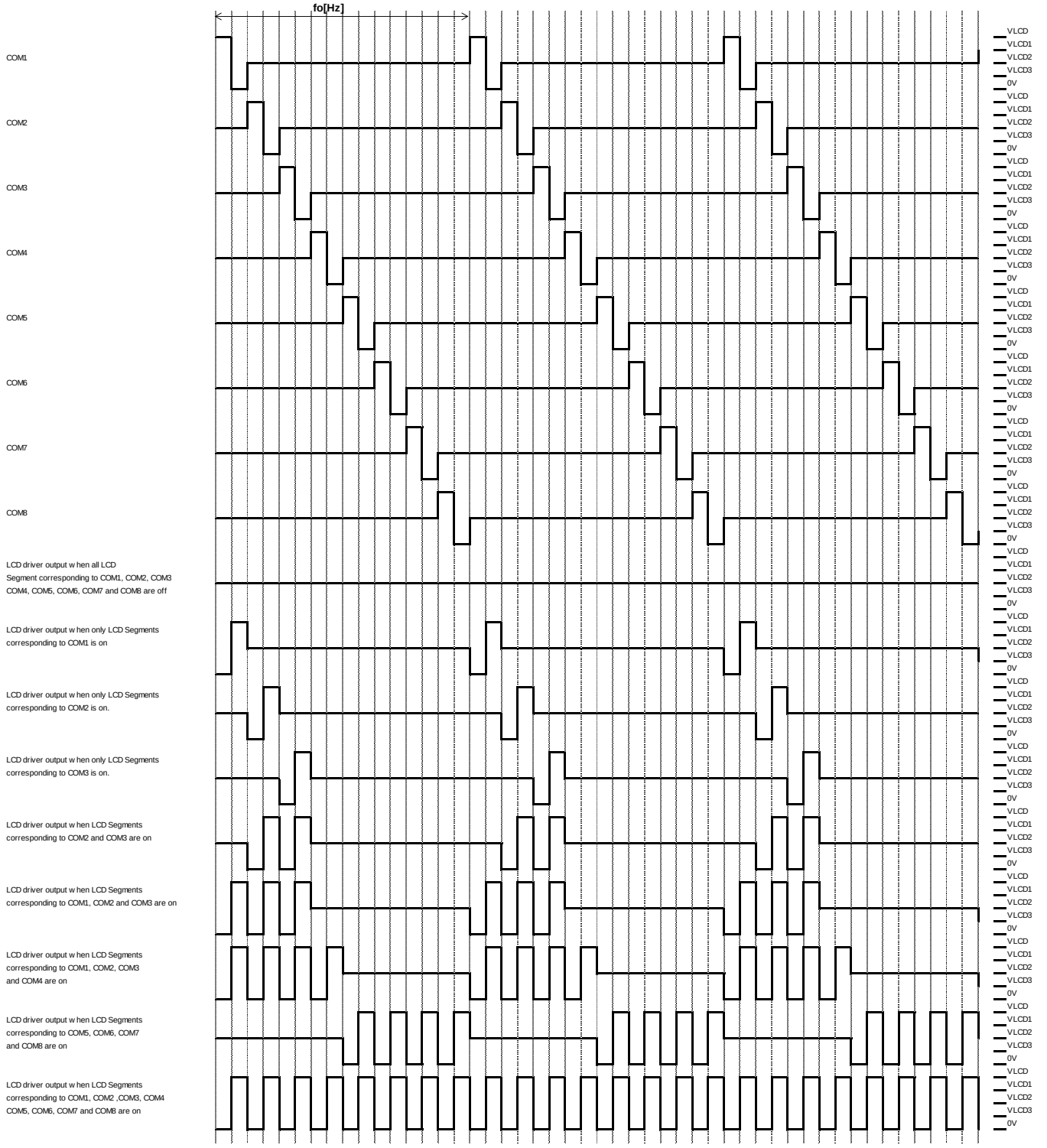


Figure 30. LCD Waveform (Line Inversion, 1/8 DUTY, 1/2 BIAS)

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LCD Driving Waveforms – continued

4. Line Inversion 1/7-Duty 1/4-Bias Drive Scheme

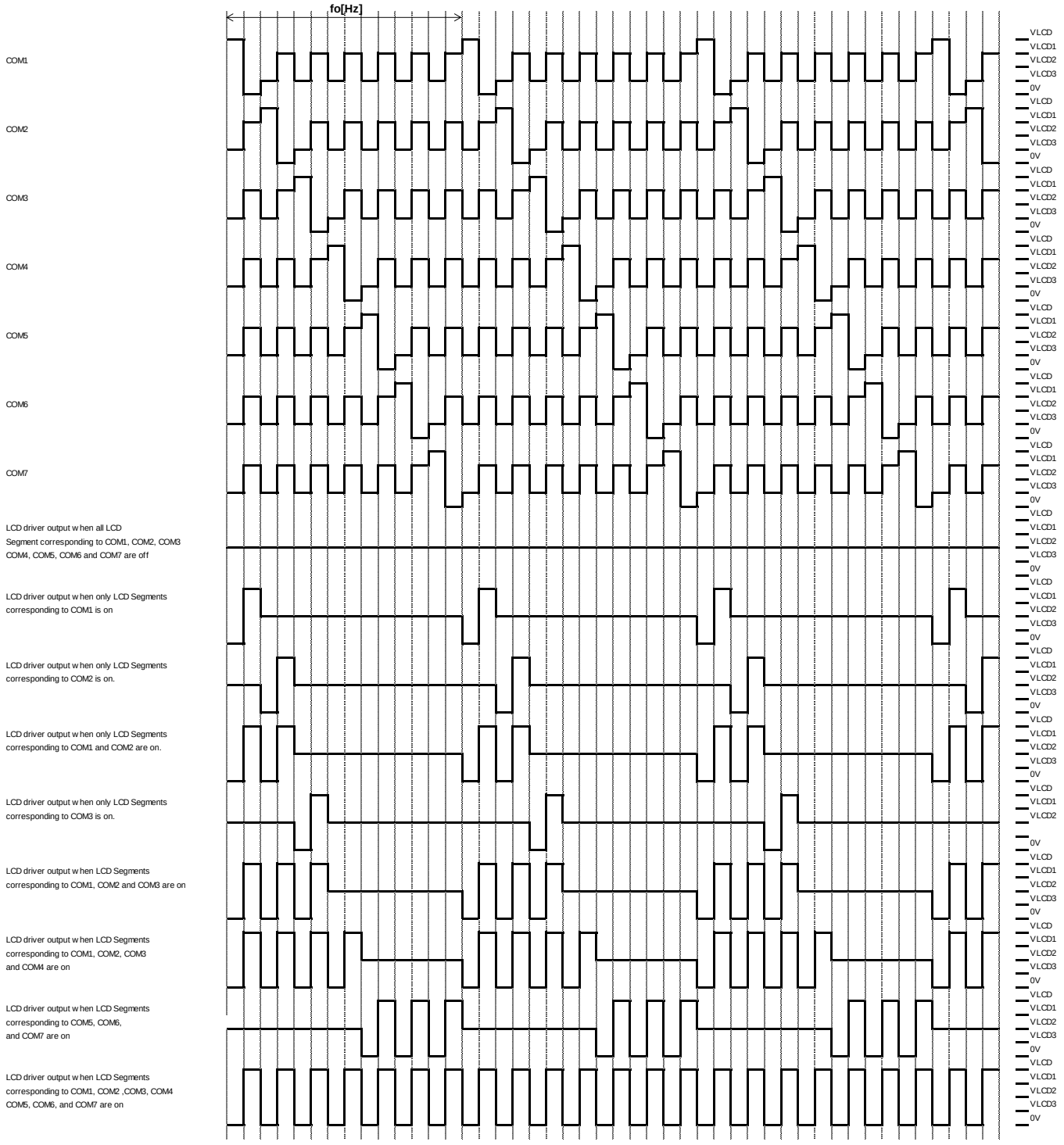


Figure 31. LCD Waveform (Line Inversion, 1/7 DUTY, 1/4 BIAS)

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LCD Driving Waveforms – continued

5. Line Inversion 1/5-Duty 1/3-Bias Drive Scheme

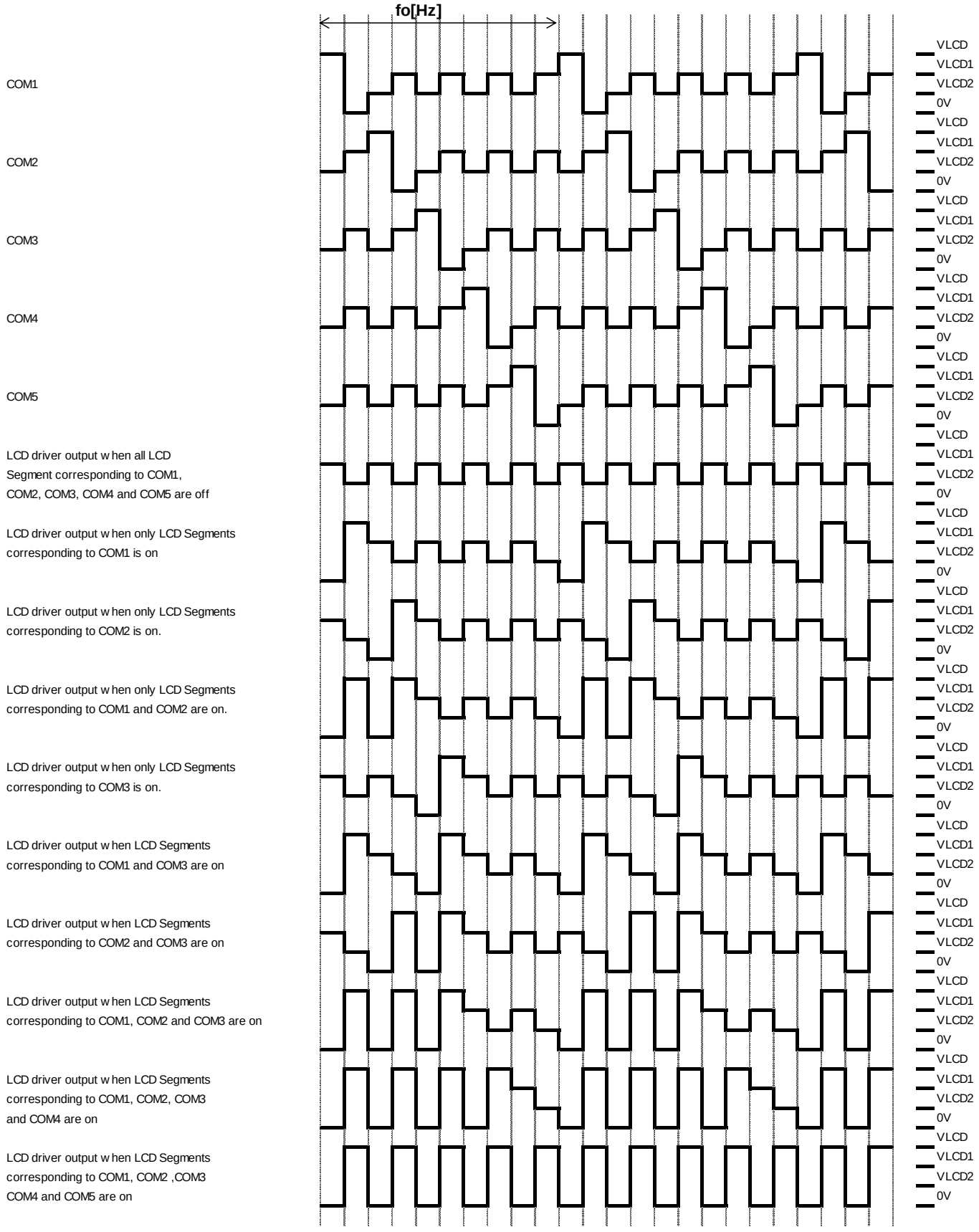


Figure 32. LCD Waveform (Line Inversion, 1/5 DUTY, 1/3 BIAS)

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LCD Driving Waveforms – continued

6. Line Inversion 1/5-Duty 1/2-Bias Drive Scheme

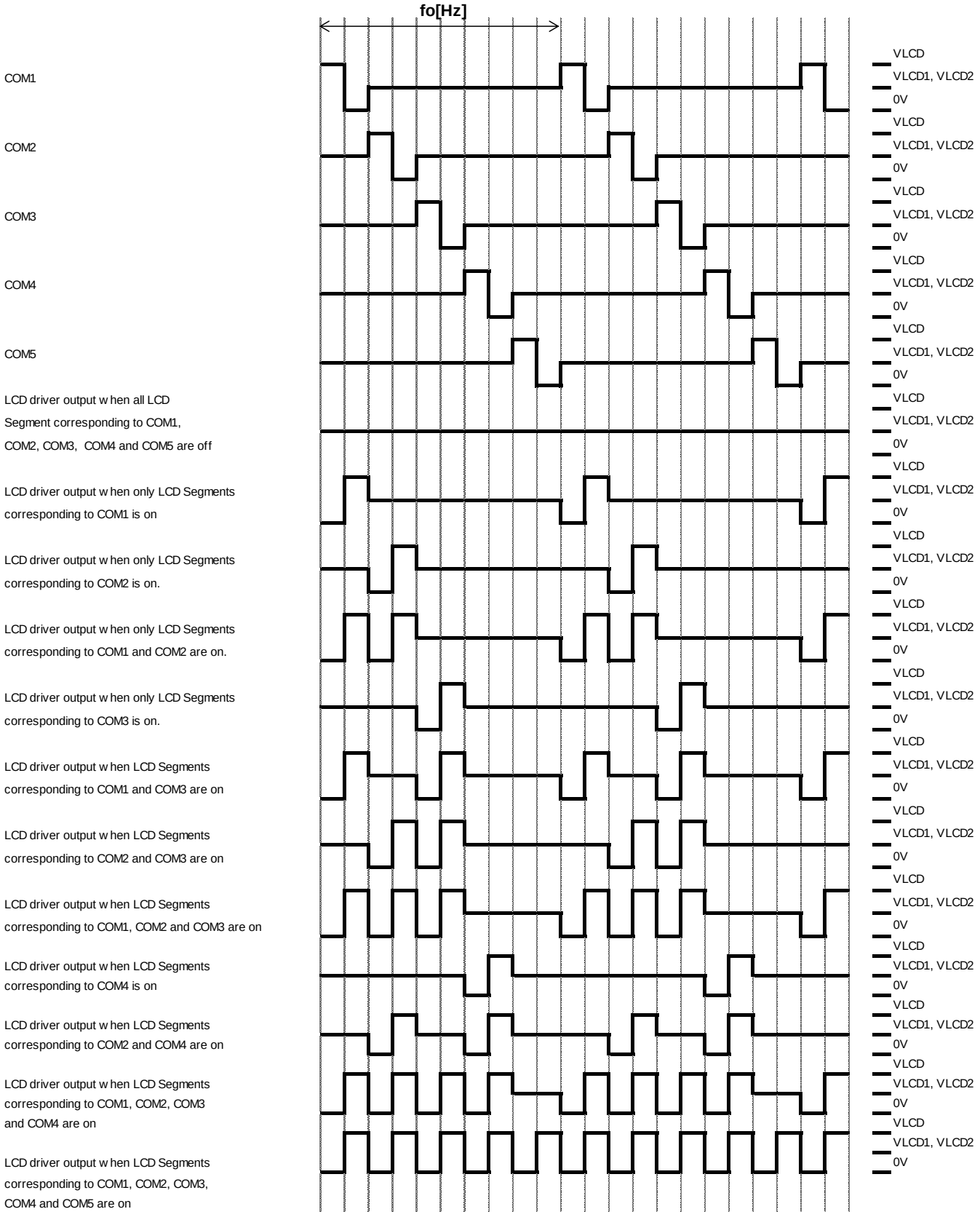


Figure 33. LCD Waveform (Line Inversion, 1/5 DUTY, 1/2 BIAS)

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LCD Driving Waveforms – continued

7. Line Inversion 1/4-Duty 1/3-Bias Drive Scheme

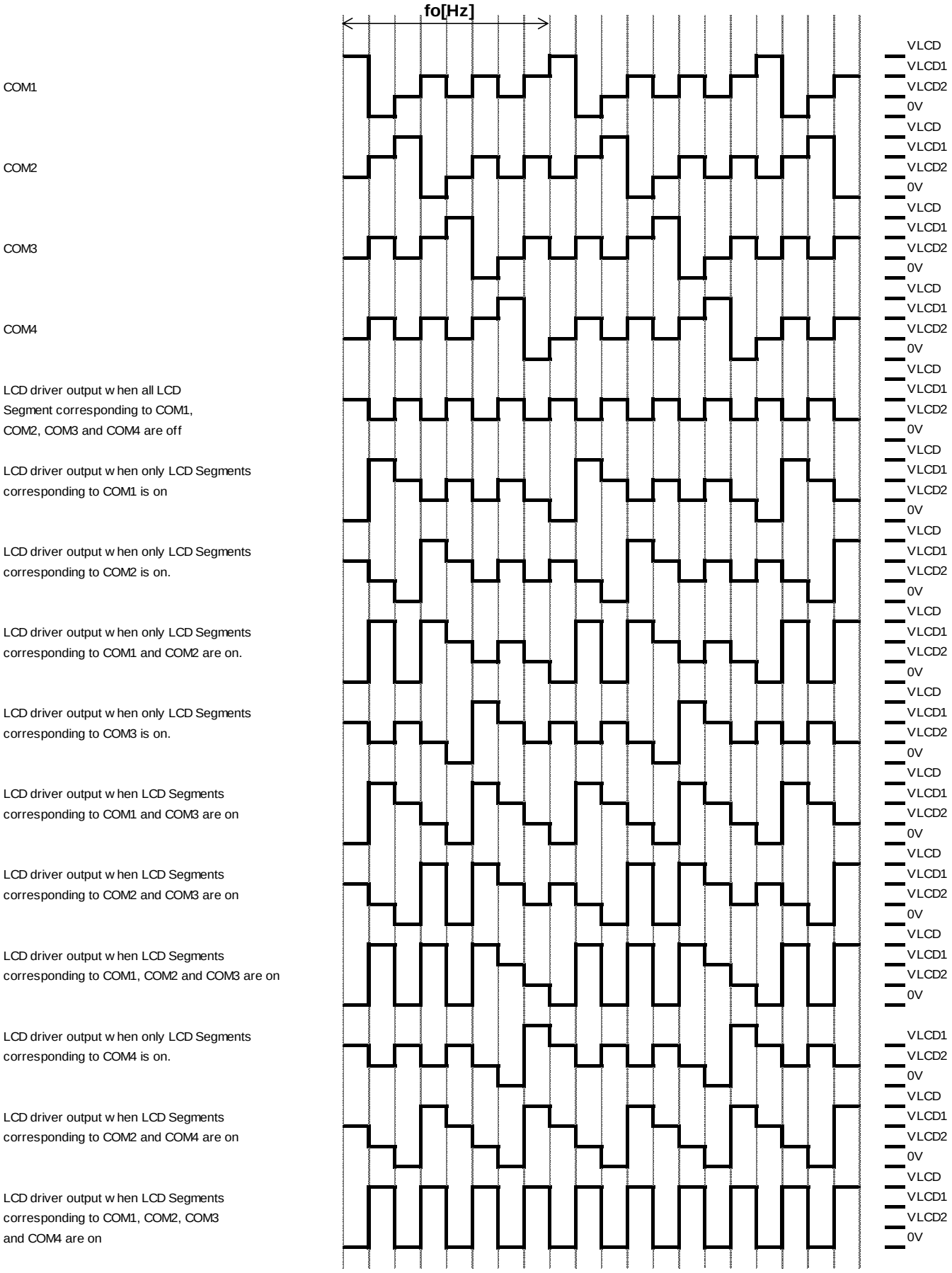


Figure 34. LCD Waveform (Line Inversion, 1/4 DUTY, 1/3 BIAS)

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LCD Driving Waveforms – continued

8. Line Inversion 1/4-Duty 1/2-Bias Drive Scheme

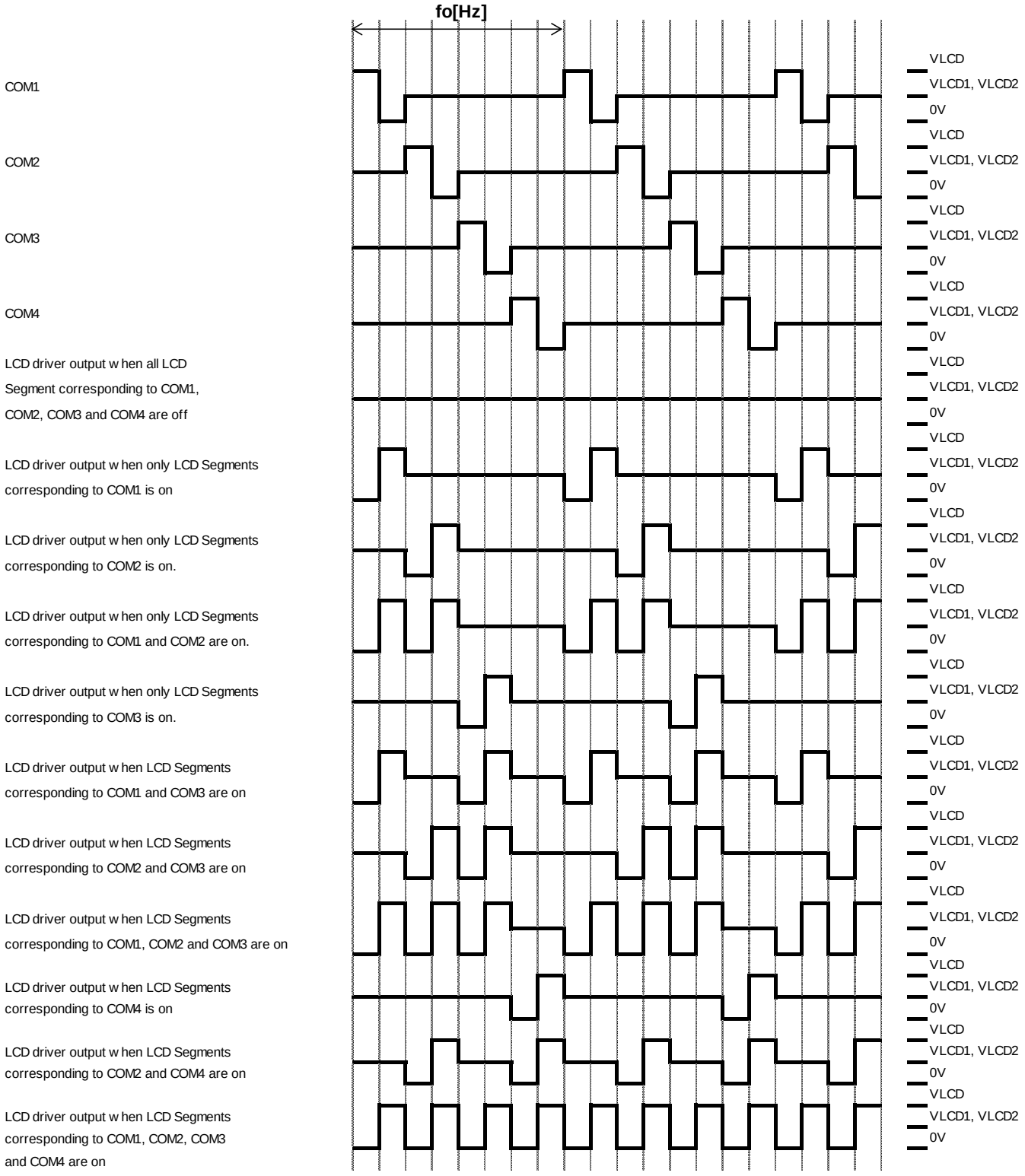


Figure 35. LCD Waveform (Line Inversion, 1/4 DUTY, 1/2 BIAS)

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LCD Driving Waveforms – continued

9. Line Inversion 1/3-Duty 1/3-Bias Drive Scheme

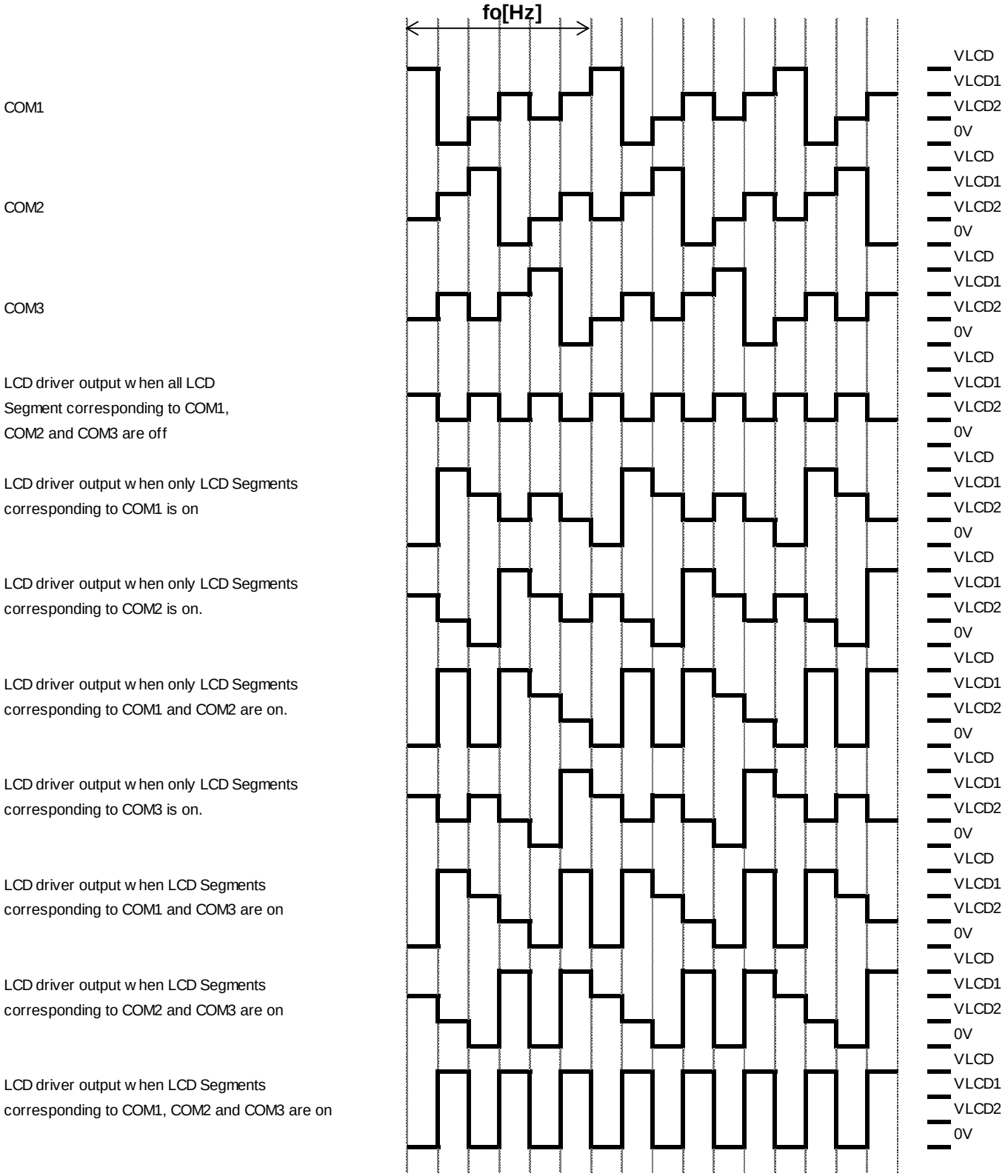


Figure 36. LCD Waveform (Line Inversion, 1/3 DUTY, 1/3 BIAS) (Note30)

(Note30) COM4 function is same as COM1 at 1/3 duty.

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LCD Driving Waveforms – continued

10. Line Inversion 1/3-Duty 1/2-Bias Drive Scheme

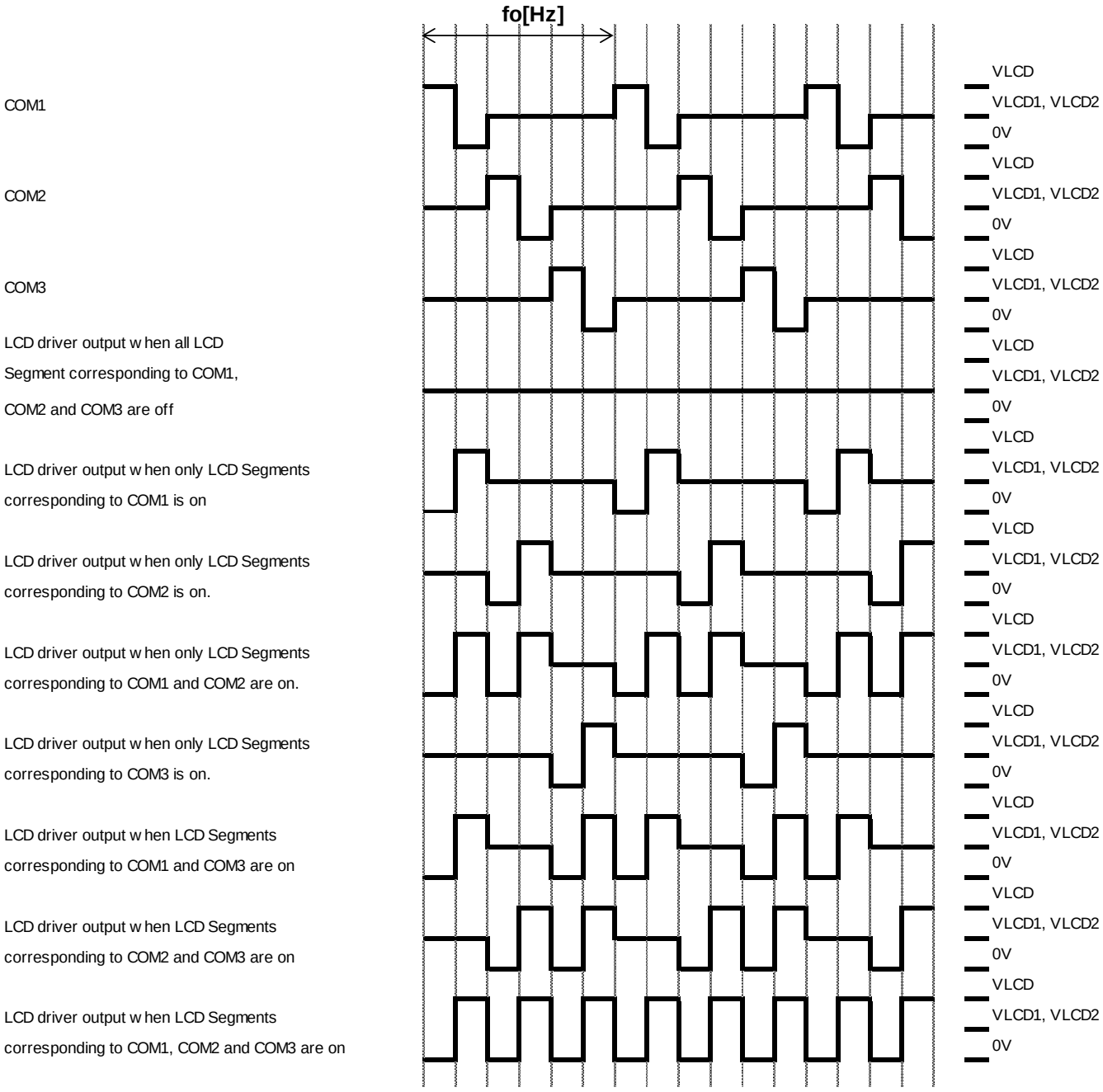


Figure 37. LCD Waveform (Line Inversion, 1/3 DUTY, 1/2 BIAS) (Note31)

(Note31) COM4 function is same as COM1 at 1/3 duty.

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LCD Driving Waveforms – continued

11. Line Inversion Static Drive Scheme

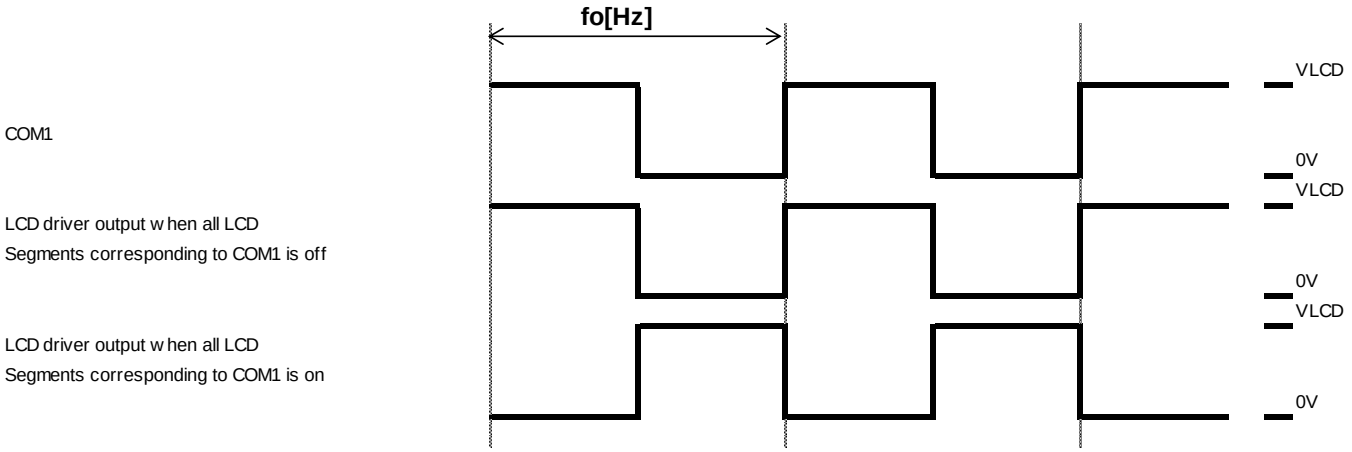


Figure 38. LCD Waveform (Line Inversion, Static) (Note32)

(Note32) COM2, COM3 and COM4 function are same as COM1 at Static.

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LCD Driving Waveforms – continued

12. Frame Inversion, 1/8-Duty 1/4-Bias Drive Scheme

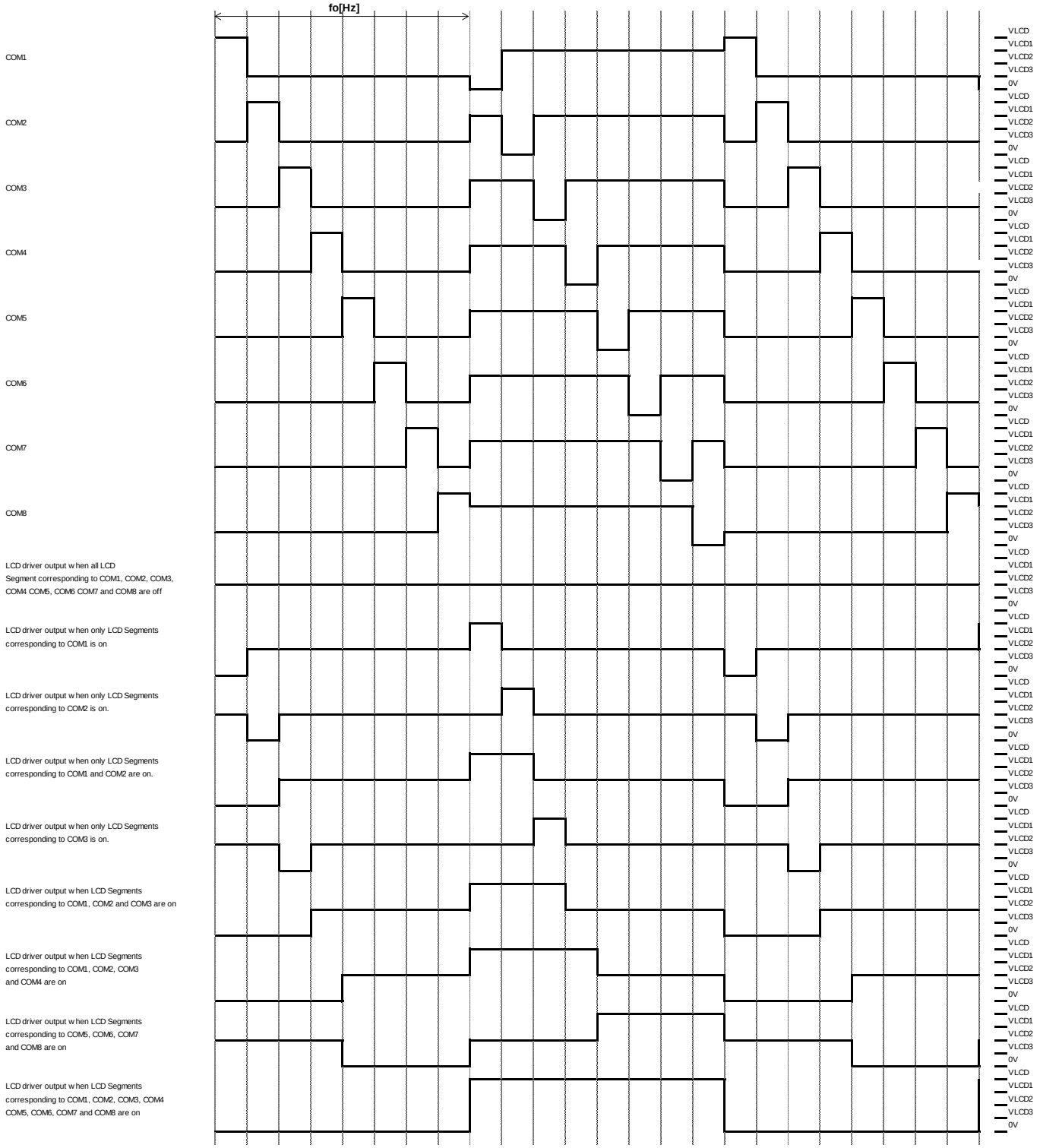


Figure 39. LCD Waveform (Frame Inversion, 1/8 DUTY, 1/4BIAS)

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LCD Driving Waveforms – continued

13. Frame Inversion 1/5-Duty 1/3-Bias Drive Scheme

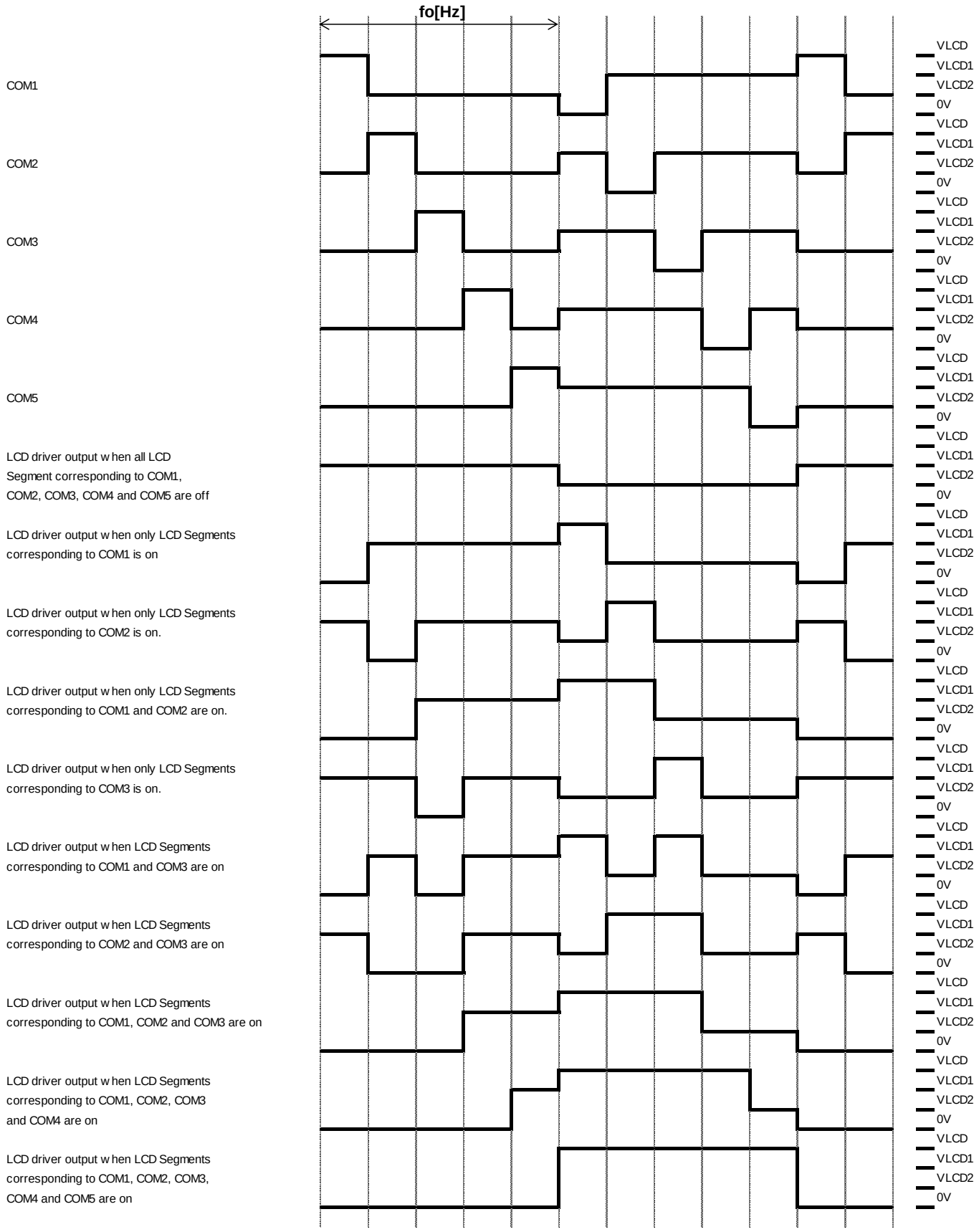


Figure 40. LCD Waveform (Frame Inversion, 1/5 DUTY, 1/3BIAS)

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LCD Driving Waveforms – continued

14. Frame Inversion 1/5-Duty 1/2-Bias Drive Scheme

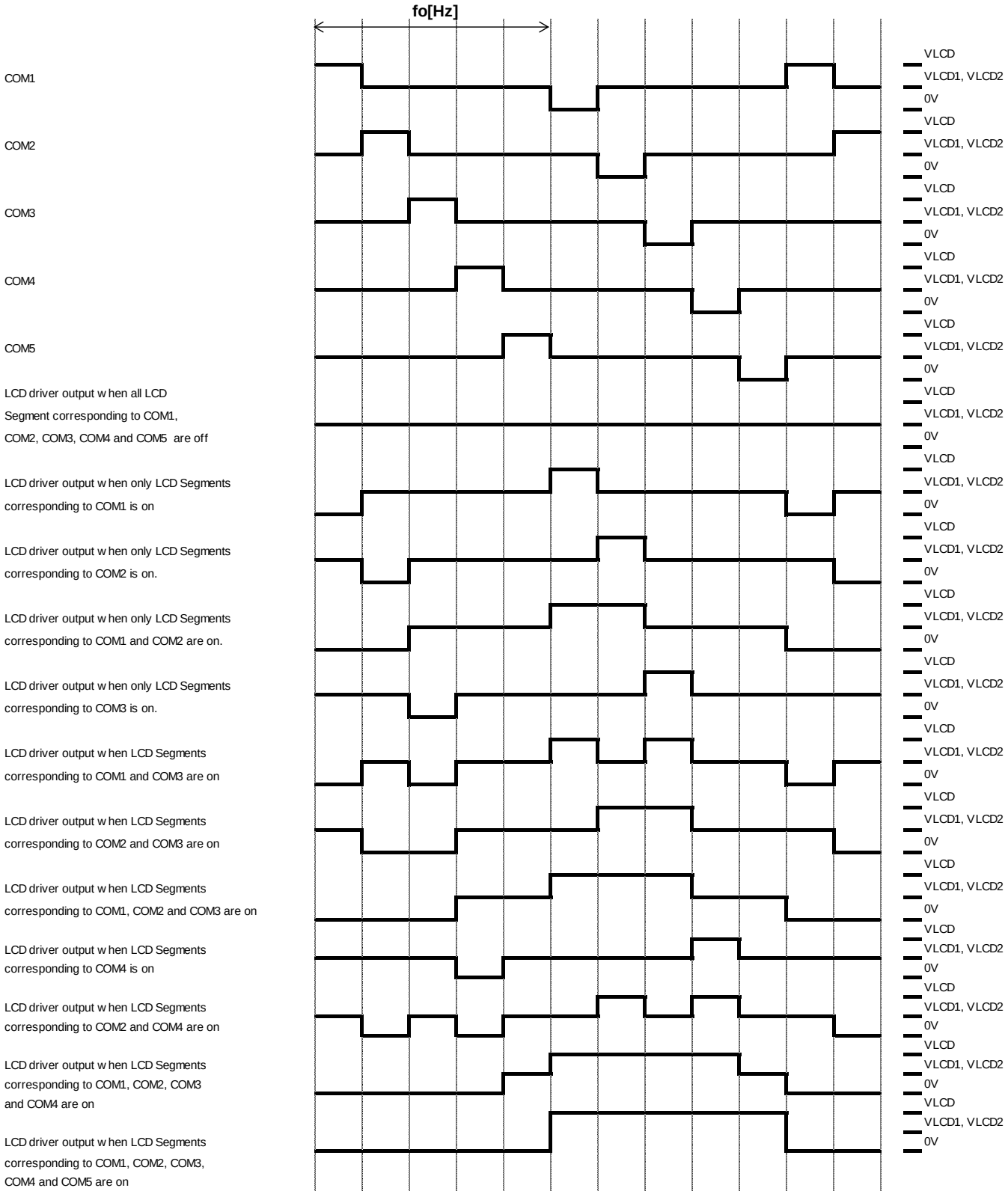


Figure 41. LCD Waveform (Frame Inversion, 1/5 DUTY, 1/2BIAS)

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LCD Driving Waveforms – continued

15. Frame Inversion 1/4-Duty 1/3-Bias Drive Scheme

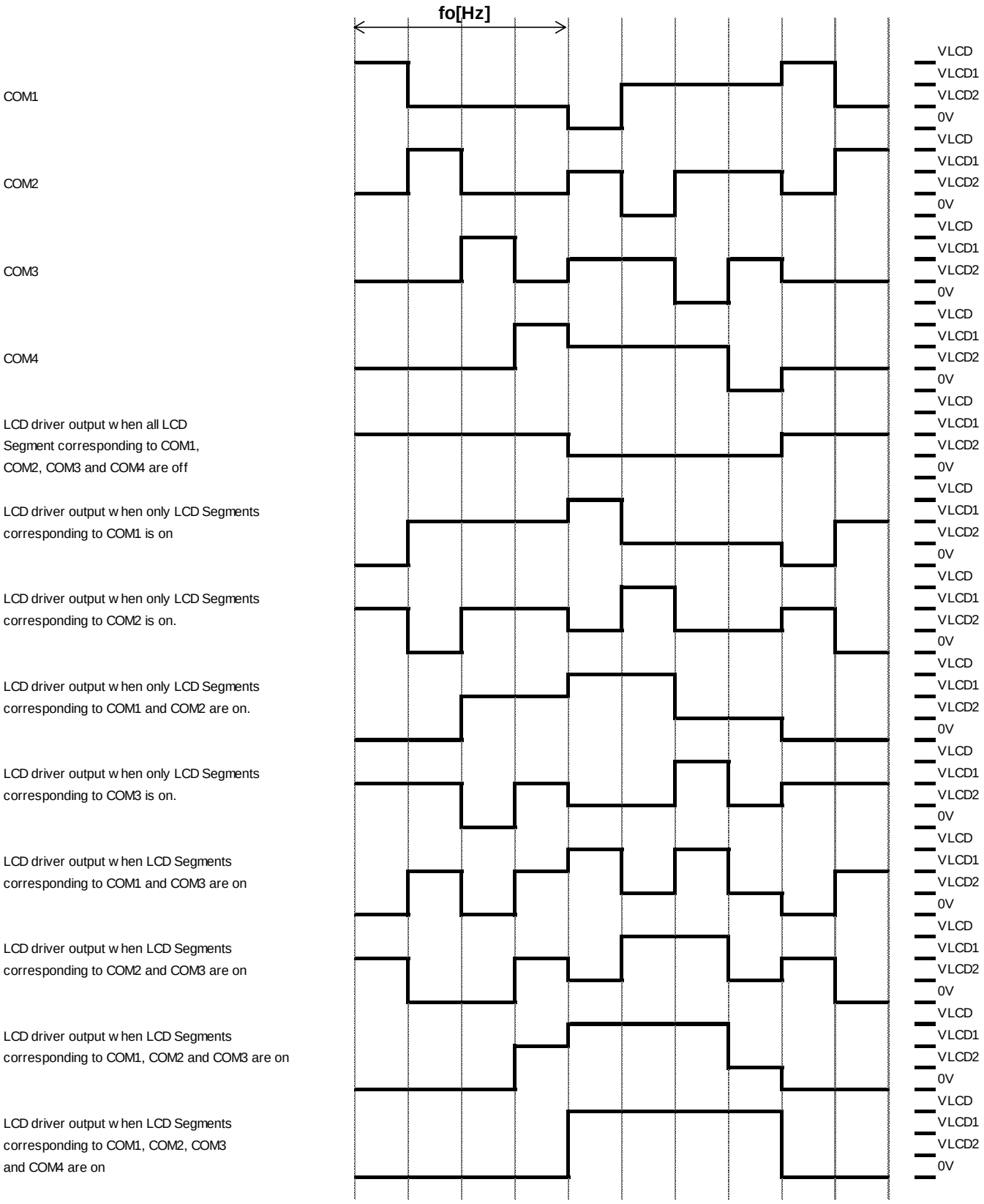


Figure 42. LCD Waveform (Frame Inversion, 1/4 DUTY, 1/3BIAS)

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LCD Driving Waveforms – continued

16. Frame Inversion 1/4-Duty 1/2-Bias Drive Scheme

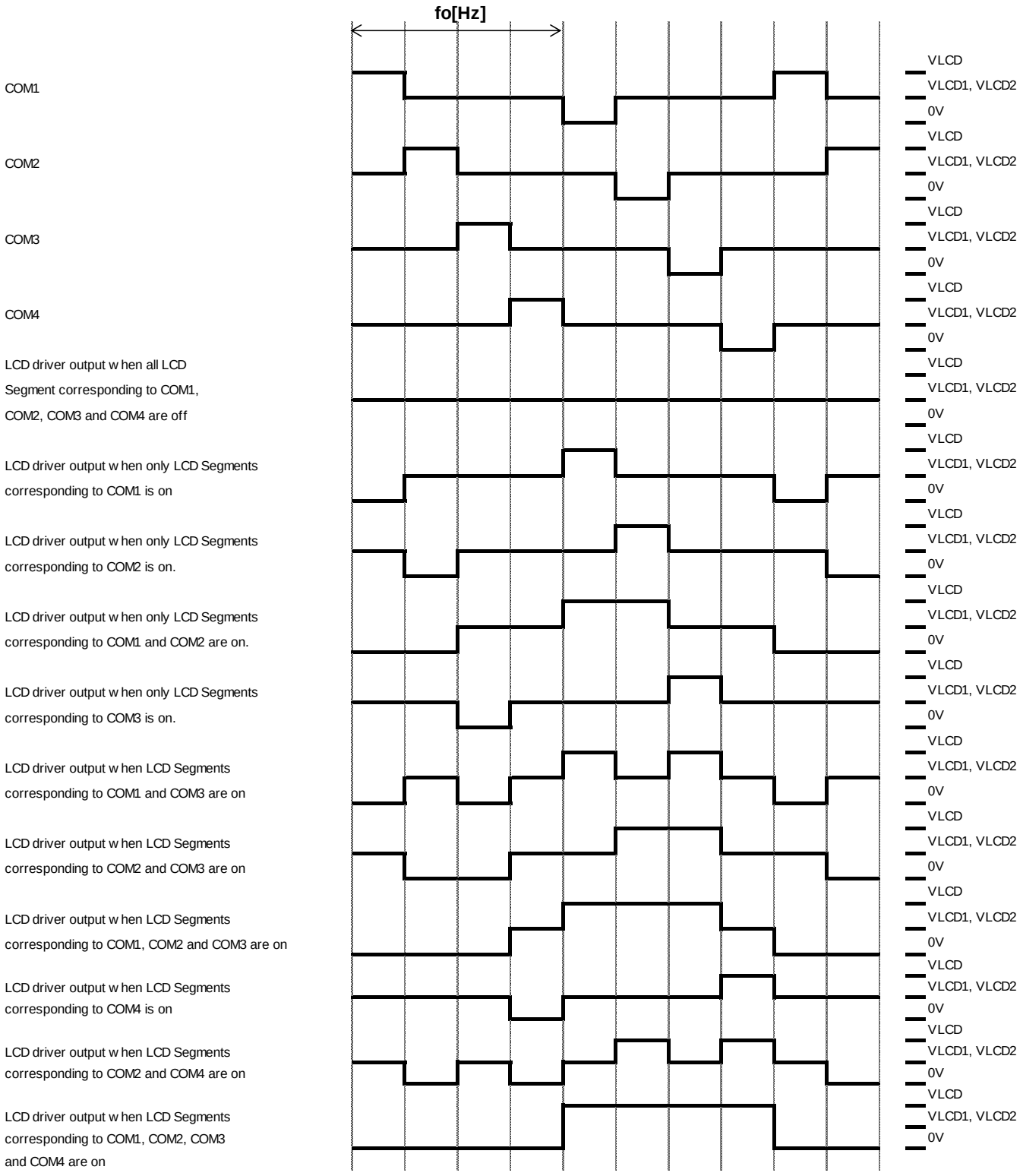


Figure 43. LCD Waveform (Frame Inversion, 1/4 DUTY, 1/2BIAS)

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LCD Driving Waveforms – continued

17. Frame Inversion 1/3-Duty 1/3-Bias Drive Scheme

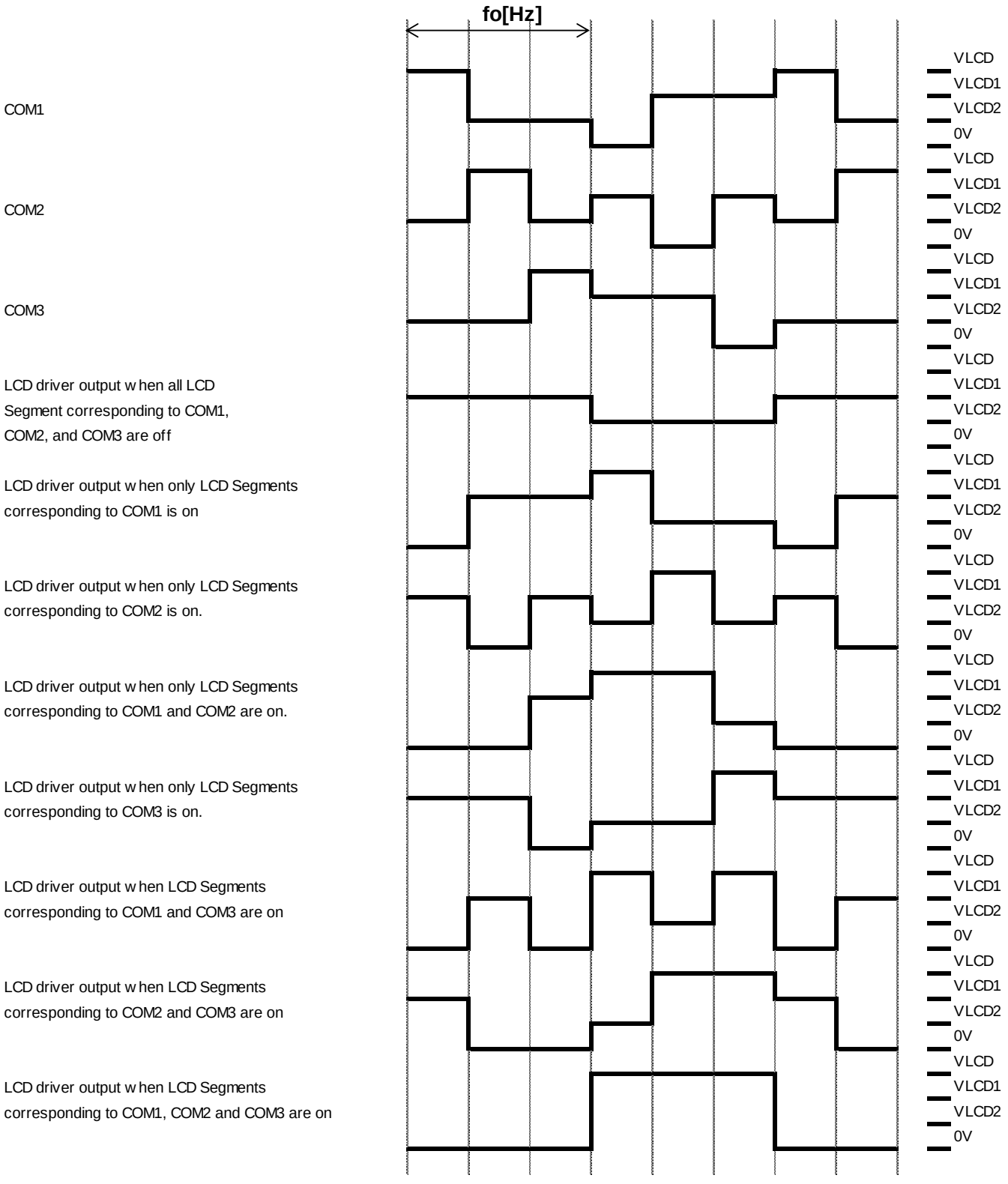


Figure 44. LCD Waveform (Frame Inversion, 1/3 DUTY, 1/3BIAS) (Note33)

(Note33) COM4 function is same as COM1 at 1/3 duty.

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LCD Driving Waveforms – continued

18. Frame Inversion 1/3-Duty 1/2-Bias Drive Scheme

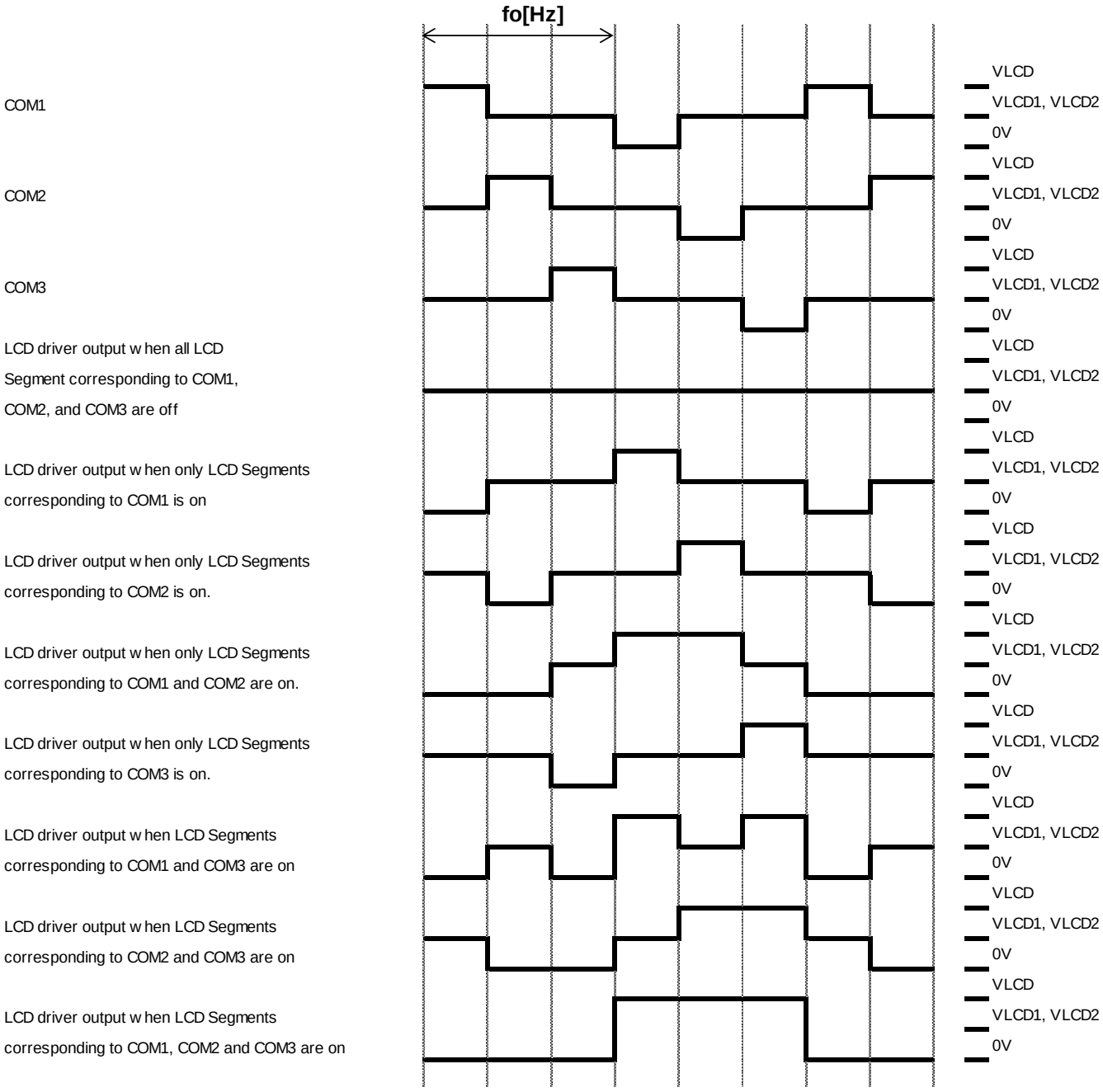


Figure 45. LCD Waveform (Frame Inversion, 1/3 DUTY, 1/2 BIAS) (Note34)

(Note34) COM4 function is same as COM1 at 1/3 duty.

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LCD Driving Waveforms – continued

19. Frame Inversion Static Drive Scheme

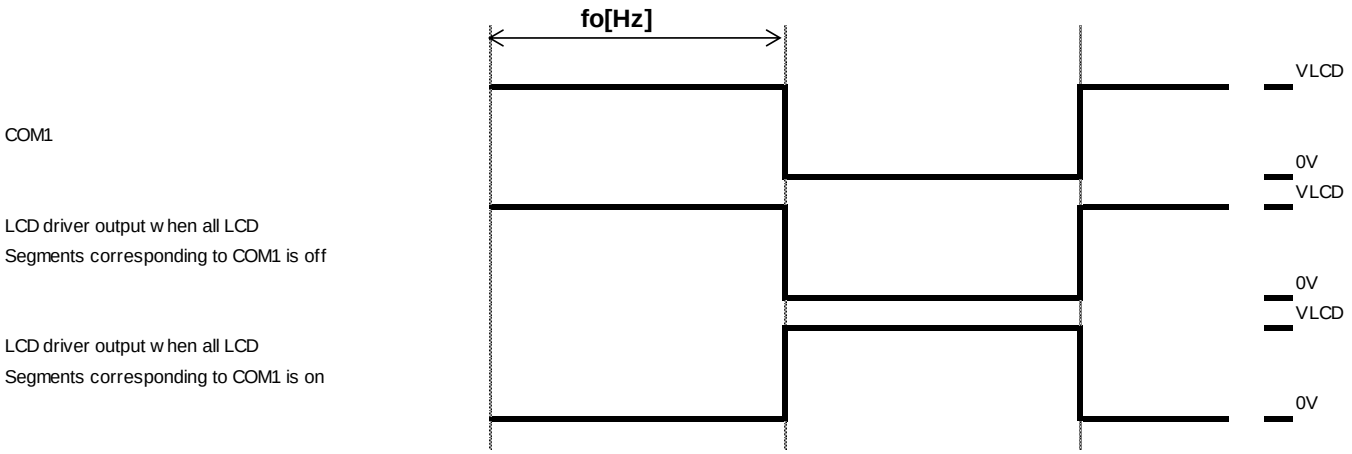


Figure 46. LCD Waveform (Frame Inversion, Static) (Note35)

(Note35) COM2, COM3 and COM4 function are same as COM1 at Static.

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Oscillation Stabilization Time of the Internal Oscillation Circuit

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100μs (oscillation stabilization time) after oscillation has started.

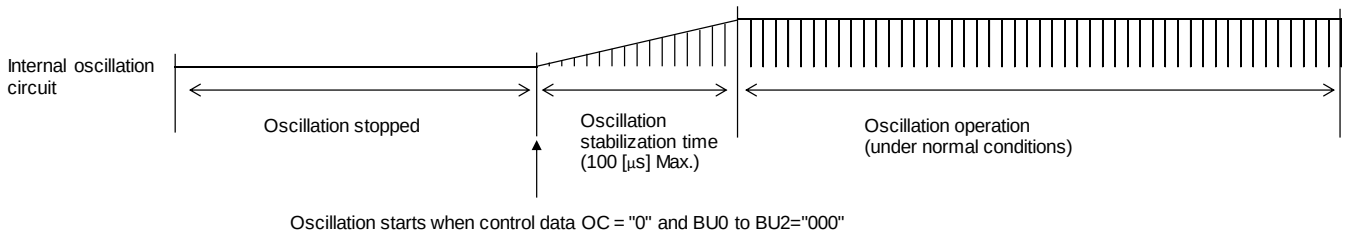


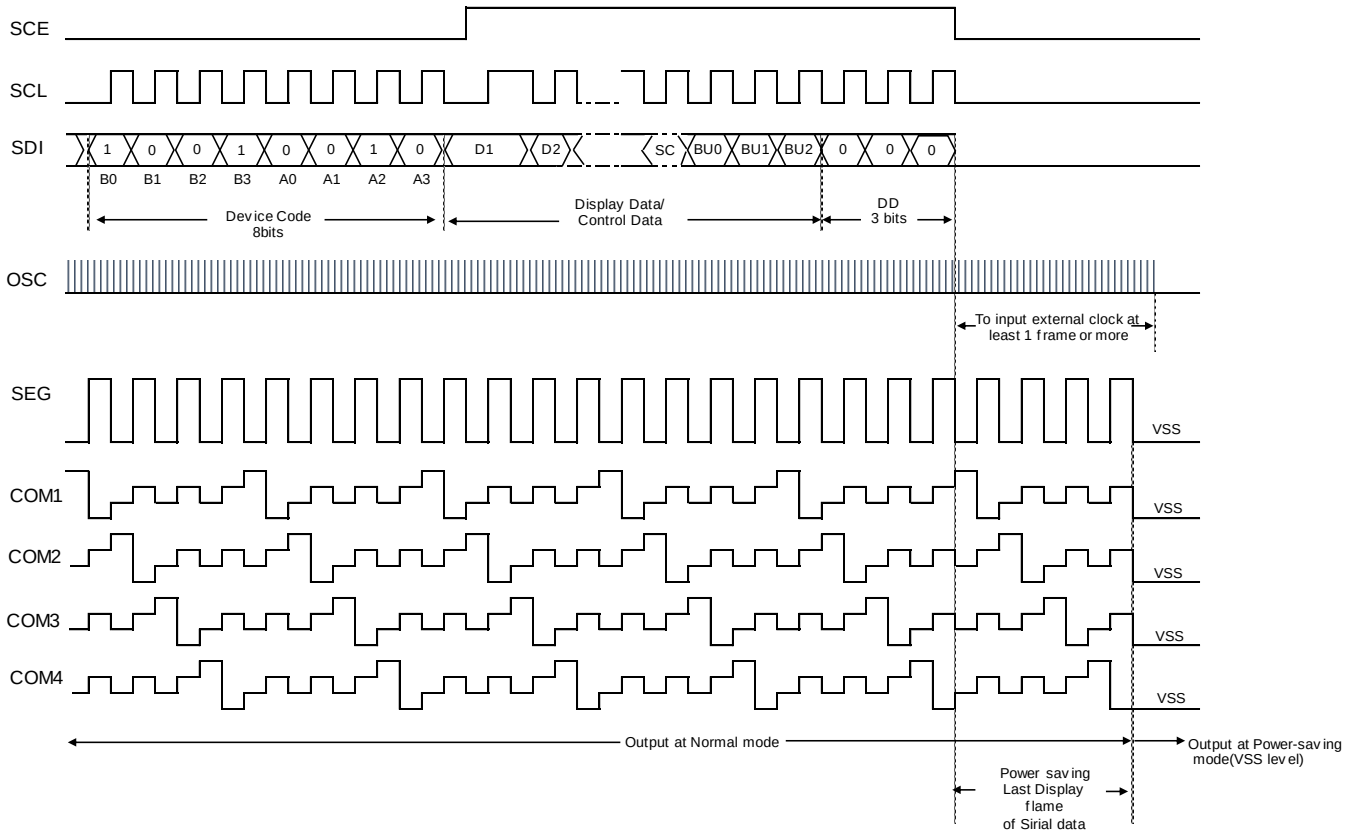
Figure 47. Oscillation Stabilization Time

Power-saving mode operation in external clock mode

After receiving [BU0,BU1,BU2]=[1,1,1], BU97550KV-M enter to Power-saving mode synchronized with frame then Segment and Common ports output VSS level.
Therefore, in external clock mode, it is necessary to input the external clock based on each frame frequency setting after sending [BU0,BU1,BU2]=[1,1,1].
For the required number of clock, refer to “Control Data Functions 6. FC0, FC1, FC2 and FC3”.

For example, please input the external clock as below.
[FC0,FC1,FC2,FC3]=[0,0,0,0]: In case of fosc/12288 setting, it needs over 12288clk,
[FC0,FC1,FC2,FC3]=[0,1,0,1]: In case of fosc/4608 setting, it needs over 4608clk,
[FC0,FC1,FC2,FC3]=[1,1,1,1]: In case of fosc/1536 setting, it needs over 1536clk

Please refer to the timing chart below.



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Voltage Detection Type Reset Circuit (VDET)

The Voltage Detection Type Reset Circuit generates an output signal that resets the system when power is applied for the first time and when the power supply voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage (V_{DET} = 1.8V Typ). To ensure that this reset function works properly, it is recommended that a capacitor be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

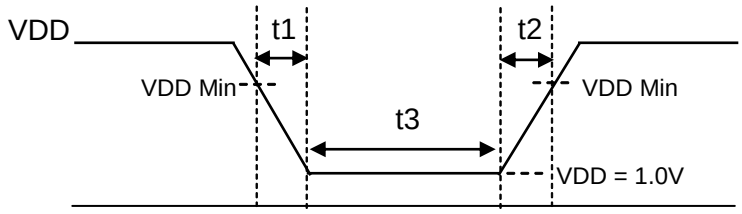
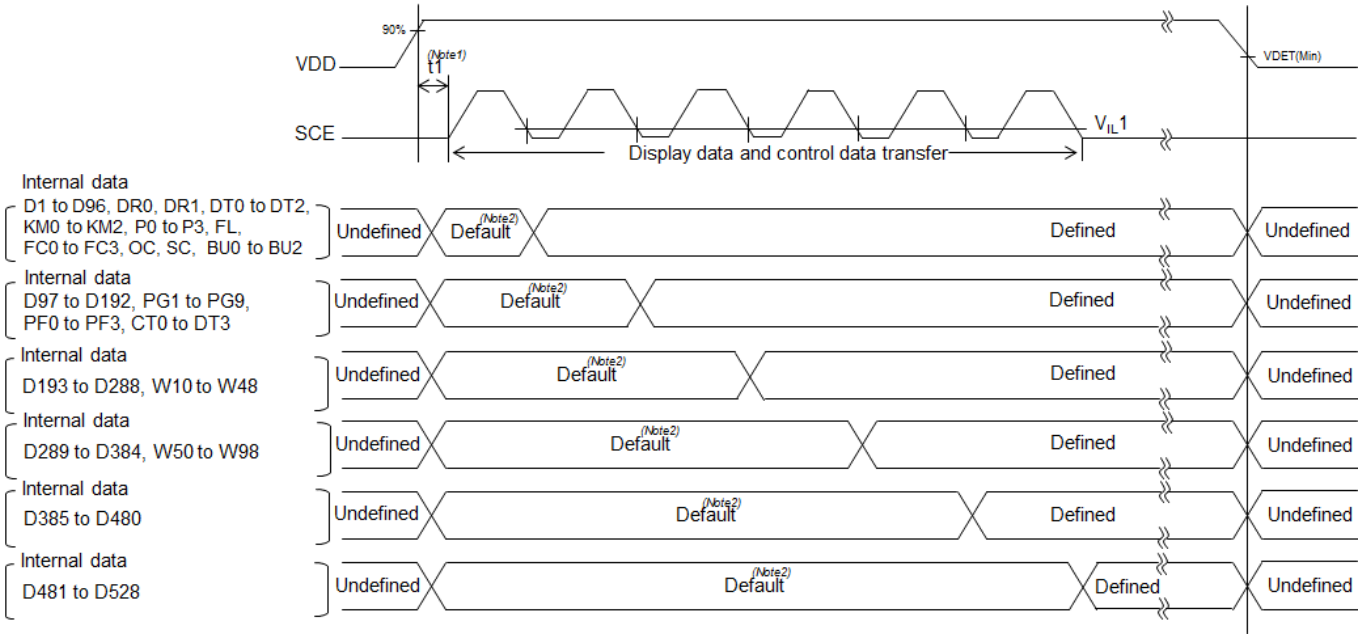


Figure 48. V_{DET} Detection Timing

Power supply voltage VDD fall time: t1 > 1ms
Power supply voltage VDD rise time: t2 > 1ms
Internal reset power supply retain time: t3 > 1ms

When it is difficult to keep above conditions, it is possibility to cause meaningless display due to no IC initialization.
Please execute the IC initialization as quickly as possible after Power-On to reduce such an affect.
See the IC initialization flow as below.
But since commands are not received when the power is OFF, the IC initialization flow is not the same function as VDET.

Set [BU0,BU1,BU2]=[1,1,1](power-saving mode) and SC=1(Display Off) as quickly as possible after Power-On.
BU97550KV-M can receive commands in 0ns after Power-On(VDD level is 90%).



(Note1) t1≥0, t2≥0, tc: Min 10µs
When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.
(Note2) Display data are undefined. Regarding default value, refer to Reset Condition.

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Reset Condition

When BU97550KV-M is initialized, the internal status after power supply has been reset as the following table.

Instruction	At Reset Condition
Key Scan Mode	[KM0,KM1,KM2]=[1,1,1]:Key scan no use
S1/P1/G1 to S9/P9/G9 Pin	[P0,P1,P2,P3]=[0,0,0,0]:all Segment output
Inversion Mode	FL=0:Line Inversion
LCD Bias	[DR0,DR1]=[0,0]:1/3 bias
LCD Duty	[DT0,DT1,DT2]=[0,1,0]:1/4 duty
DISPLAY Frequency	[FC0,FC1,FC2,FC3]=[0,0,0,0]:fosc/12288
Display Clock Mode	OC=0:Internal oscillator
LCD Display	SC=1:OFF
Power Mode	[BU0,BU1,BU2]=[1,1,1]:Power saving mode
PWM/GPO output	PGx=0:PWM output(x=1 to 9)
PWM Frequency	[PF0,PF1,PF2,PF3]=[0,0,0,0]: fosc /4096
PWM Duty	[Wn0 to Wn8]=[0,0,0,0,0,0,0,0,0]:0/256)xTp (n=1 to 9,Tp=1/fp)
Display Contrast Setting	[CT0,CT1,CT2,CT3]=[0,0,0,0]:VLCD Level is 1.00*VDD

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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Ordering Information

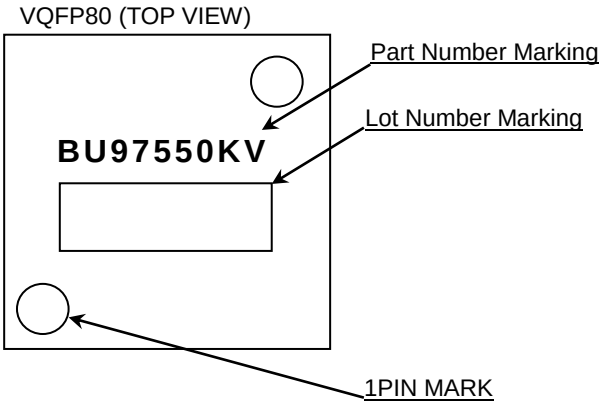
B U 9 7 5 5 0 K V - M E 2

Part Number

Package
KV : VQFP80

Product Rank
M: for Automotive
Packaging Specification
E2: Embossed tape and reel
(VQFP80)

Marking Diagram

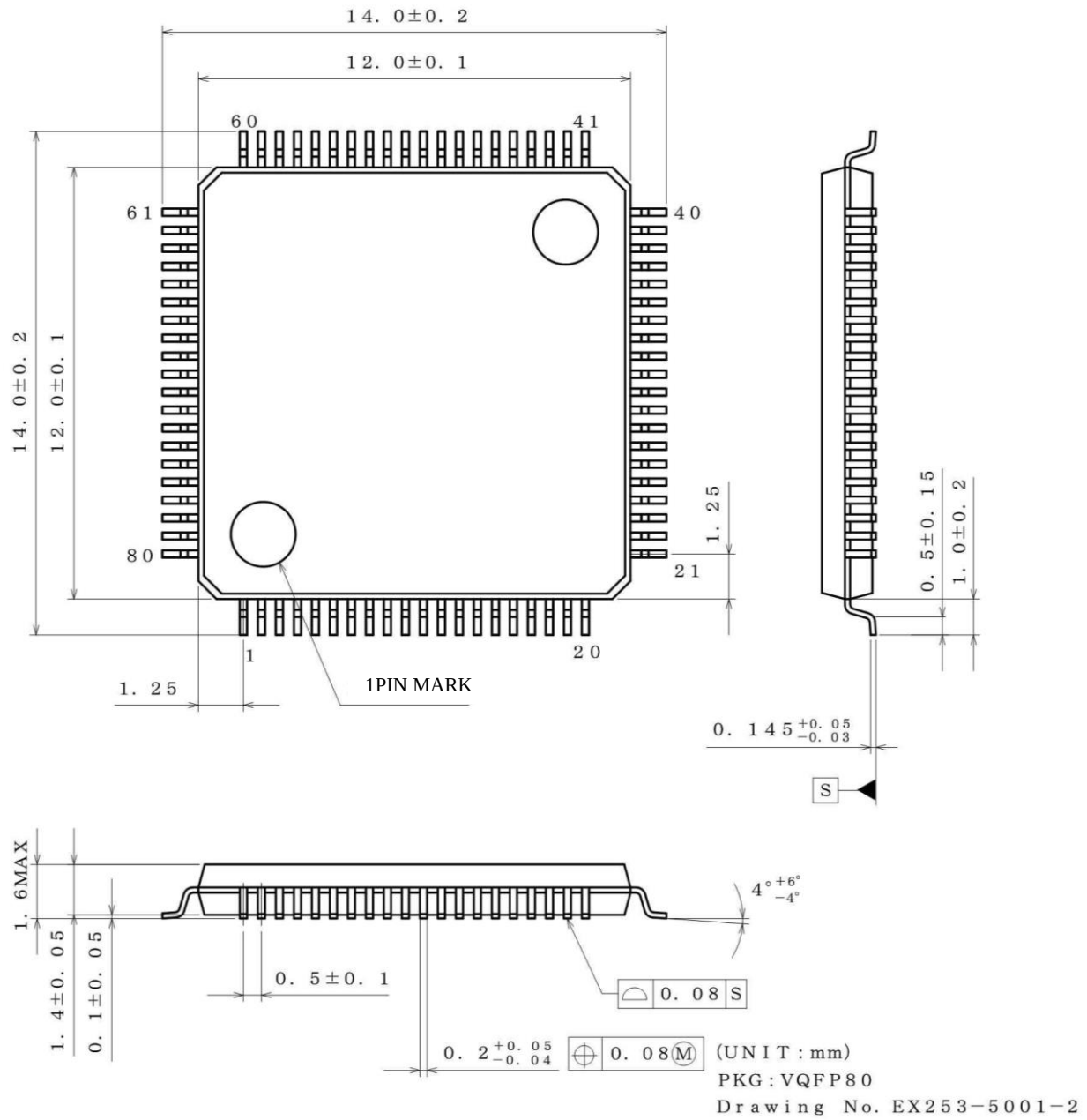


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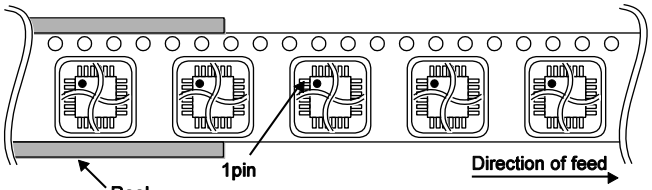
Physical Dimension, Tape and Reel Information

Package Name	VQFP80



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
30.Mar.2015	001	New Release
09.Jul.2015	002	Modified Absolute Maximum Ratings(6.5V to 7.0V) table in Page 3. Modified comment of figure.48 in Page 64.
21.Mar.2017	003	Page.3 Delete temperature condition in Absolute Maximum Ratings Page.4 Add tr,tf item in Oscillation Characteristics Page.7 Modify Figure.6 I/O Equivalent Circuit Page.22 Add notice of External Clock input timing function Page.25 Add The relationship of LCD display contrast setting and VLCD voltage Page.65Add notice of Power-saving mode operation in external clock mode Page.66 Add notice in Voltage Detection Type Reset Circuit (VDET) Change from “1/1 duty” to “Static” Add Reset condition in each Control Data Function Change “Sleep mode” to” Power-saving mode” Correction of errors
18 Jun 2019	004	Page. 9,11,13,15,17 and 19 Add Description

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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