NCP1532

Dual, Output Step-Down Converter

2.25 MHz

The NCP1532 dual step down DCDC converter is a monolithic integrated circuit dedicated to supply core and I/O voltages of new multimedia design in portable applications powered from 1−cell Li−ion or 3 cell Alkaline / NiCd / NiMH batteries.

Both channels are externally adjustable from 0.9 V to 3.3 V and can source totally up to 1.6 A, 1.0 A maximum per channel. Converters are running at 2.25 MHz switching frequency which reduces component size by allowing the use of small inductor (down to 1 μH) and capacitors and operates 180° out of phase to reduce large amount of current demand on the battery. Automatic switching PWM/PFM mode and synchronous rectification offer improved system efficiency. The device can also operate into fixed frequency PWM mode for low noise applications where low ripple and good load transients are required.

Additional features include integrated soft−start, cycle−by−cycle current limit and thermal shutdown protection. The device can also be synchronized to an external clock signal in the range of 2.25 MHz.

The NCP1532 is available in a space saving, ultra low profile 3x3 x 0.55 mm 10 pin μDFN package.

Features

- Up to 97% Efficiency
- 50 μA Quiescent Current
- Synchronous Rectification for Higher Efficiency
- 2.25 MHz Switching Frequency, 180° Out of Phase
- Sources up to 1.6 A, 1.0 A Maximum per Channel
- Adjustable Output Voltage from 0.9 V to 3.3 V
- Mode Selection Pin: Eco Mode or Low Noise Mode
- 2.7 V to 5.5 V Input Voltage Range
- Thermal Limit Protection
- Short Circuit Protection
- All pins are fully ESD Protected
- This is a Pb−Free Device

Typical Applications

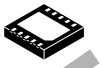
- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

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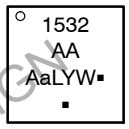
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MARKING DIAGRAM

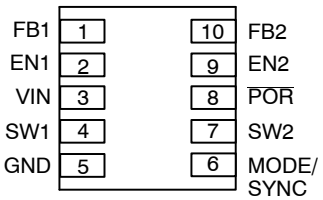


UDFN10
MU SUFFIX
CASE 506AT



Aa = Assembly Location
(may be 1 or 2 characters)
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)
UDFN10

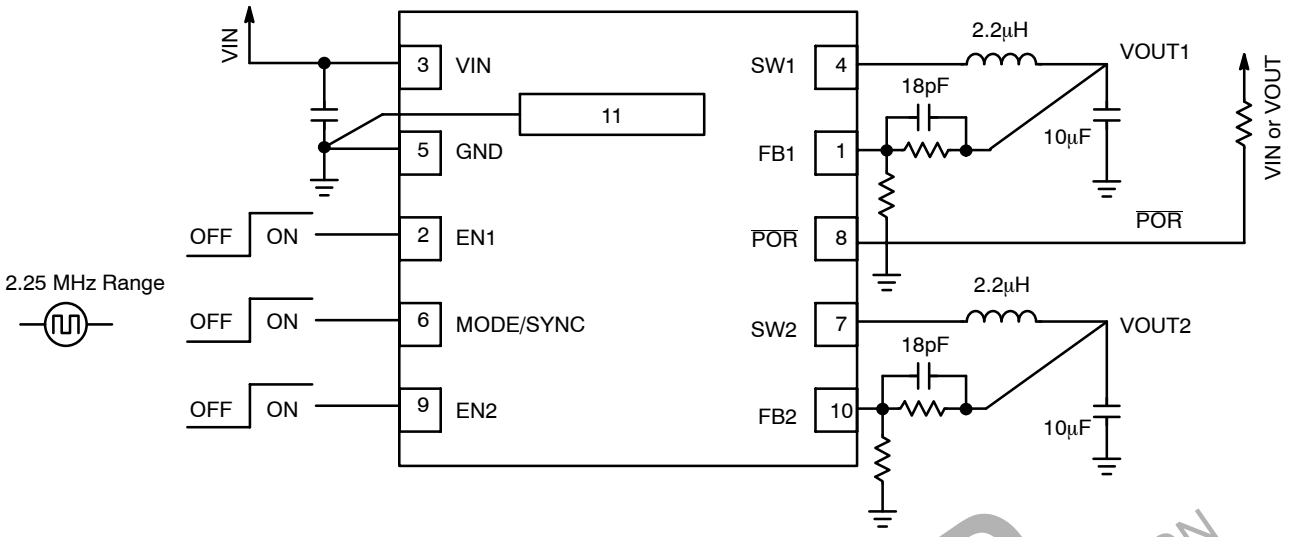
ORDERING INFORMATION

Device	Package	Shipping†
NCP1532MUAATXG	UDFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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NOTE: Exposed pad of UDFN10 package − named pin11 − must be connected to system ground.

Figure 1. NCP1532 Typical Application

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PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
1	FB1	Analog Input	Feedback voltage from the output 1. This is the input to the error amplifier.
2	EN1	Digital Input	Enable for converter 1. This pin is active HIGH (higher than 1.2 V) and is turned off by logic LOW (lower than 0.4 V. Do not leave this pin floating.
3	VIN	Analog / Power Input	Power supply input for the PFET power stage, analog and digital blocks. The pin must be decoupled to ground by a 10 µF ceramic capacitor.
4	SW1	Analog Output	Connection from power MOSFETs of output 1 to the Inductor.
5	GND	Analog Ground	This pin is the GROUND reference for the analog section of the IC. The pin must be connected to the system ground by 10 µF low ESR ceramic capacitor.
6	MODE/SYNC	Digital Input	Combination Mode Selection and Oscillator Synchronization. If this pin is LOW, the regulator runs in automatic switching PFM/PWM. With a HIGH level (equal or lower Analog Input voltage), the converter runs in PWM mode only. This pin can be also synchronized to an external clock in the range of 2.25 MHz; in this case the device runs in PWM mode only. Insert the clock before enabling the part is recommended to force external synchronization. Do not let this pin floating. Following rule is being used: ”0”: Eco mode, automatic switching PFM/PWM, 180° out of phase. “1”: Low noise, forced PWM mode, 180° out of phase. ”CLK”: External synchronization, forced PWM mode, 0° in phase.
7	SW2	Analog Output	Connection from power MOSFETs of output 2 to the Inductor.
8	POR	Digital Output	Power On Reset. This is an open drain output. This output is shutting down when each output voltages are less than 90% of their nominal values and goes high after 120 ms when active outputs are within regulation. A pullup resistor around 500k should be connected between POR and V_{IN}, V_{OUT1} or V_{OUT2} depending on the supplied device.
9	EN2	Digital Input	Enable for converter 2. This pin is active HIGH (higher than 1.2 V) and is turned off by logic LOW (lower than 0.4 V). Do not let this pin floating.
10	FB2	Analog Input	Feedback voltage from the output 2. This is the input to the error amplifier.
11	Exposed Pad	Power Ground	This pin is the GROUND reference for the NFET power stage of the IC. The pin must be connected to the system ground and to both input and output capacitors.

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BLOCK DIAGRAM

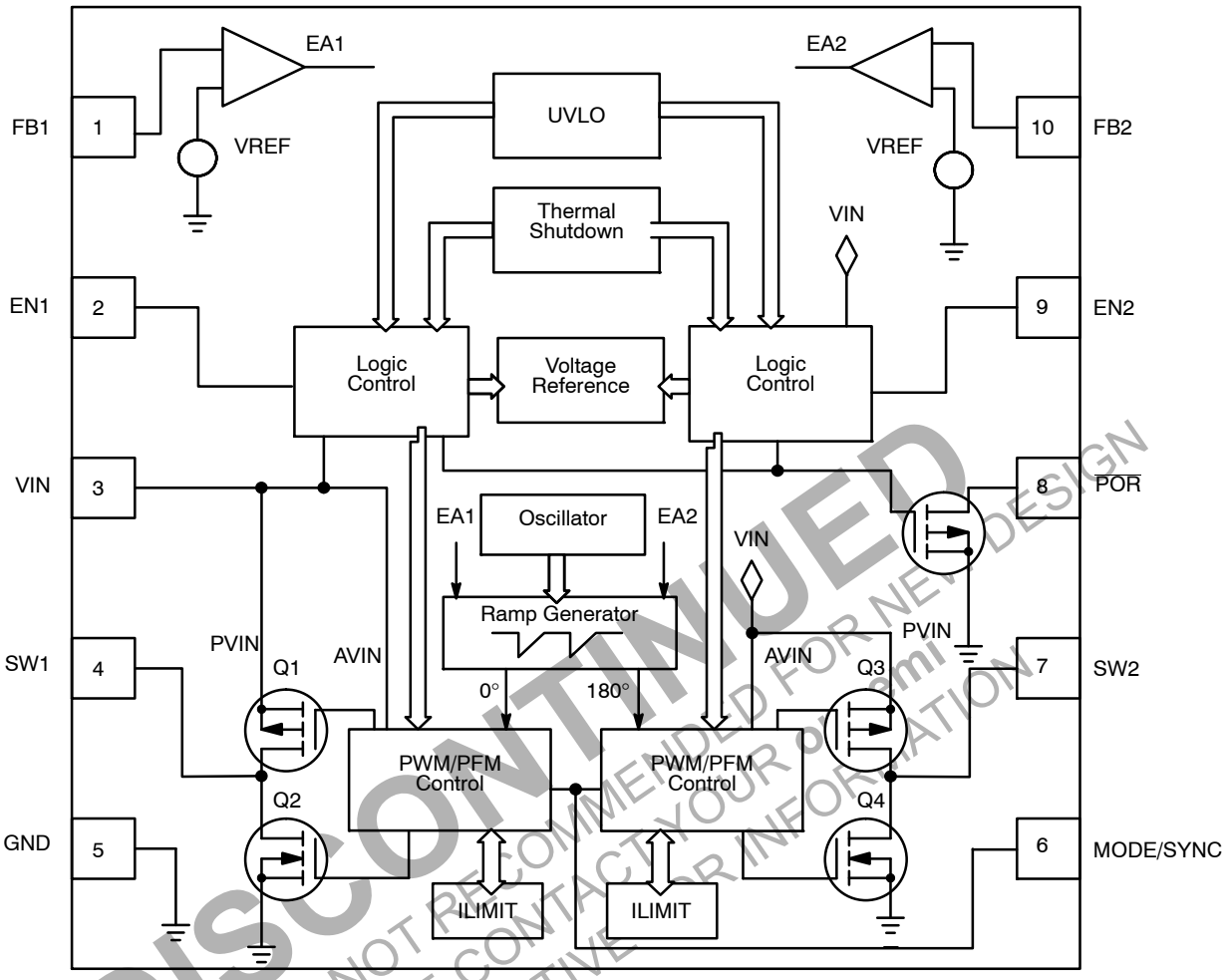


Figure 2. Simplified Block Diagram

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins (Note 1)	V_{max}	7.0	V
Maximum Voltage EN1, EN2, MODE	V_{max}	V_{IN} + 0.3	V
Thermal Resistance Junction−to−Air (UDFN10 Package) Thermal Resistance Using Recommended Board Layout (Note 8)	$R_{\theta JA}$	200 40	°C/W
Operating Ambient Temperature Range (Notes 6 and 7)	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature (Notes 6 and 7)	T_J	−40 to 150	°C
Latchup Current Maximum Rating T_A = 85°C (Note 4) Other Pins	L_u	±100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V_{esd}	 2.0 200	 kV V
Moisture Sensitivity Level (Note 5)	MSL	1	per IPC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C
2. According JEDEC standard JESD22−A108B
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114
   Machine Model (MM) per JEDEC standard: JESD22−A115
4. Latchup current maximum rating per JEDEC standard: JESD78.
5. JEDEC Standard: J−STD−020A.
6. In applications with high power dissipation (low V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. Board design considerations − thermal dissipation vias, traces or planes and PCB material − can significantly improve junction to air thermal resistance $R_{\theta JA}$ (for more information, see design and layout consideration section). Environmental conditions such as ambient temperature Ta brings thermal limitation on maximum power dissipation allowed.
   The following formula gives calculation of maximum ambient temperature allowed by the application: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_d)$
   Where
   T_J is the junction temperature,
   P_d is the maximum power dissipated by the device (worst case of the application), and $R_{\theta JA}$ is the junction−to−ambient thermal resistance.
7. To prevent permanent thermal damages, this device include a thermal shutdown which engages at 180°C (typical).
8. Board recommended UDFN10 layout is described in Layout Considerations section.

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ELECTRICAL CHARACTERISTICS

(Typical values are referenced to T_A = +25°C, Minimum and Maximum values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.2 V, unless otherwise noted).

Rating	Conditions	Symbol	Min	Typ	Max	Unit
INPUT VOLTAGE						
Input Voltage Range		V_{IN}	2.7	–	5.5	V
Quiescent Current, No Switching, No Load No Load	MODE/SYNC = GND	I_Q	 – –	 50 60	 70 –	μA
Standby Current	EN1 = EN2 = GND	I_{STB}	–	0.3	1.0	μA
Under Voltage Lockout	V_{IN} Falling	V_{UVLO}	2.2	2.4	2.55	V
Under Voltage Hysteresis		V_{UVLOH}	–	100	–	mV
ANALOG AND DIGITAL PIN						
Positive Going Input High Voltage Threshold	EN1, EN2, MODE/SYNC	V_{IH}	1.2	–	–	V
Negative Going Input High Voltage Threshold	EN1, EN2, MODE/SYNC	V_{IL}	–	–	0.4	V
Digital Threshold Hysteresis	EN1, EN2, MODE/SYNC	V_{HYS}	–	100	–	mV
External Synchronization (Note 11) Minimum Maximum	MODE/SYNC	F_{SYNC}	 – –	 1.8 3.0	 – –	MHz
POWER ON RESET (Note 9)						
Power On Reset Threshold	V_{OUT} Falling	V_{PORT}	–	89%	–	V
Power On Reset Hysteresis		V_{PORH}	–	3%	–	V
Power On Reset Delay (See Page 12)		T_{POR}	–	116	–	ms
OUTPUT PERFORMANCES						
Feedback Voltage Threshold	FB1, FB2	V_{FB}	–	0.6	–	V
Minimum Output Voltage		V_{OUT}	–	0.9	–	V
Maximum Output Voltage		V_{OUT}	–	3.3	–	V
Output Voltage Accuracy (Note 10)	Room Temperature Overtemperature Range	ΔV_{OUT}	– −3%	±1% ±2%	– +3%	%
Output Voltage load regulation NCP1532MUAATXG	Overtemperature Load = 100 mA to 600 mA	V_{LOADR}	 –	 −0.6	 –	%
Load transient response Rise/Falltime 1 μs	10 mA to 100 mA load step (PFM to PWM mode) 200 mA to 600 mA load step (PWM to PWM mode)	V_{LOADT}	– –	40 85	– –	mV
Output Voltage Line Regulation Load = 100 mA	V_{IN} = 2.7 V to 5.5 V	V_{LINER}	–	0.05	–	%
Line Transient Response Load = 100 mA	3.6 V to 3.2 V Line Step (Falltime = 50 μs)	V_{LINET}	–	6.0	–	mV_{PP}
Output Voltage Ripple	I_{OUT} = 0 mA I_{OUT} = 300 mA	V_{RIPPLE}	– –	8.0 3.0	– –	mV_{PP}
Soft−Start Time	Time from EN to 90% of Output Voltage	t_{START}	–	230	350	μs
Switching Frequency		F_{SW}	1.8	2.25	2.7	MHz
Duty Cycle		D	–	–	100	%

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ELECTRICAL CHARACTERISTICS

(Typical values are referenced to T_A = +25°C, Minimum and Maximum values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.2 V, unless otherwise noted).

Rating	Conditions	Symbol	Min	Typ	Max	Unit
POWER SWITCHES						
High−Side MOSFET On−Resistance		R_{ONHS}	−	400	−	mΩ
Low−Side MOSFET On−Resistance		R_{ONLS}	−	300	−	mΩ
High−Side MOSFET Leakage Current		I_{LEAKHS}	−	0.05	−	μA
Low−Side MOSFET Leakage Current		I_{LEAKLS}	−	0.01	−	μA
PROTECTION						
DC−DC Short Circuit Protection	Peak Inductor Current	I_{PK}	1.2	1.6	−	A
Thermal Shutdown Threshold		T_{SD}	−	180	−	°C
Thermal Shutdown Hysteresis		T_{SDH}	−	40	−	°C

9. Refer to Power On Reset section for more information.
10. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1 and R2).
11. Guaranteed by design.

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TABLE OF GRAPHS

TYPICAL CHARACTERISTICS FOR STEP DOWN CONVERTER			FIGURE
η	Efficiency	vs. Output Current	3, 4, 5, 6, 7, 8
$I_{q\ ON}$	Quiescent Current, PFM no load	vs. Input Voltage	11
$I_{q\ OFF}$	Standby Current, EN Low	vs. Input Voltage	10
F_{SW}	Switching Frequency	vs. Ambient Temperature	16
V_{LOADR}	Load Regulation	vs. Load Current	13
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V_{UVLO}	Under Voltage Lockout Threshold	vs. Ambient Temperature	20
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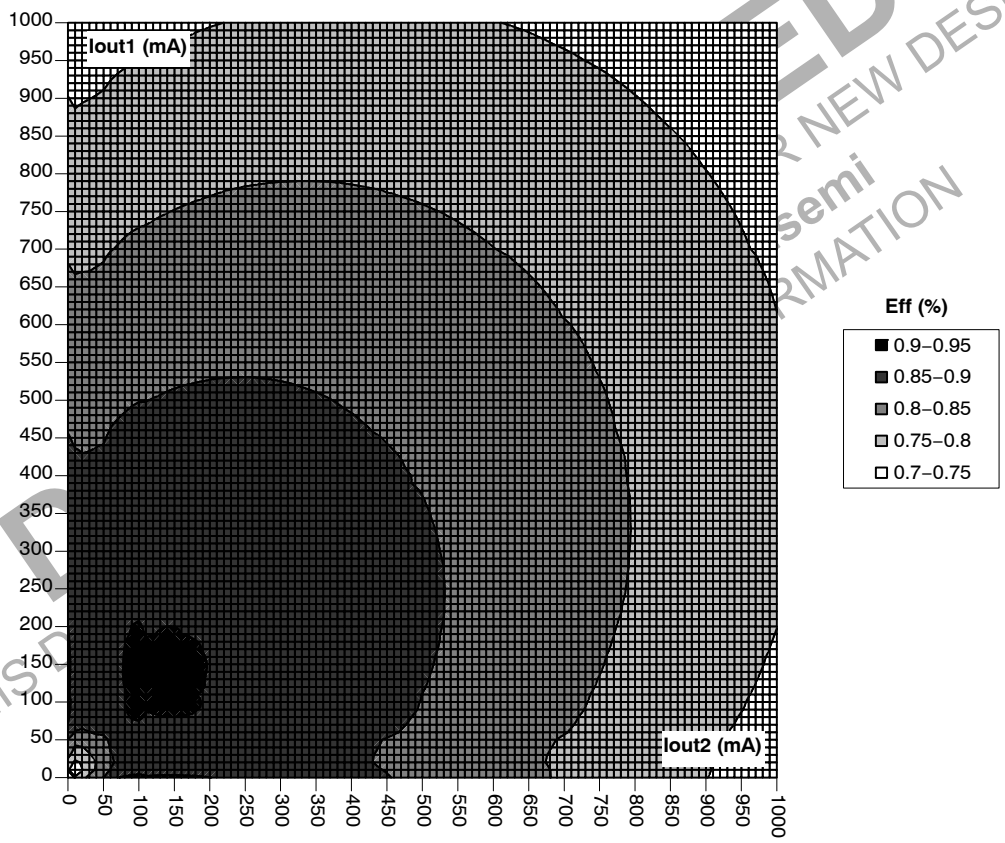


Figure 3. Efficiency vs. Output Current (V_{IN} = 3.6 V, V_{OUT1} = 1.8 V, V_{OUT2} = 1.8 V, Temperature = 25°C) MODE/SYNC Pin = GND

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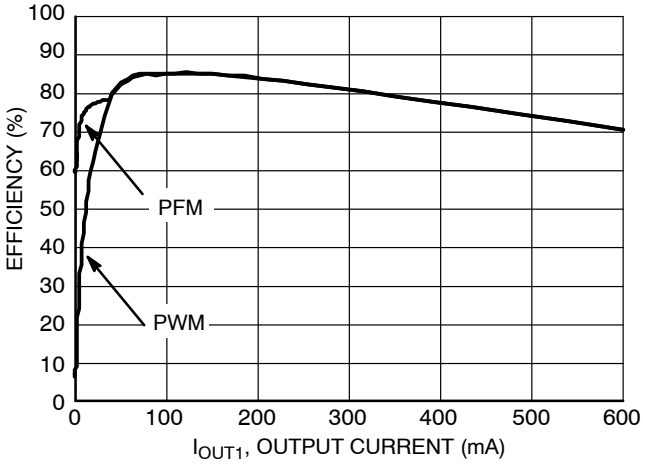


Figure 4. Efficiency vs. Output Current
V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, EN2 = GND

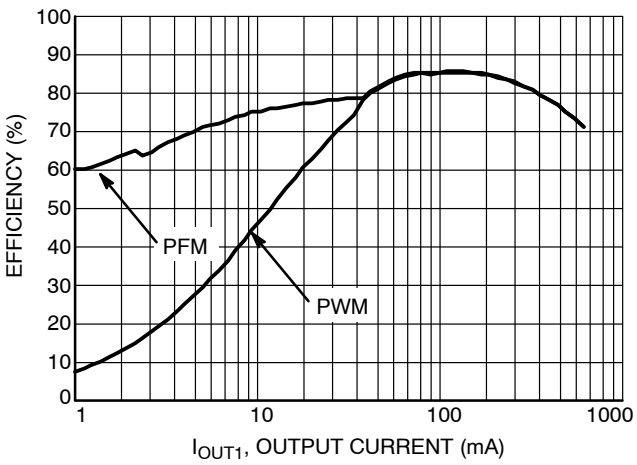


Figure 5. Efficiency vs. Output Current
V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, EN2 = GND

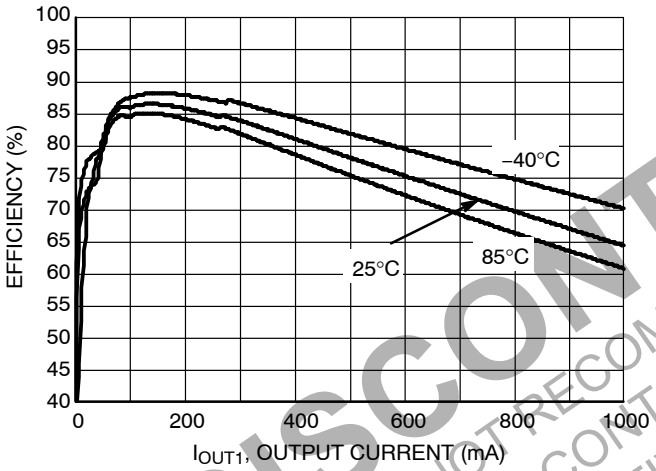


Figure 6. Efficiency vs. Output Current
V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, EN2 = GND, Temperature = 25°C

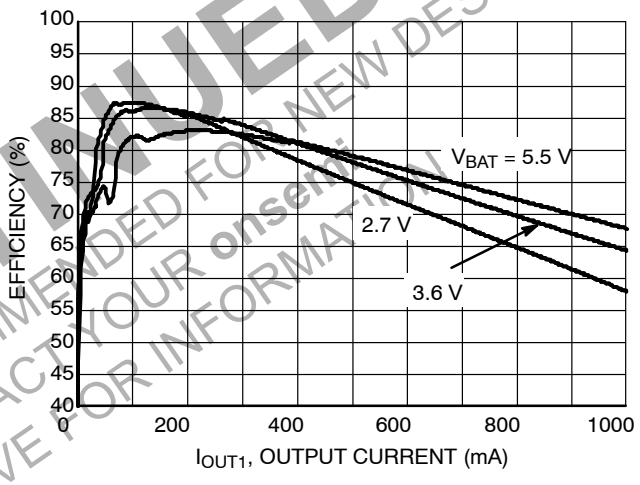


Figure 7. Efficiency vs. Output Current
V_{OUT1} = 1.2 V, EN2 = GND, Temperature = 25°C

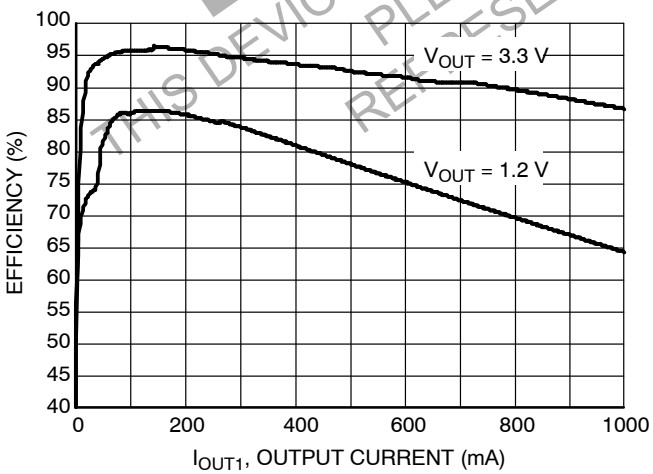


Figure 8. Efficiency vs. Output Current
V_{IN} = 3.6 V, EN2 = GND, Temperature = 25°C

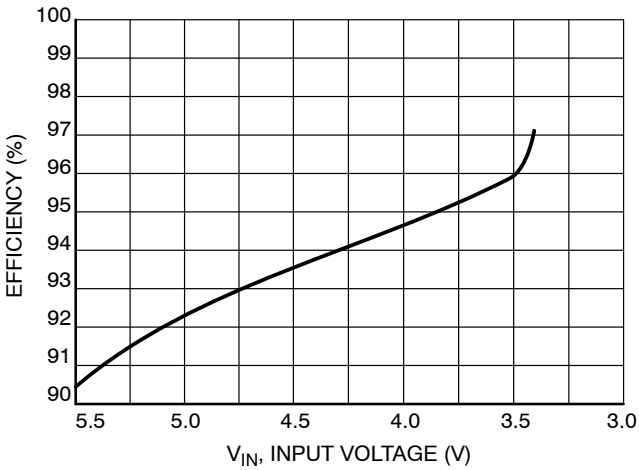


Figure 9. Maximum Efficiency vs. Input Voltage
V_{OUT1} = V_{OUT2} = 3.3 V I_{OUT1} = I_{OUT2} = 100 mA

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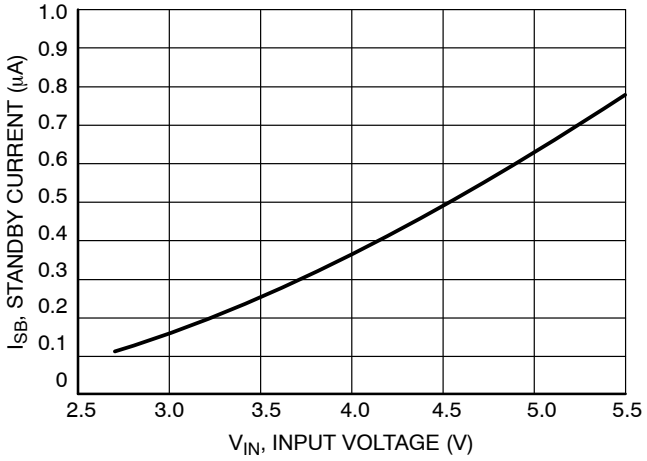


Figure 10. Standby Current vs. Input Voltage
V_{IN} = 3.6 V, EN1 = EN2 = GND, Temperature = 25°C

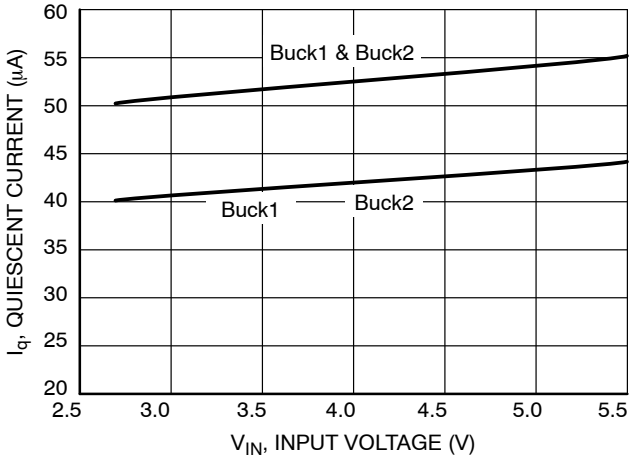


Figure 11. Quiescent Current vs. Input Voltage
V_{IN} = 3.6 V, V_{FB1} = V_{FB2} = 0.8 V

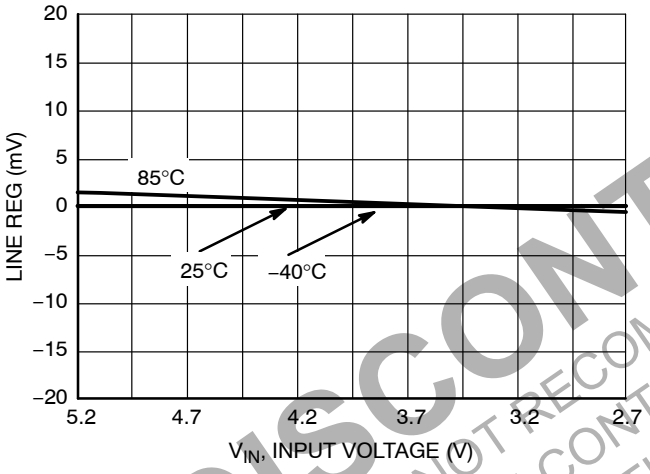


Figure 12. Line Regulation
V_{OUT1} = 1.2 V, I_{OUT1} = 100 mA, EN2 = GND

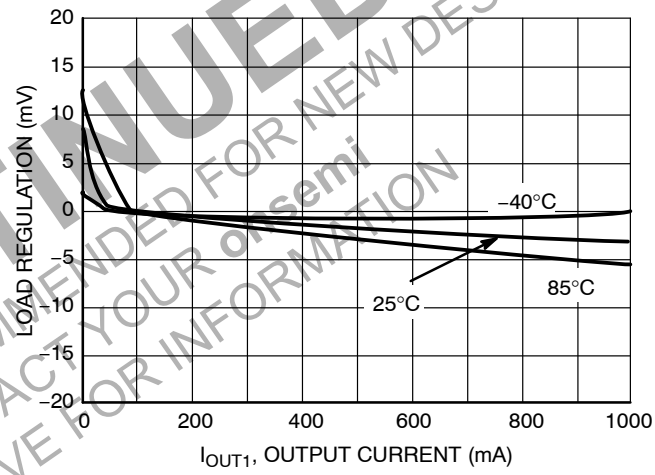


Figure 13. Load Regulation
V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, EN2 = GND

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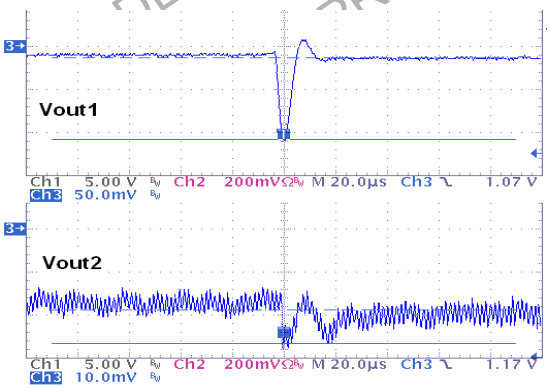


Figure 14. Load Transient and Crosstalk, V_{IN} = 3.6 V V_{OUT1} = 1.2 V, I_{OUT1} from 200 mA to 600 mA V_{OUT2} = 1.2 V, I_{OUT2} = 600 mA, 8 mV Crosstalk

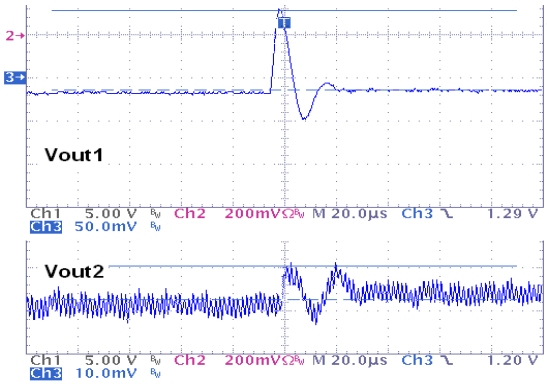


Figure 15. Load Transient and Crosstalk, V_{IN} = 3.6 V V_{OUT1} = 1.2 V, I_{OUT1} from 200 mA to 600 mA V_{OUT2} = 1.2 V, I_{OUT2} = 600 mA, 8 mV Crosstalk

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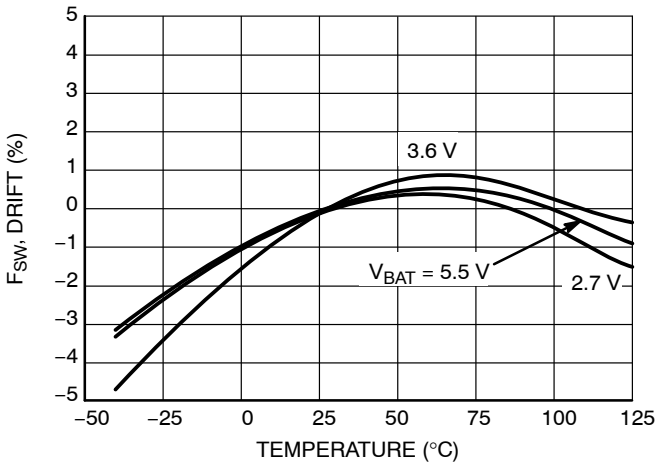


Figure 16. Switching Frequency vs. Temperature

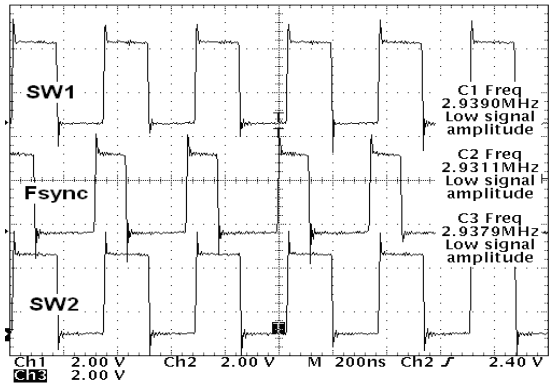


Figure 17. External Synchronization, F_{sync} = 2.93 MHz

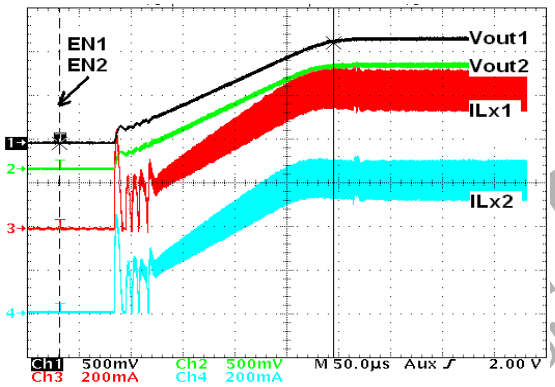


Figure 18. Soft−Start Typical Behavior V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.2 V, I_{OUT1} = I_{OUT2} = 600 mA

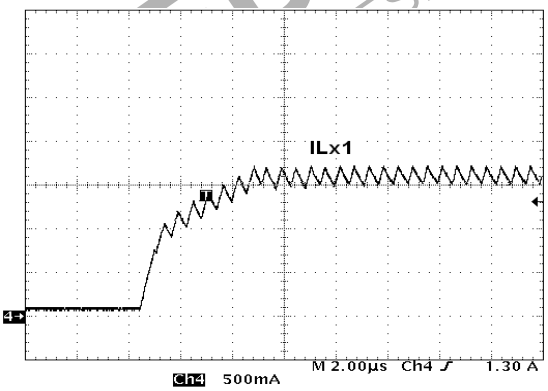


Figure 19. Current Peak Inductor Protection V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, I_{OUT1} Short to GND, EN2 = GND

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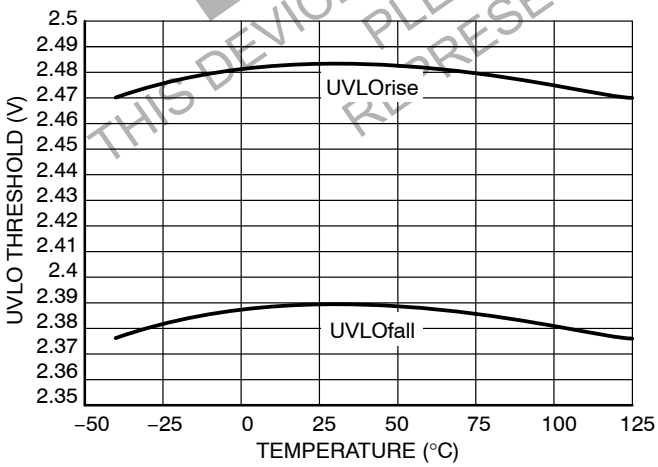


Figure 20. UVLO Thresholds V_{IN} = 3.6 V, I_{OUT1} = I_{OUT2} = 2 mA

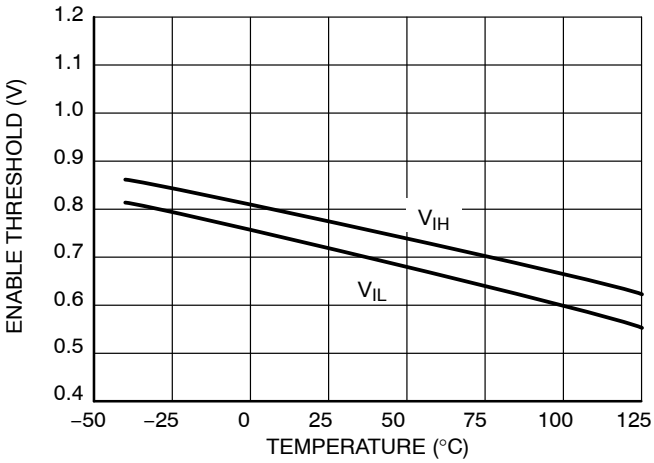


Figure 21. Enable Thresholds V_{IN} = 3.6 V, I_{OUT1} = I_{OUT2} = 2 mA

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DC/DC OPERATION DESCRIPTION

Detailed Description

The NCP1532 uses a constant frequency, current mode step−down architecture. Both the main (P−channel MOSFET) and synchronous (N−channel MOSFET) switches are internal.

The output voltages are set by the external resistor divider in the range of 0.9 V to 3.3 V and can source 1600 mA totally depending on device option.

The NCP1532 works with two modes of operation; PWM/PFM depending on the current required. In PWM mode, the device can supply voltage with a tolerance of ±3% and 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM mode to reduce current consumption (I_q = 50 μA) and extended battery life. For low noise applications, by pulling the MODE/SYNC Pin to V_{IN}, the device operates in PWM mode only.

Additional features include soft−start, undervoltage protection, current overload protection and thermal shutdown protection. As shown on Figure 1, only six external components are required for implementation. The part uses an internal reference voltage of 0.6 V. It is recommended to keep NCP1532 in shutdown until the input voltage is 2.7 V or higher. To reduce power demand on the battery, the two DC−DC operates out of phase. This reduces significantly spikes on V_{in} line. Using external synchronization, the two channels are working on same signal phase. See MODE/SYNC section for more information.

PWM Operating Mode

In this mode, the output voltage of the device is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed 2.25 MHz frequency.

The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp.

The driver switches ON and OFF the upper side transistor (Q1) and switches the lower side transistor in either ON state or in current source mode.

At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error amplifier's voltage. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF while the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

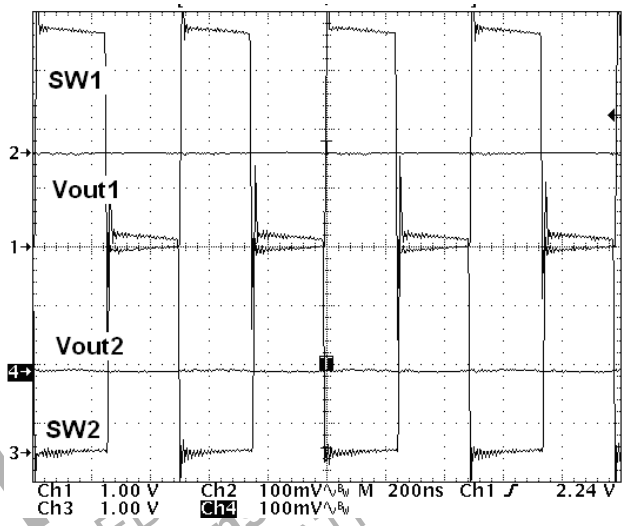


Figure 22. PWM Switching Waveforms
V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.2 V,
I_{OUT1} = I_{OUT2} = 100 mA

PFM Operating Mode

Under light load conditions, the NCP1532 enters in low current PFM mode of operation to reduce power consumption. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PFM comparator a new cycle will be initiated by the PFM comparator to turn on the switch Q1. Q1 remains ON during the minimum on time of the structure while Q2 is in its current source mode. The peak inductor current depends upon the drop between input and output voltage. After a short dead time delay where Q1 is switched OFF, Q2 is turned in its ON state. The negative current detector will detect when the inductor current drops below zero and sends the signal to turn Q2 in current source mode to prevent a too large deregulation of the output voltage. When the output voltage falls below the threshold of the PFM comparator, a new cycle starts immediately.

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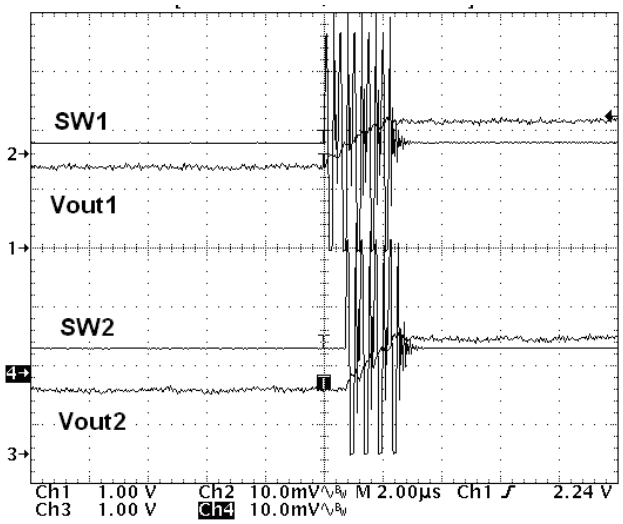


Figure 23. PFM Switching Waveforms
V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.2 V,
I_{OUT1} = I_{OUT2} = 0 mA

Soft−Start

The NCP1532 uses soft−start to limit the inrush current when the device is initially powered up or enabled. Soft−start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Cycle−by−Cycle Current Limitation

From the block diagram (Figure 2), an I_{LIM} comparator is used to realize cycle−by−cycle current limit protection. The comparator compares the SW pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the ILIM comparator detects the SW voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle−by−cycle current limit is set at 1600 mA (nom).

Low Dropout Operation

The NCP1532 offers a low input to output voltage difference. The NCP1532 can operate at 100% duty cycle on both channels.

In this mode the PMOS (Q1) remains completely ON. The minimum input voltage to maintain regulation can be calculated as:

$$V_{IN}(min) = V_{OUT}(max) + (I_{OUT} \times (R_{DS(on)} + R_{INDUCTOR}) \quad \text{(eq. 1)}$$

- V_{OUT}: Output Voltage (V)
- I_{OUT}: Maximum Output Current
- $R_{DS(on)}$: P−Channel Switch $R_{DS(on)}$
- $R_{INDUCTOR}$: Inductor Resistance (DCR)

Power On Reset

The Power On Reset (POR) is pulled low when either active converter is out of 89% of their regulation. When active outputs are in the range of regulation, a counter starts to provide the POR signal with a delay equal to 262,144 clock cycles. The delay is depending on internal clock frequency. If only one channel is active, POR runs only on the active output until the other converter is disabled. When this regulator becomes enabled, POR drops down until the second output reaches its voltage range. A pullup resistor (around 500 k) is needed to this open drain output. This resistor may be connected to V_{IN} or to an output voltage of one regulator if the device supplied cannot accept V_{IN} on the IO. In the case of POR being tied to V_{IN}, POR is high when NCP1532 is off. In the case of POR being tied to V_{OUT}, POR is low when NCP1532 is off.

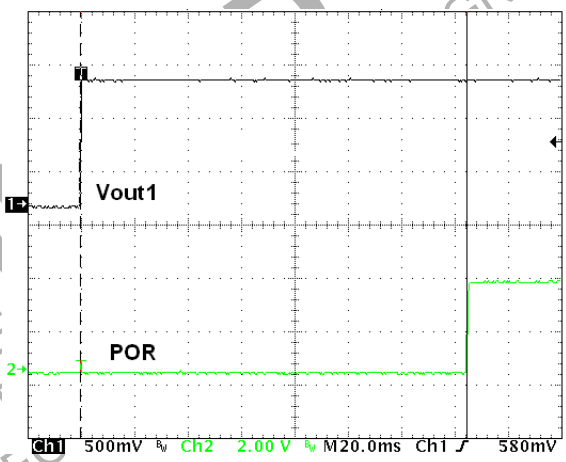


Figure 24. POR Behavior vs. V_{OUT1}

Leave the POR pin unconnected when not used.

Mode Selection and Frequency Synchronization

The MODE/SYNC pin is a multipurpose pin which provides mode selection and frequency synchronization. When this pin is connected to ground, auto−switching PFM/PWM mode is selected which provides the best efficiency at light load and quiescent current with a good ripple compromise (less than 8 mV). Connecting this pin to V_{IN} enables PWM mode of operation, which provides the best low noise solution, low ripple and low load transient performance.

NCP1532 can also be synchronized to an external clock signal in the range from internal switching frequency to 3.0 MHz. Lower frequency causes the part enters one time in PFM/PWM mode, and the other time in PWM mode. Insert the clock before enabling the part is recommended to force external synchronization. This function allows synchronizing NCP1532 with another switching device such as the switching output of another DC to DC converter forced in PWM mode. This decreases noise dispersion generated by the converters.

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Undervoltage Lockout

The Input voltage V_{IN} must reach 2.4 V (typ) before the NCP1532 enables the DC/DC converter output to begin the start up sequence (see soft−start section). The UVLO threshold hysteresis is typically 100 mV.

Shutdown Mode

When the EN pin has applied voltage of less than 0.4 V, the NCP1532 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.3 μA (typical value). Applying a voltage above 1.2 V to EN pin will enable the DC/DC converter for normal operation. The device will go through soft−start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction Temperature is exceeded. If the junction temperature exceeds 180°C, the device shuts down. In this mode all power transistors and control circuits are turned off. The device restarts in soft start after the temperature drops below 140°C. This feature is provided to prevent catastrophic failures from accidental device overheating.

Short Circuit Protection

When one output is shorted to ground, the device limits the inductor current. The duty−cycle is minimum and the consumption on the input line is 300 mA (typ). When the short circuit condition is removed, the device returns to the normal mode of operation.

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connected from V_{OUT} to FB then to GND.

For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100 kΩ 600 k] range. If R2 is 200 k given the V_{FB} is 0.6 V, the current through the divider will be 3.0 μA.

The formula below gives the value of V_{OUT}, given the desired R1 and the R2 value:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 2)}$$

- V_{OUT}: Output Voltage (V)
- V_{FB}: Feedback Voltage = 0.6 V
- R1: Feedback Resistor from V_{OUT} to FB
- R2: Feedback Resistor from FB to GND

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is IO, max/2.

For NCP1532, a low profile ceramic capacitor of 10 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the VIN Pin. Capacitors with 10 V rated voltage are recommended to avoid DC bias effect over input voltage range.

Table 1. LIST OF INPUT CAPACITOR

Murata	GRM21BR61A106	10 μF
Taiyo Yuden	JMK212BJ106	10 μF
TDK	C2012X5R1A106	10 μF

Output L−C Filter Design Considerations

The NCP1532 is built in 2.25 MHz frequency and uses current mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L−C filter must be selected to work with internal compensation. For NCP1532, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 10 μF.

The corner frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 10 \mu F}} = 34\ kHz \quad \text{(eq. 3)}$$

The device operates with inductance value of 2.2 μH. If the corner frequency is moved, it is recommended to check the loop stability depending of the accepted output ripple voltage and the required output current. Take care to check the loop stability. The phase margin is usually higher than 45°.

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Table 2. Table 2: L−C FILTER EXAMPLE

Inductance (L)	Output Capacitor (C_{OUT})
1.0 μH	22 μF
2.2 μH	10 μF
4.7 μH	4.7 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 4)}$$

- ΔI_L: Peak−to−Peak Inductor Ripple Current
- L: Inductor Value
- f_{SW}: Switching Frequency

The saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_L(max) = I_O(max) + \frac{\Delta I_L}{2} \quad \text{(eq. 5)}$$

- I_L(max): Maximum Inductor Current
- I_O(max): Maximum Output Current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 3. LIST OF INDUCTOR

FDK	MIPW3226 series
TDK	VLF3010AT series
	TFC252005 series
Taiyo Yuden	LQ CBL2012
Coil craft	DO1605 Series
	LPS4018 series

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric. We recommend to place a capacitor with rated voltage much higher than the output voltage selected by the external divider. Capacitors with 10 V rated voltages are recommended from 2.0 V to 3.3 V output voltages.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR\right) \quad \text{(eq. 6)}$$

Table 4. LIST OF OUTPUT CAPACITOR

Murata	GRM219R61A475	4.7 μF
	GRM21BR61A106	10 μF
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5R1A475	4.7 μF
	C2012X5R1A106	10 μF

Feed−Forward Capacitor Selection

The feed−forward capacitor sets the feedback loop response and is critical to obtain good loop stability. Given that the compensation is internally fixed, an 18 pF or higher ceramic capacitor is needed. Choose a small ceramic capacitor X7R or X5R or COG dielectric.

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LAYOUT CONSIDERATIONS

Electrical Layout Considerations

Implementing a high frequency DC−DC converter requires respect of some rules to get a powerful portable application. Good layout is key to prevent switching regulators to generate noise to application and to themselves.

Electrical layout guide lines are:

- Use short and large traces when large amount of current is flowing.
- Keep the same ground reference for input and output capacitors to minimize the loop formed by high current path from the battery to the ground plane.
- Isolate feedback pin from the switching pin and the current loop to protect against any external parasitic signal coupling. Add a feed−forward capacitor between VOUT and FB which adds a zero to the loop and participates to the good loop stability. A 18 pF capacitor is recommended to meet compensation requirements. A four layer PCB with a ground plane and a power plane will help NCP1532 noise immunity and loop stability.

Thermal Layout Considerations

High power dissipation in small package leads to thermal consideration such as:

- Enlarge the V_{IN} trace and add several vias that are connected to power plane.
- Connect the GND pin to the top plane.
- Join top, bottom and each ground plane together using several free vias in order to increase dissipation capability.

For high ambient temperature and high power dissipation requirements, refer to notes 7, 8, and 9 to prevent any thermal issue.

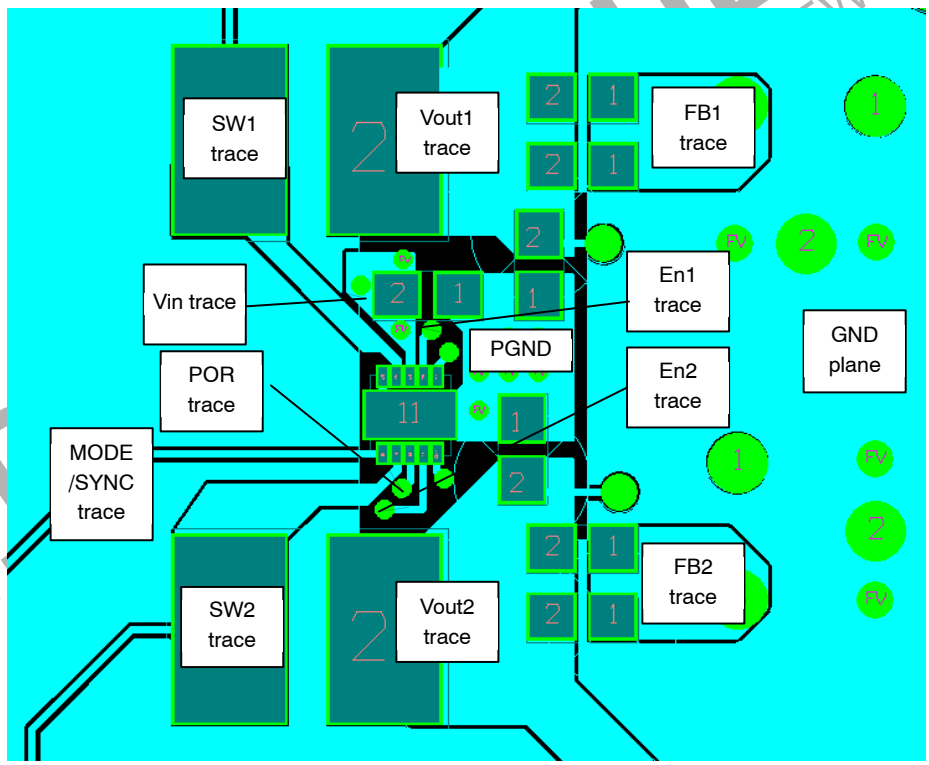


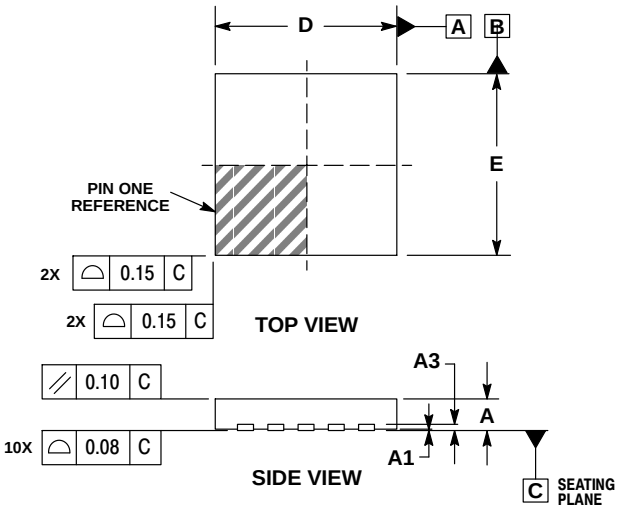
Figure 25.

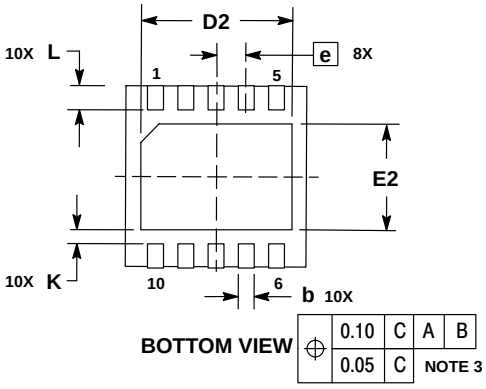
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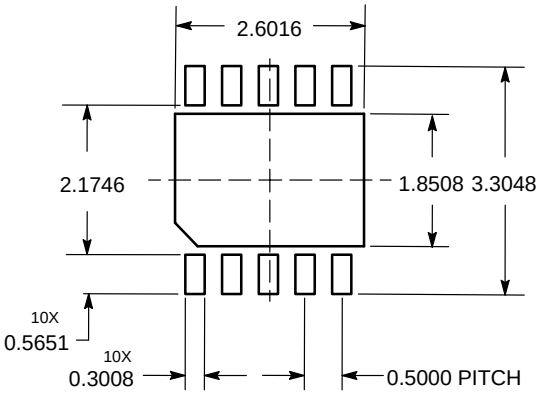
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SCALE 2:1





SOLDERING FOOTPRINT*



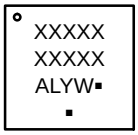
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3		0.127 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.19 TYP	
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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