1Mb Ultra-Low Power Asynchronous CMOS SRAM

128K × 8 bit

Overview

The N01L83W2A is an integrated memory device containing a 1 Mbit Static Random Access Memory organized as 131,072 words by 8 bits. The device is designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. The N01L83W2A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 128Kb x 8 SRAMs.

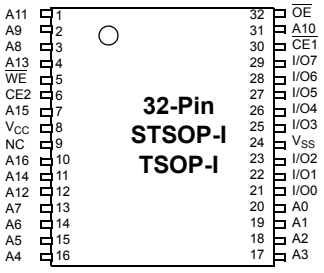
Features

- **Single Wide Power Supply Range**
  2.3 to 3.6 Volts
- **Very low standby current**
  2.0µA at 3.0V (Typical)
- **Very low operating current**
  2.0mA at 3.0V and 1µs (Typical)
- **Very low Page Mode operating current**
  0.8mA at 3.0V and 1µs (Typical)
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$and CE2)
  Output Enable ($\overline{OE}$) for memory expansion
- **Low voltage data retention**
  Vcc = 1.8V
- **Very fast output enable access time**
  30ns $\overline{OE}$ access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB}), Typical	Operating Current (Icc), Typical
N01L83W2AT	32 - TSOP I	-40°C to +85°C	2.3V - 3.6V	55ns @ 2.7V 70ns @ 2.3V	2 µA	2 mA @ 1MHz
N01L83W2AN	32 - STSOP I					
N01L83W2AT2	32 -TSOP I Green					
N01L83W2AN2	32 - STSOP I Green					

Pin Configuration



Pin Descriptions

Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
I/O_0-I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected

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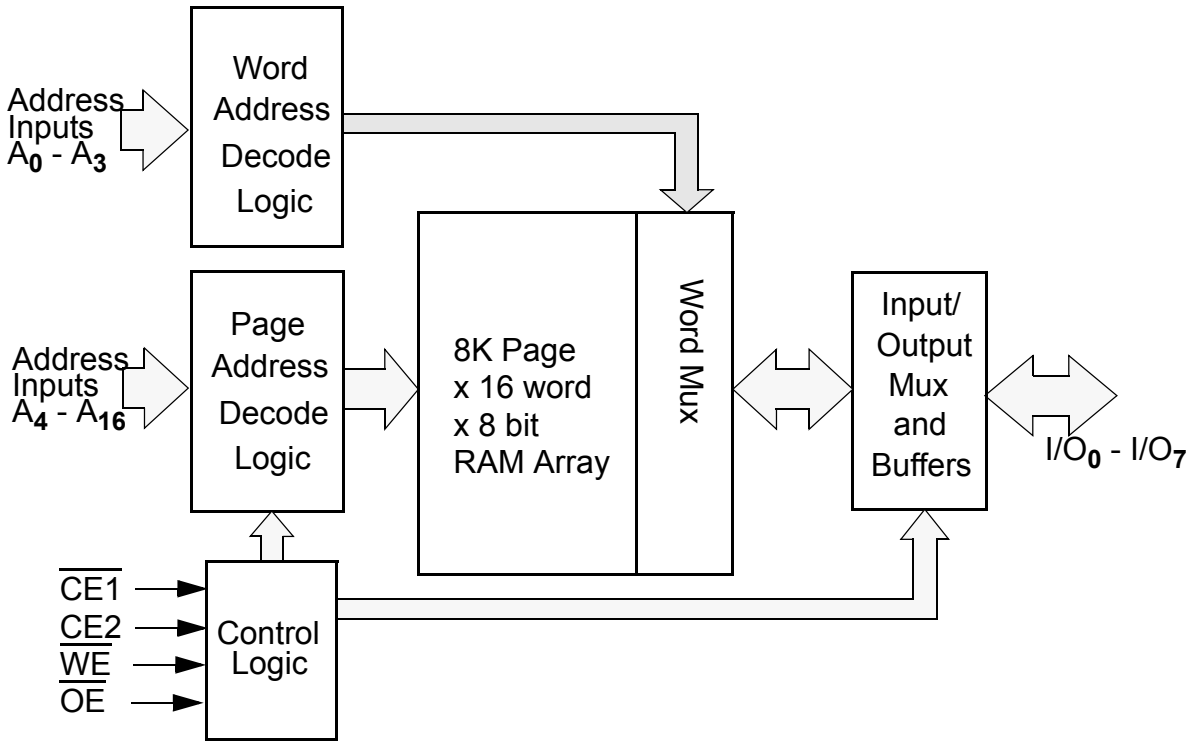
Publication Order Number:
N01L83W2A/D

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O_0 - I/O_7	MODE	POWER
H	X	X	X	High Z	Standby[1]	Standby
X	L	X	X	High Z	Standby[1]	Standby
L	H	L	X[2]	Data In	Write[2]	Active
L	H	H	L	Data Out	Read	Active
L	H	H	H	High Z	Active	Active

1. When the device is in standby mode, control inputs ($\overline{WE}$ and $\overline{OE}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
2. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

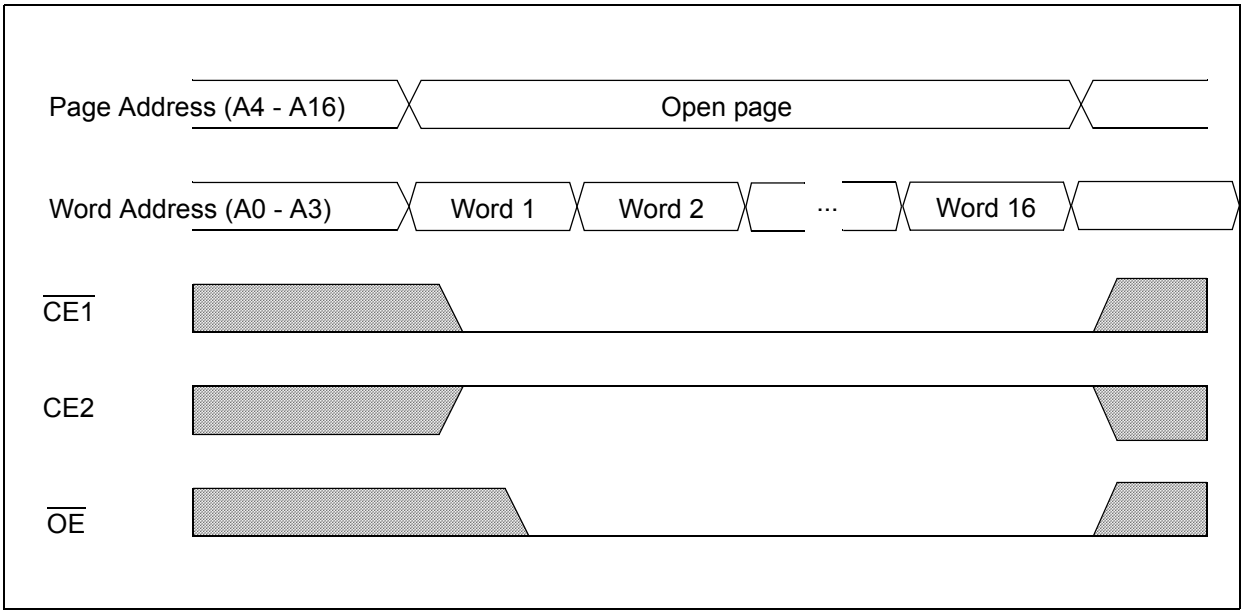
Item	Symbol	Test Conditions	Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}		2.3	3.0	3.6	V
Data Retention Voltage	V_{DR}	Chip Disabled[3]	1.8			V
Input High Voltage	V_{IH}		1.8		V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CC}–0.2			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current @ 1 µS Cycle Time[2]	I_{CC1}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		2.0	3.0	mA
Read/Write Operating Supply Current @ 70 nS Cycle Time[2]	I_{CC2}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		9.5	14.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time[2] (Refer to Power Savings with Page Mode Operation diagram)	I_{CC3}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0,		4		mA
Read/Write Quiescent Operating Supply Current[3]	I_{CC4}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0, f = 0			3.0	mA
Maximum Standby Current[3]	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, V_{CC} = 3.6 V		2.0	20	µA
Maximum Data Retention Current[3]	I_{DR}	Vcc = 1.8V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A= 85°C			10	µA

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.

Power Savings with Page Mode Operation ($\overline{WE}$ = V_{IH})



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 8-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

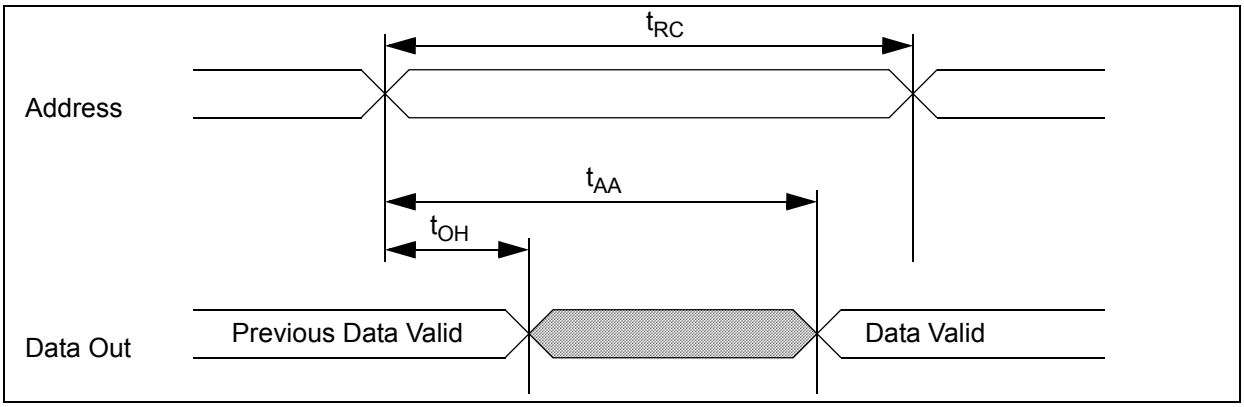
Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 ^{O}C

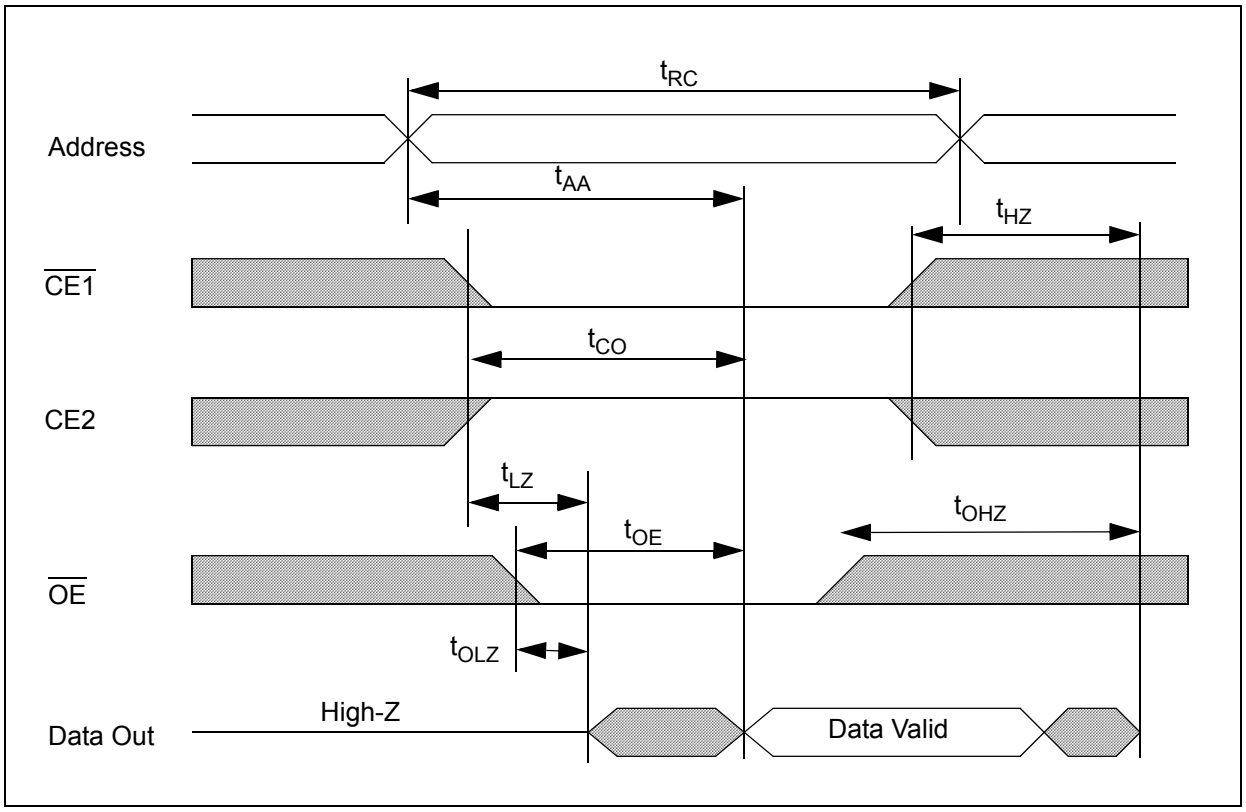
Timing

Item	Symbol	2.3 - 3.6 V		2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70		55		ns
Address Access Time	t_{AA}		70		55	ns
Chip Enable to Valid Output	t_{CO}		70		55	ns
Output Enable to Valid Output	t_{OE}		35		30	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	15	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	15	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	70		55		ns
Chip Enable to End of Write	t_{CW}	50		45		ns
Address Valid to End of Write	t_{AW}	50		45		ns
Write Pulse Width	t_{WP}	40		32.5		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		15	ns
Data to Write Time Overlap	t_{DW}	40		30		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

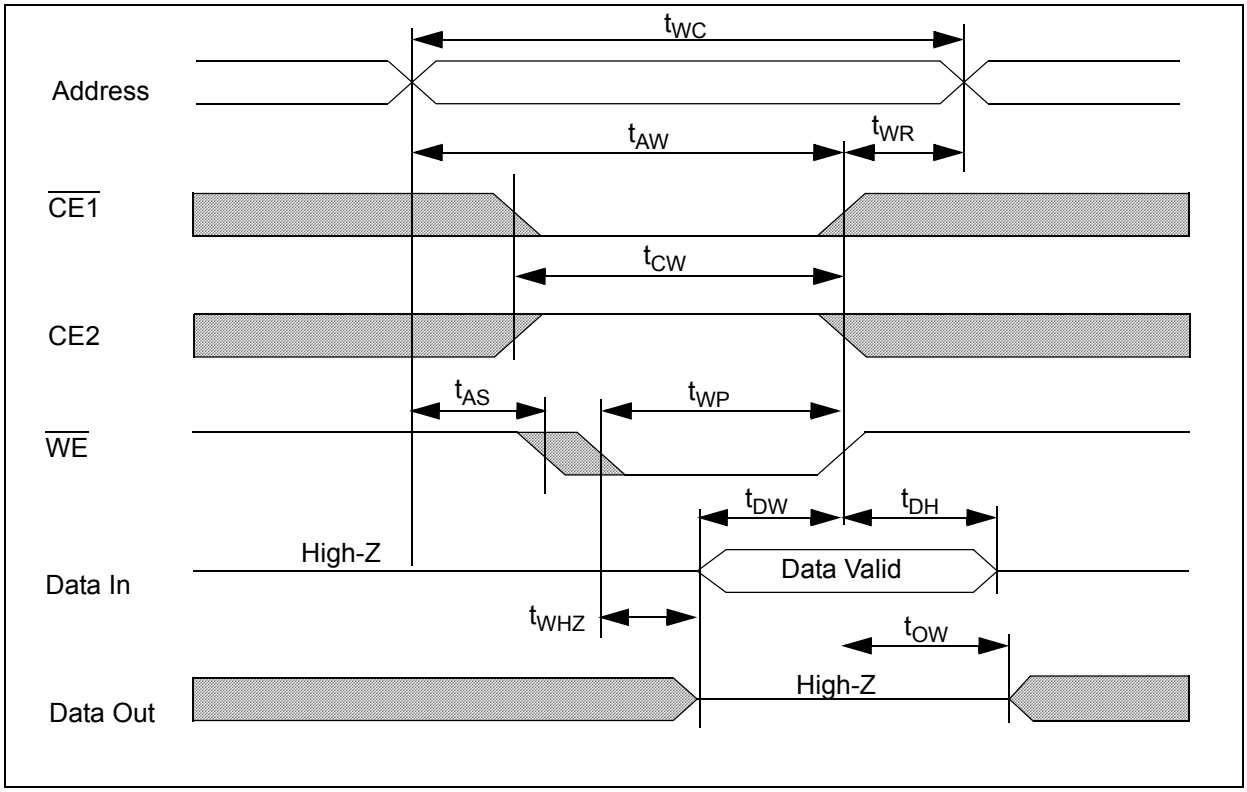
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



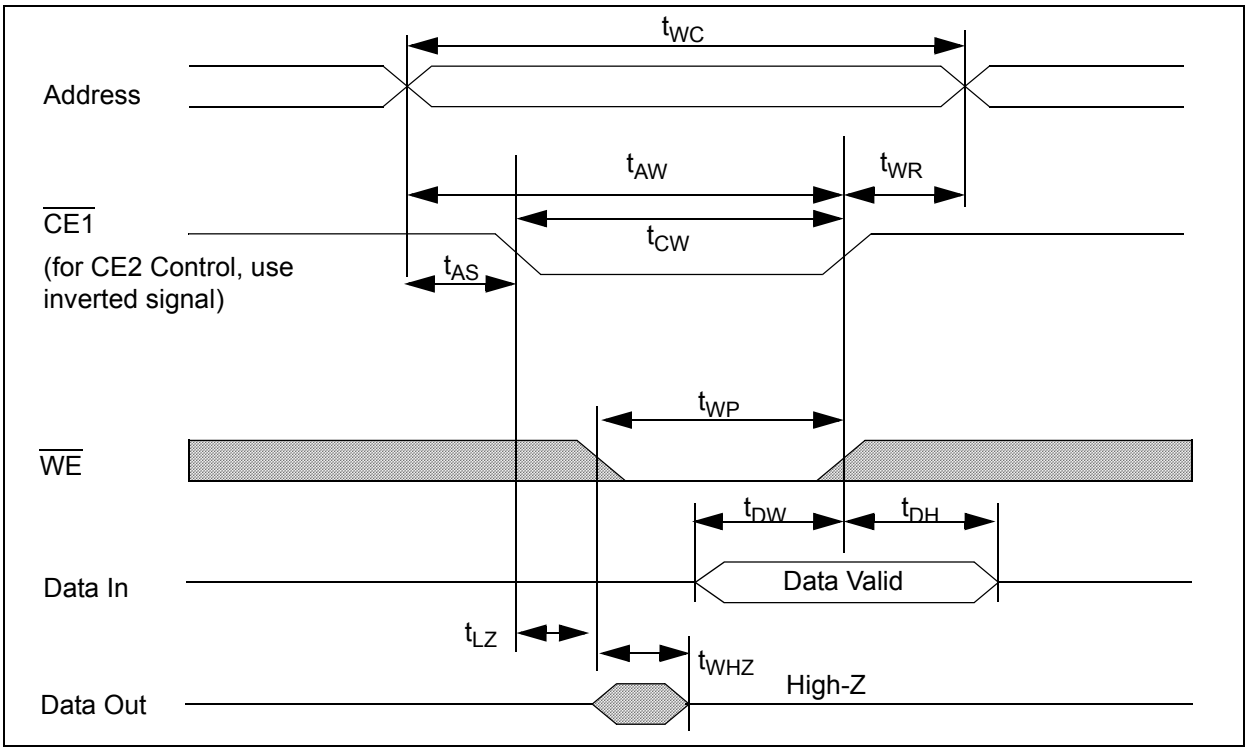
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



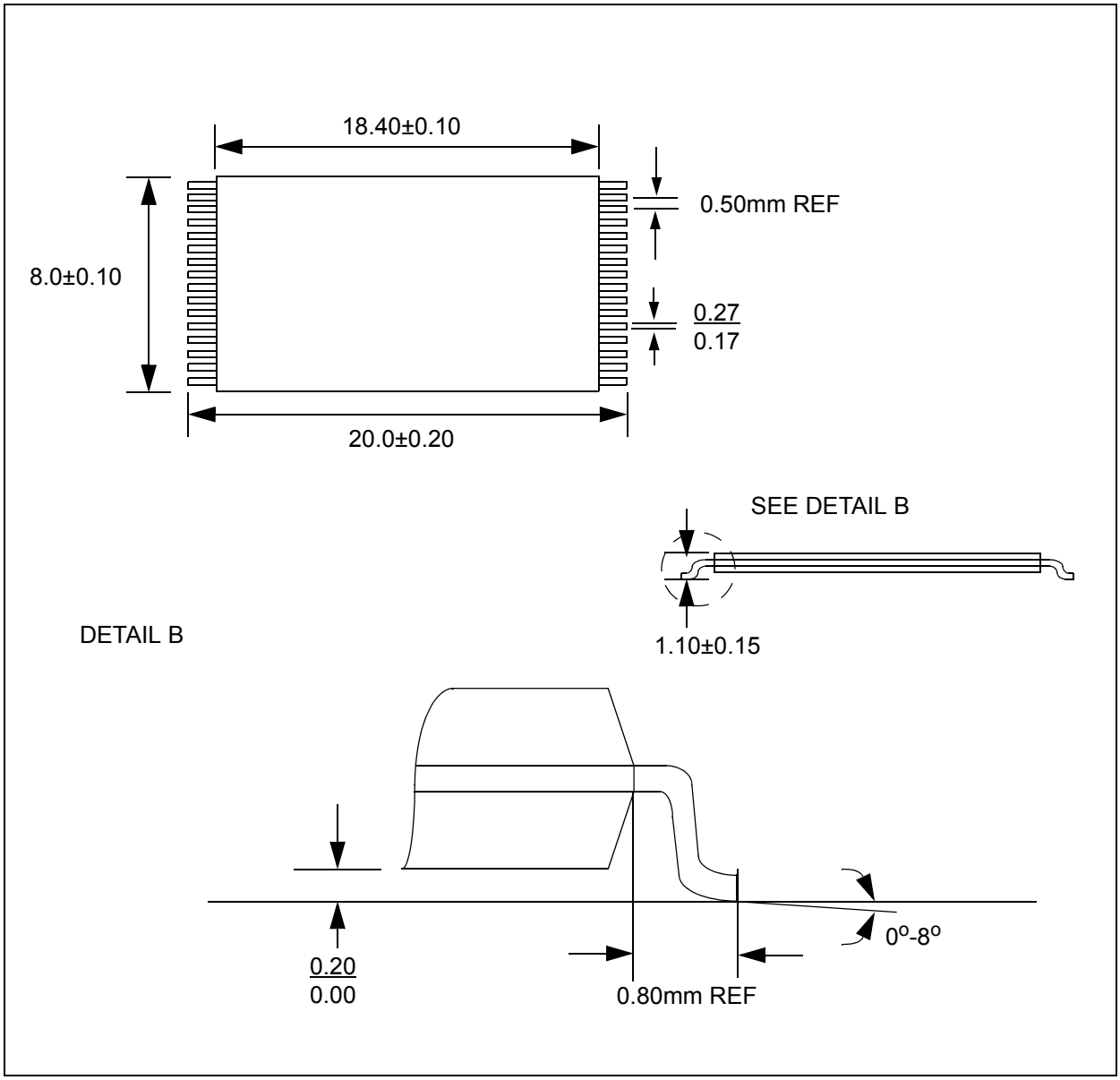
Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)

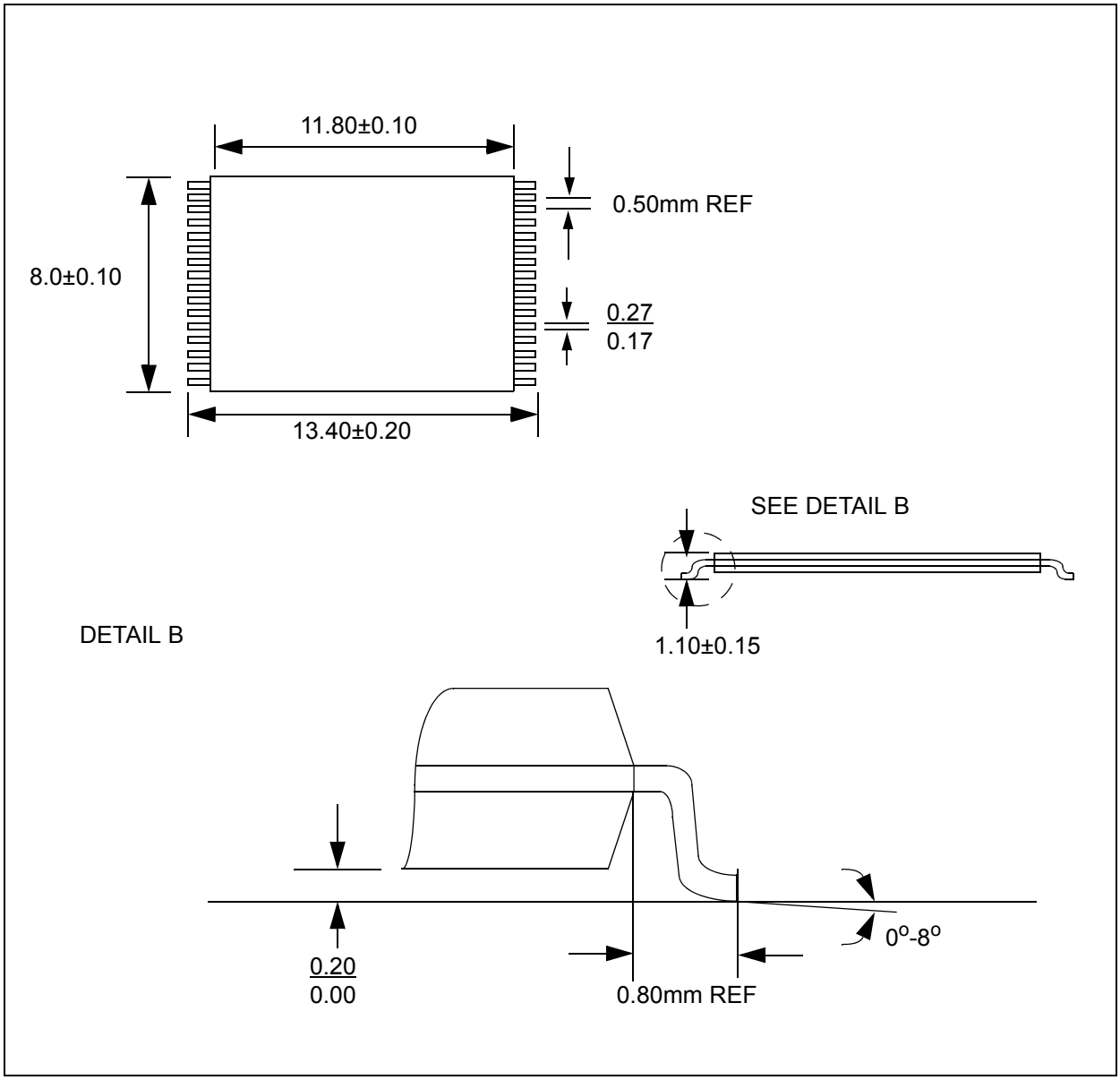


32-Lead TSOP-I Package (T32)



Note:
1. All dimensions in millimeters
2. Package dimensions exclude molding flash

32-Lead STSOP-I Package (N32)



Note:
1. All dimensions in millimeters
2. Package dimensions exclude molding flash

Ordering Information

Part Number	Package	Shipping Method
N01L83W2AT5I	Leaded 32-TSOP I	Tray
N01L83W2AT25I	Green 32-TSOP I	Tray
N01L83W2AN5I	Leaded 32-sTSOP I	Tray
N01L83W2AN25I	Green 32-sTSOP I	Tray
N01L83W2AT5IT	Leaded 32-TSOP I	Tape & Reel
N01L83W2AT25IT	Green 32-TSOP I	Tape & Reel
N01L83W2AN5IT	Leaded 32-sTSOP I	Tape & Reel
N01L83W2AN25IT	Green 32-sTSOP I	Tape & Reel

Revision History

Revision #	Date	Change Description
A	Jan 2001	Initial Advance Release
B	Mar 2001	Added Table 3: Capacitance. Revised quiescent operating current, changed pin 31 to CE1, modified Pin Description and Pin Configuration, other minor edits
C	Dec. 2001	Part number change from EM128L08, modified Overview and Features, added Page Mode Operation diagram and Package diagrams, revised Operating Characteristics table, Functional Description table, Timing diagrams, and Ordering Information diagram
D	Nov. 2002	Replaced Isb and Icc on Product Family table with typical values
E	Dec. 2002	Add 32-pin SOP package
F	Aug, 2004	Changed tWP to 32.5ns and tDW to 30ns for 55ns sort
G	Oct, 2004	Added Green Package Option
H	Dec. 2005	Added RoHS Compliant
I	September 2006	Converted to AMI Semiconductor
10	July 2008	Converted to ON Semiconductor and new part numbers

PUBLICATION ORDERING INFORMATION

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