REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make corrections to the dimension “b” minimum and nominal limits as specified under figure 1 case outline X. - ro	18-08-01	C. SAFFLE

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
17-09-12

MICROCIRCUIT, DIGITAL-LINEAR, DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-16211**

SHEET 1 OF 26

DSCC FORM 2233
APR 97

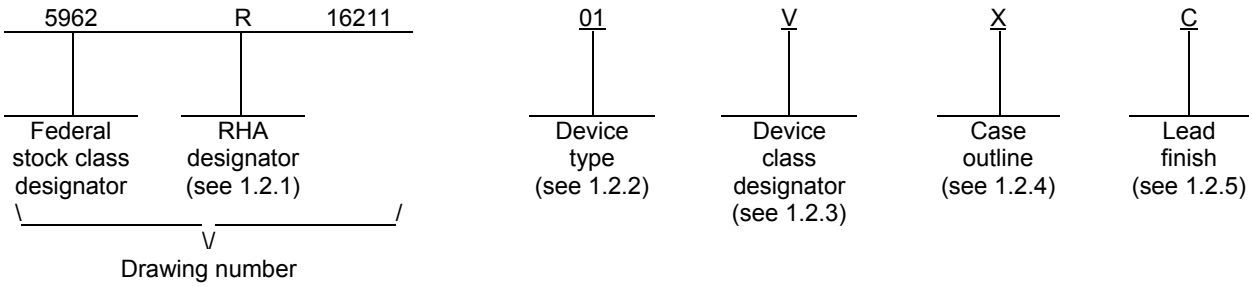
5962-E524-18

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHRDAC1612	Radiation hardened high resolution digital to analog converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	24	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Analog supply voltage (AV_{CC})	4.5 V
Digital supply voltage (DV_{CC})	4.5 V
Digital buffer supply voltage (IOV_{CC})	4.5 V
Analog inputs (V_{IN_Ana})	-0.3 V to AV_{CC} + 0.3 V
Digital inputs (V_{IN_Dig})	-0.3 V to IOV_{CC} + 0.3 V
Digital output current (I_{DOUT})	-10 mA to 10 mA
Continuous current is ESD diode (I_{ESD} diode)	10 mA
Maximum power dissipation (P_D) at T_A = +125°C	0.4 W
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	150°C
Lead temperature (soldering, 10 seconds)	260°C
Thermal resistance, junction-to-case (θ_{JC})	22°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	60°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HDM)	2 kV 2/

1.4 Recommended operating conditions.

Analog supply voltage (AV_{CC})	3 V to 3.6 V
Digital supply voltage (DV_{CC})	3 V to 3.6 V
Differential voltage (AV_{CC} – DV_{CC})	-0.2 V to 0.2 V
Input/output (I/O) supply voltage (IOV_{CC})	1.6 V to DV_{CC}
Differential voltage (DV_{CC} – IOV_{CC})	0 V to 2 V
External reference voltage (V_{REF})	1 V to 1.4 V
Digital input voltage low level (V_{IL})	0 V to 0.4 V
Digital input voltage high level (V_{IH})	0.8 x IOV_{CC} to IOV_{CC}
Digital output voltage low level with 1 mA sink current (V_{OLD})	0 V to 0.4 V
Digital output voltage high level with 1 mA source current (V_{OHD})	IOV_{CC} – 0.4 V to IOV_{CC}
Internal master clock (MCLK)	2.4 MHz to 3.6 MHz
External master clock (MCLKI)	2.4 MHz to 3.6 MHz
External master clock duty cycle	40% to 60%
External master clock jitter, bench evaluation	100 ps
Capacitance load guaranteed be design, stability, noise (C_L)	100 pF to 200 pF
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

1.5 Radiation features.

Maximum total dose available (dose rate = 60 mrad(Si)/s) ..... 100 krad(Si) 3/

Single event phenomenon (SEP) :

No single event latch up (SEL) effective LET (see 4.4.4.2) ..... ≤ 120 MeV/(mg/cm^2) 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

JEDEC Solid State Technology Association

JEDEC JEP 163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

3/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. However, radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition C as agreed by the users and manufacturers. Where the final user is not known, the test conditions and results shall be made available in the test report with each purchase order.

4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing diagrams. The timing diagrams shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current consumption on AV_{CC}	I_{CCA}	PDN = ARSTN = IOV_{CC}	1,2,3	01		4.7	mA
Current consumption on 3/ DV_{CC}	I_{CCD}	PDN = ARSTN = IOV_{CC}	1,2,3	01		750	µA
Current consumption on 4/ 5/ IOV_{CC} internal clock	I_{CCIO}	PDN = ARSTN = CS = IOV_{CC}	1,2,3	01		10	µA
Total current consumption in standby mode	$I_{CCSTDBY}$	PDN = 0.4 V, ARSTN = CS = IOV_{CC}, Ext MCLK = OFF	1,2,3	01		200	µA
Internal power on reset threshold levels	POR level	V_{CC} increasing	1,2,3	01	2.02	2.3	V
		V_{CC} decreasing			1.7	2	
Between AV_{CC} and V_{REFOUT}	RON1		4,5,6	01	30	70	Ω
Between AV_{CC} and $V_{REFBOOST}$	RON2		4,5,6	01	200	350	Ω
Between $V_{REFBOOST}$ and V_{REFIN}	RON3		4,5,6	01	30	70	Ω
Low output rail on 10 kΩ load connected to GND	Vmin		1,2,3	01		12	mV
Output load regulation with 100 µA output sink current	LRsink	V_{OUT} = 1.2 V (middle code), LSB = 36.6 µV	1,2,3	01		+4.1	LSB
Output load regulation with 1 mA output source current	LRsource	V_{OUT} = 1.2 V (middle code), LSB = 36.6 µV	1,2,3	01		+4.1	LSB
Gain error	GE	V_{REF} = 1.2 V	4,5,6	01	-0.75	-0.35	%
Offset error 6/ (After a calibration sequence)	Oe	V_{REF} = 1.2 V, LSB = 36.6 µV	1,2,3	01	-4.1	+4.1	LSB
Integral non-linearity (Guarantee by distortion measurement)	INL	V_{REF} = 1.2 V, LSB = 36.6 µV	4,5,6	01	-4.5	+4.5	LSB

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Noise level	N	V_{REF} = 1.2 V, T_A = +25°C, BW = 10 Hz to 3 kHz	1	01		19	µVrms
Spectral noise density at 1 kHz	e_n	V_{REF} = 1.2 V, T_A = +25°C	1	01		345	nV/VHz
Output signal to noise ratio	SNR	V_{REF} = 1.2 V, T_A = +25°C, BW = 10 Hz to 3 kHz, sine 64 Hz and -1 dBFS	4	01	93		dB
Spurious free dynamic range	SFDR	V_{REF} = 1.2 V, BW = 10 Hz to 3 kHz, sine 64 Hz and -1 dBFS	4,5,6	01	89.5		dBc
Total harmonic distortion H2 =	THD	V_{REF} = 1.2 V, BW = 10 Hz to 3 kHz, sine 64 Hz and -1 dBFS	4,5,6	01		-89.5	dBc
Total harmonic distortion H3 =	THD	V_{REF} = 1.2 V, BW = 10 Hz to 3 kHz, sine 64 Hz and -1 dBFS	4,5,6	01		-100	dBc
Master clock divided by OSR (OSR = 256)	SYNC OUT freq	Internal MCLK	4,5,6	01	9.6	14.4	kHz
		External MCLK			9.6	14.4	
Sync out pulse duration 7/ 8/ tpulse = 8/MCLKx	SYNC OUT pulse	Internal MCLK	9,10,11	01	2.2	3.32	µs
		External MCLK			2.2	3.32	
DAC sample rate (MCLK/256)	Sample rate	Internal MCLK	4,5,6	01	9.6	14.4	ksps
		External MCLK			9.6	14.5	
Input reference current	Iref	Vref = 1 V to 1.4 V	1,2,3	01		1	µA
Wake up time 8/ 9/ (during CALT, the DAC cannot be used)	TWU	10/	9,10,11	01	230	440	ms
Calibration time 8/ (during CALT, the DAC cannot be used)	CALT	11/	9,10,11	01		40	ms

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 12/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics.		See figure 3.					
Internal POR high level to ARSTN high level threshold.	t1	8/	9,10,11	01	100		µs
ARTN high level threshold to PDN high level threshold	t2	8/	9,10,11	01	50		µs
PDN high level threshold to CS low level threshold	t3	8/	9,10,11	01	1		ms
PDN high level threshold to stable output voltage without any SPI commands	t4	8/	9,10,11	01	230	480	ms
CS high level threshold to effective output voltage change	t5	8/	9,10,11	01		5500/ MCLK	s
PDN low level threshold to effective high Z output	t6	8/	9,10,11	01		5	ms
Internal POR low level to effective high Z output (to do with PDN falling before)	t7	8/	9,10,11	01		5	ms
PDN high level threshold to effective SYNC OUT signal ON	t8	8/	9,10,11	01		490	ms
PDN low level threshold to effective SYNC OUT signal OFF	t9	8/	9,10,11	01		10	ms
ARSTN low level threshold to SYNC OUT signal OFF	t10	8/	9,10,11	01		100	µs
PDN high level threshold to first calibration sequence	t11	8/	9,10,11	01	t4 max + 100 µs		ms
MCLK OFF before PDN high level threshold	t12	8/	9,10,11	01		500	µs
MCLK ON after PDN low level threshold	t13	8/	9,10,11	01	500		µs
PDN pulse width low	t14	8/	9,10,11	01	20		ms
ARSTN pulse width low	t15	8/	9,10,11	01	1		ms

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 12/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.		See figure 3.					
CS low level threshold to rising edge of SCLK	t16	8/	9,10,11	01	1		µs
Data setup time	t17	8/	9,10,11	01	25		ns
Data hold time	t18	8/	9,10,11	01	25		ns
SCLK period	t19	8/	9,10,11	01	125		ns
SCLK low time	t20	8/	9,10,11	01	50		ns
SCLK high time	t21	8/	9,10,11	01	50		ns
SCLK rising edge to CS high level threshold	t22	8/	9,10,11	01	1		µs
Minimum CS time at high level	t23	8/	9,10,11	01	5		µs
SDOUT setup time	t24	8/	9,10,11	01	25		ns
SDOUT hold time	t25	8/	9,10,11	01	25		ns
V_{CCA}, DV_{CC}, IOV_{CC} positive slew rate	t26	8/	9,10,11	01	300	0.003	V/ms
Delay between POR high level to AV_{CC} minimum value	t27	8/	9,10,11	01	0	100	ms
Delay between AV_{CC} minimum value to IOV_{CC} minimum value	t28	8/	9,10,11	01	0	100	ms
V_{CCA}, DV_{CC}, IOV_{CC} negative slew rate	t29	8/	9,10,11	01	300	0.003	V/ms
Delay between POR low level to DV_{CC} = 0.5 V	t30	8/	9,10,11	01	0	100	ms
Delay between POR low level to IOV_{CC} = 0.5 V	t31	8/	9,10,11	01	0	100	ms

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ Device type 01 has been characterized through all levels M, D, P, L, R of irradiation. However, this device is tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Unless otherwise specified, AV_{CC} = DV_{CC} = 3 V to 3.6 V, IOV_{CC} = 1.6 V to 3.6 V, EXT MCLKIN = 3.072 MHz, external V_{REF} = 1.2 V, and C_L = 100 pF.

3/ In case of external master clock, ICCD is divided by 2.

4/ If PDN connected to IOVCC pin, add IH current.

5/ In case of external master clock, add 20 μA to 30 μA to I_{CCIO}.

6/ Due to internal ADC LSB value calibration sequencer, after each calibration a difference of about 20 μV to 30 μV can be observed.

7/ Guaranteed by design.

8/ Post irradiation test measurement is not performed, however this parametric limits are guaranteed by characterization.

9/ Settling time of analog output filter is not taken into account.

10/ Add calibration time (CALT) for the total wake up (TWU) time.

11/ Tested during offset error test by applying a calibration time lower than the maximum time specified.

12/ Unless otherwise specified, AV_{CC} = DV_{CC} = 3 V to 3.6 V and IOV_{CC} = 1.6 V to 3.6 V.

TABLE IB. SEP test limits. 1/ 2/

Device type	Bias V_{DD} = 3.6 V for Single event latch-up (SEL) test No SEL occurs at effective LET
01	LET ≤ 120 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

Case X

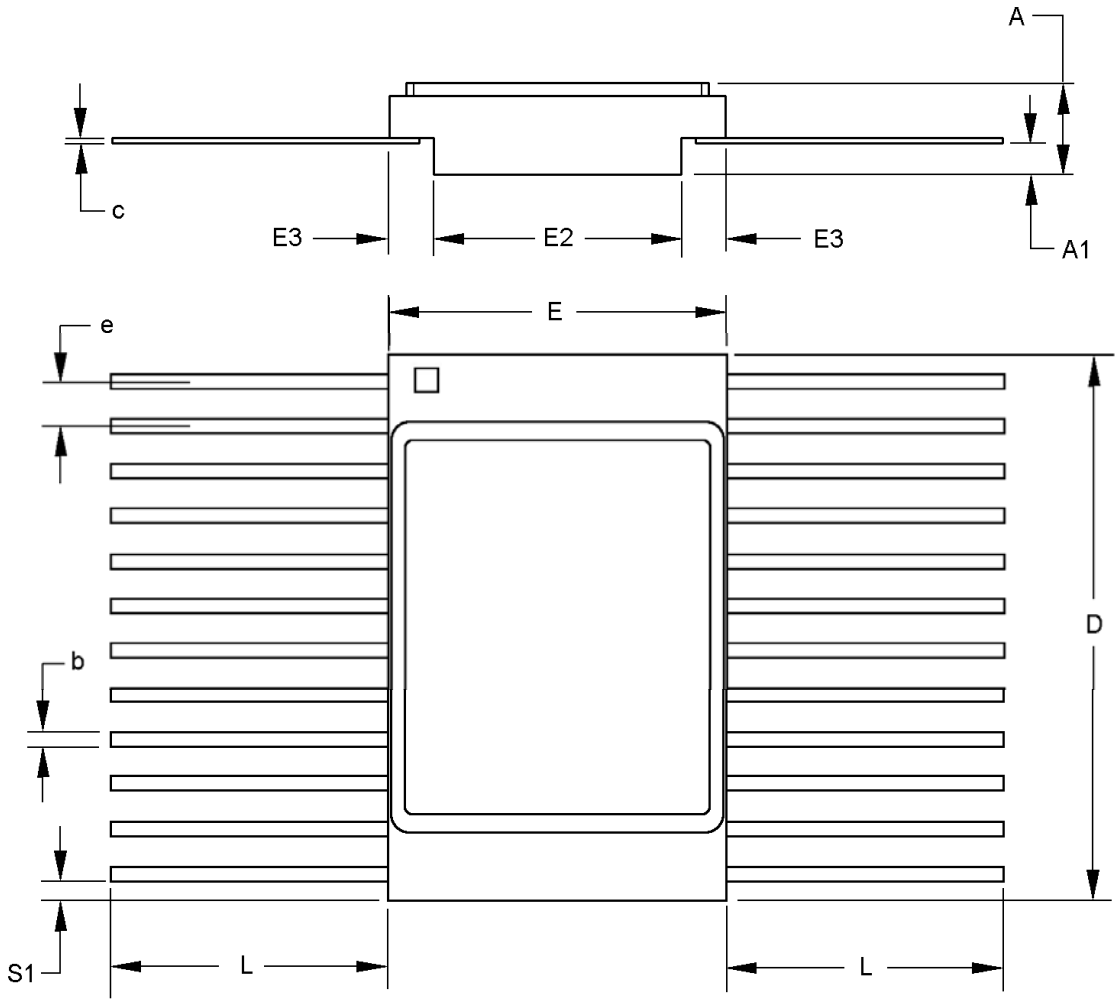


FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.091	.100	.109	2.31	2.54	2.77
A1	.026	---	.045	0.66	---	1.14
b	.013	.015	.019	0.33	0.38	0.48
c	.004	.005	.006	0.1	0.125	0.15
D	.604	.610	.616	15.34	15.49	15.64
E	.375	---	.385	9.52	---	9.78
E2	.274	---	.285	6.96	---	7.26
E3	---	.050	---	---	1.27	---
e	---	.050	---	---	1.27	---
L	.25	---	.37	6.35	---	9.4
S1	---	.005	---	---	0.13	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The upper metallic lid is electrically connected to DGND pin.

FIGURE 1. Case outline.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
1	PDN	Digital	Power down (active low) + internal pull down current source.
2	SDOUT	Digital	SPI data output + external pull down resistor of 33 kΩ.
3	SDIN	Digital	SPI data input + internal pull down current source.
4	SCLK	Digital	SPI clock input + internal pull down current source.
5	CS	Digital	Chip select and SPI synchronization + internal pull up current source.
6	SYNC OUT	Digital	Master clock divided by OSR low level during TWU.
7	TESTD	Digital	Digital test input. Must be connected to GND.
8	DGND	Power	Digital ground.
9	IOV_{CC}	Power	IO power supply.
10	MCLKIN	Digital	Master clock input. When not used, this input must be connected to DGND.
11	ASTRN	Digital	Asynchronous rest (active low) + internal pull up current source.
12	DV_{CC}	Power	Digital power supply.
13	VREFOUT	Analog	External voltage reference output power supply.
14	VREFBOOST	Analog	External voltage reference boost current.
15	TESTA	Analog	Analog test pin. Must be left floating.
16	VREFIN	Analog	External voltage reference input.
17	AV_{CC}	Power	Analog power supply.
18	AGND	Power	Analog ground.
19	Ca	Analog	Filter I/O.
20	Cb	Analog	Filter I/O.
21	Cc	Analog	Filter I/O.
22	Cd	Analog	Filter I/O.
23	OFB	Analog	Output feedback.
24	OUT	Analog	Analog buffered/filtered single ended output.

FIGURE 2. Terminal connections.

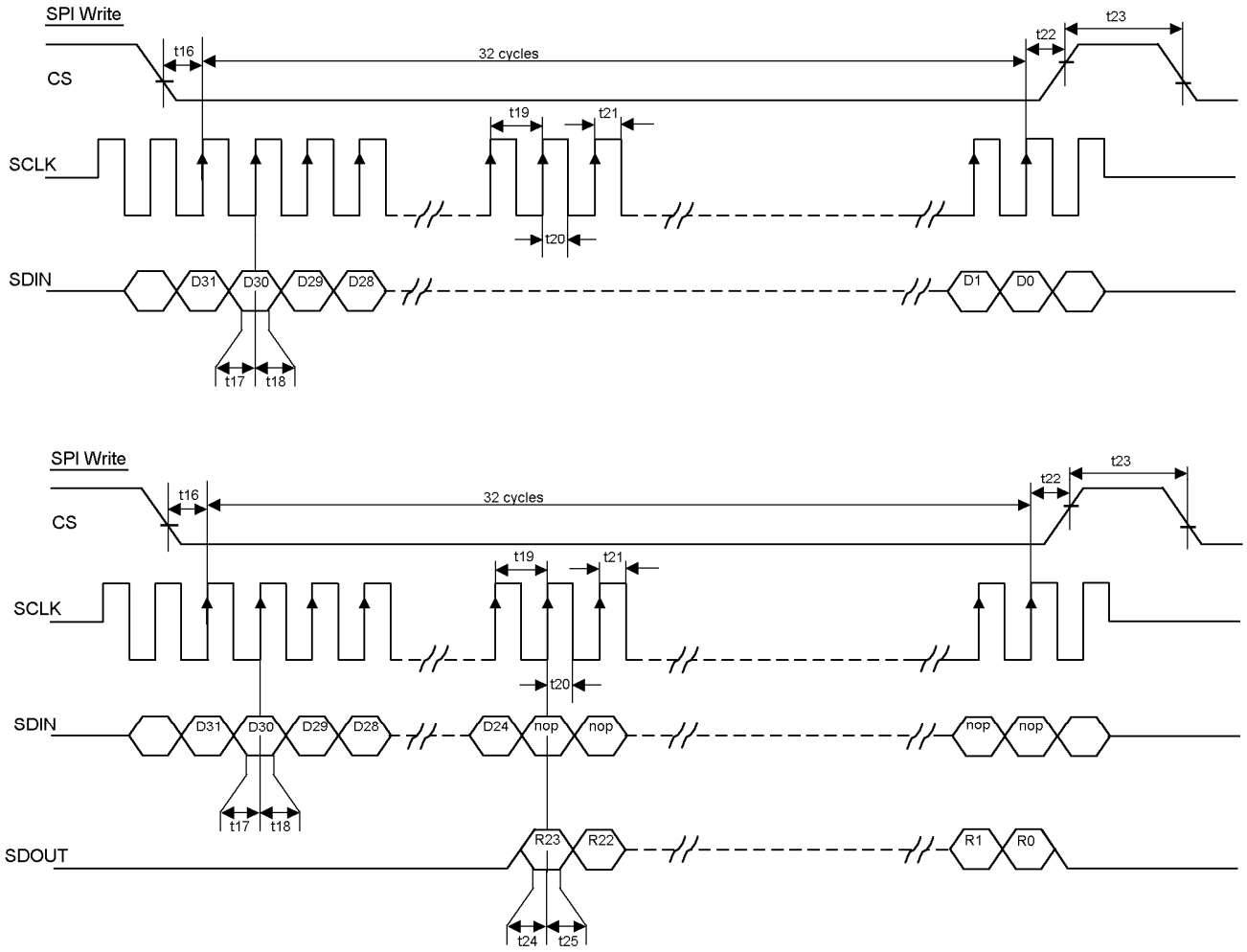


FIGURE 3. Timing waveforms.

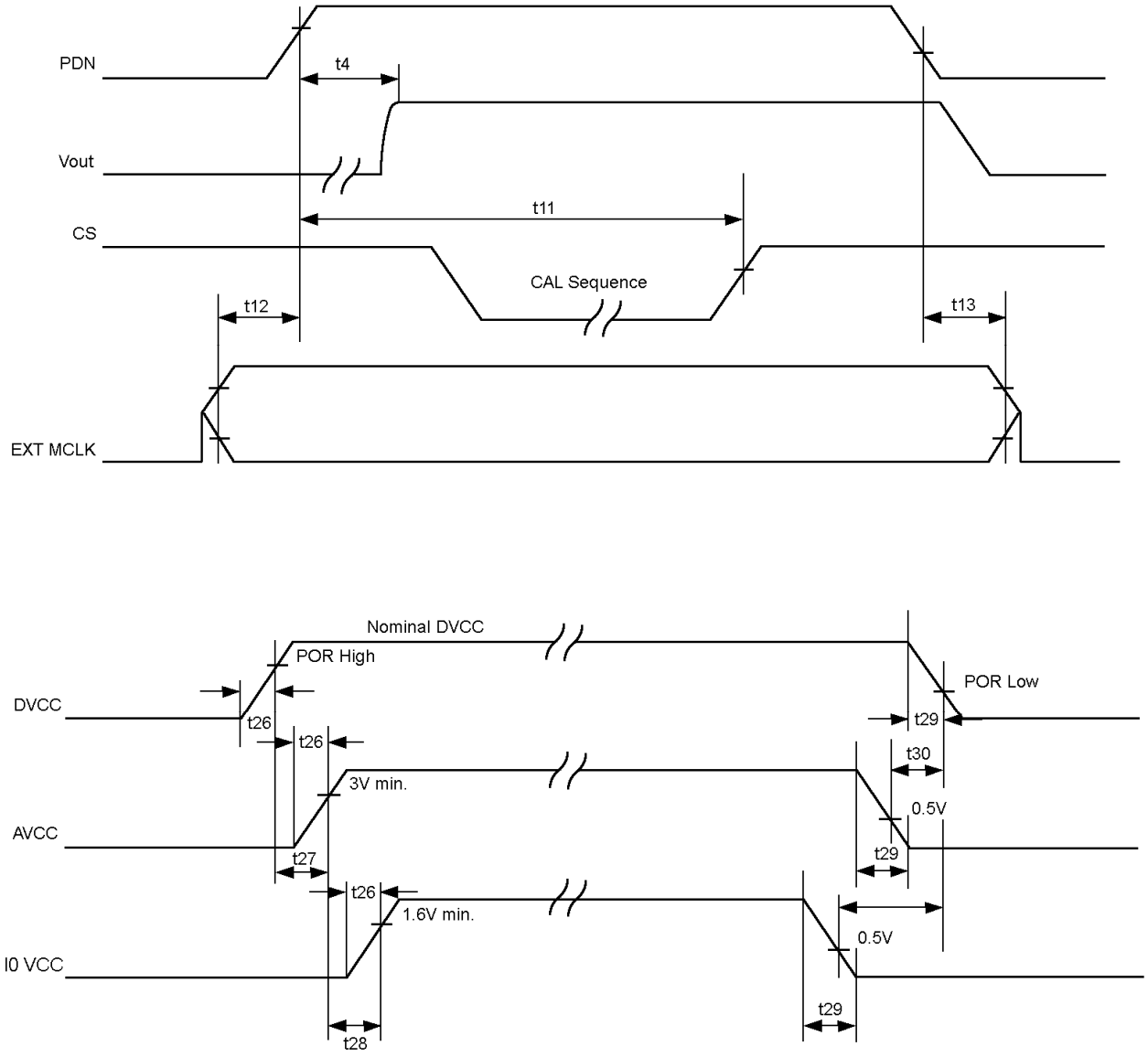


FIGURE 3. Timing waveforms - continued.

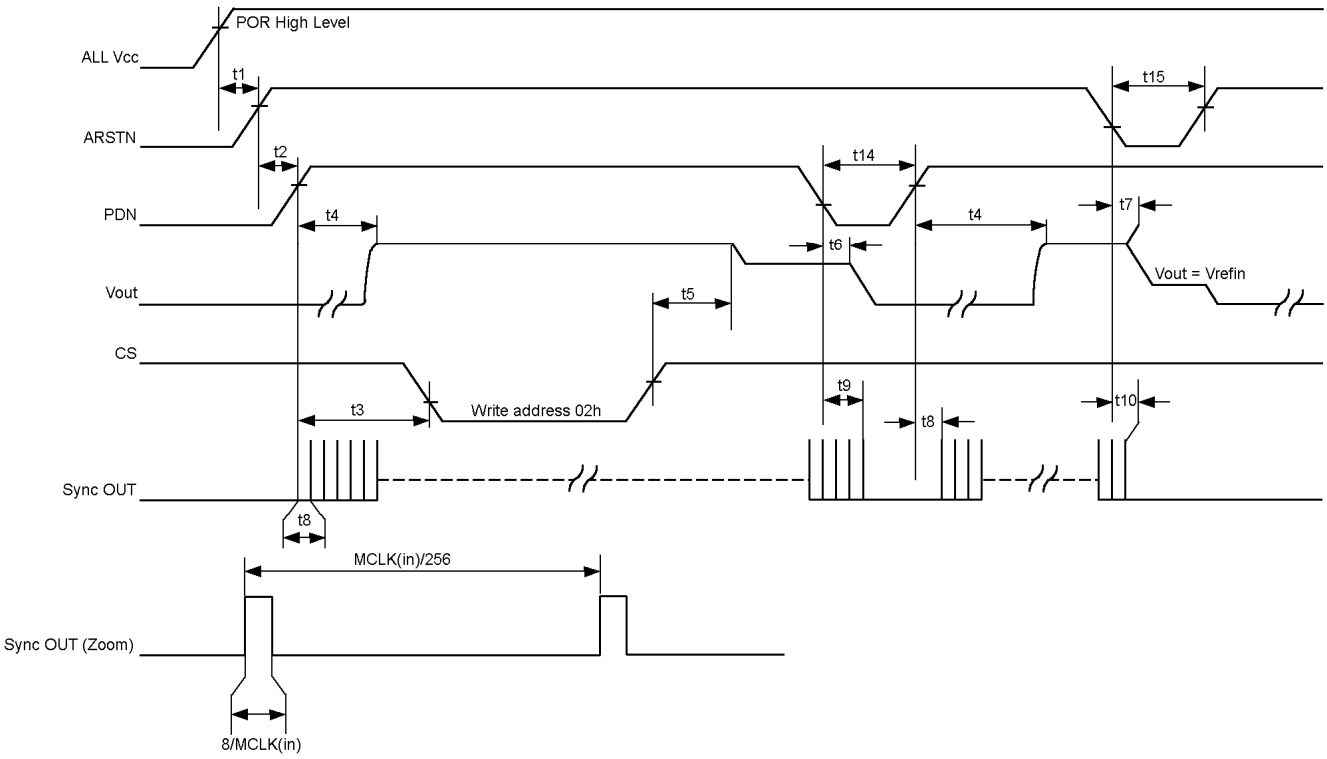


FIGURE 3. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535 and JEDEC JEP163. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

c. For devices class V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V, shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters subgroups shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters subgroups shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups Group A (electrical test) table III (in accordance with MIL-PRF-38535)	
	Device class Q	Device class V
Interim (pre burn-in) electrical parameters, (see 4.2)	1, 9 1/	1, 9 1/ 2/
Dynamic burn-in (see 4.2.1)	Required 3/	Required 4/
Post burn-in electrical parameters (see 4.2.1)	1, 9 1/	1, 9 1/ 2/
Group A (Final electrical) test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 9 10, 11	1, 2, 3, 4, 5, 6, 9 10, 11
Group C end-point electrical parameters, (see 4.4.2)	1, 2, 3, 4, 5, 6, 9 10, 11	1, 2, 3, 4, 5, 6, 9 10, 11
Group D end-point electrical parameters, (see 4.4.3)	1, 2, 3, 4, 5, 6, 9 10, 11	1, 2, 3, 4, 5, 6, 9 10, 11
Group E (RHA) end-point electrical parameters,(see 4.4.4)	1, 4	1, 4

1/ PDA applies to subgroup 1 (see 4.2). For device class V (class level S) PDA applies to subgroup 1 (see 4.2.1).
2/ For device class V (class level S): 100 percent of the devices shall be tested. Pre and post burn-in test results shall be read and recorded for those parameters requiring delta calculations. Delta parameters shall be specified in table IIB.
3/ The burn-in configuration, either static or dynamic burn-in test shall be performed per method 1015 with test condition A or B or C or D (see MIL-PRF-38535 and JEDEC JEP163).
4/ For device class V (class level S): If the device operates in a dynamic mode, then dynamic burn-in test shall be performed per method 1015 with test condition D (see MIL-PRF-38535 and JEDEC JEP163).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters 1/ 2/	Symbol	Conditions	Limit
Current consumption on IOV_{CC} internal clock	I_{CCIO}		±2 μA
Current consumption on AV_{CC}	I_{CCA}		±200 μA
Current consumption on DV_{CC}	I_{CCD}		±20 μA
Total current consumption in standby mode	I_{CC} stdby		±25 μA

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

2/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall be corresponding to the test defined in table IA (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table IA.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition C and as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (for example: 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the transient measurements and the maximum rated operating temperature ±10°C for the latchup measurements.

f. Bias conditions shall be V_{CC} = V_{CC} maximum for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

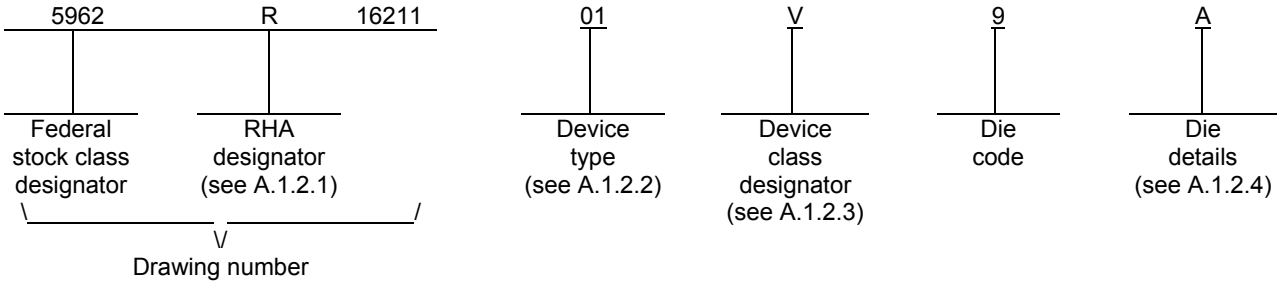
b. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-16211

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHRDAC1612	Radiation hardened high resolution digital to analog converter

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

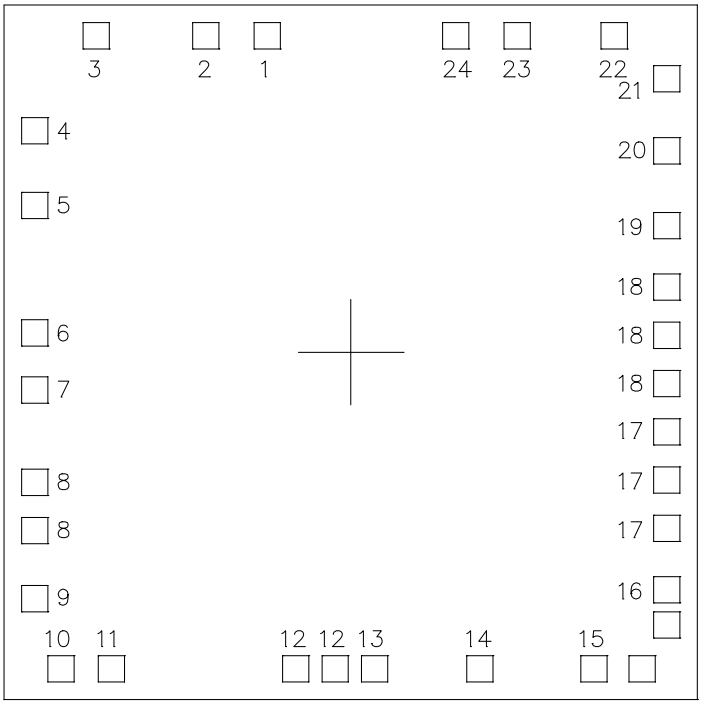
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Die physical dimensions.

Die size: 2100 µm x 2100 µm
Die thickness: 525 (± 10 µm)

Interface materials.
Top metallization: Metal 1 TaN/Ta/Cu = 0.250 µm
Metal 2 TaN/Ta/Cu = 0.350 µm
Metal 3 TaN/Ta/Cu = 0.350 µm
Metal 4 TaN/Ta/Cu = 0.900 µm
Metal 5 AlCu = 1.2 µm (TOP)

Backside metallization: raw silicon – back grinding

Glassivation.
Type: PSG + Nitride
Thickness: 1.1 µm

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: tied to V_{SS}
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

Die pad	Pad symbol	Pad placements	
		X	Y
3	SDIN	-772.03	949.31
2	SDOUT	-442.39	949.31
1	PDN	-271.83	949.31
24	OUT	283.31	949.31
23	OFB	453.87	949.31
22	CD	783.51	949.31
21	CC	949.31	808.13
20	CB	949.31	558.85
19	CA	949.31	334.17
18	AGND	949.31	157.41
18	AGND	949.31	18.41
18	AGND	949.31	-122.59
17	AVCC	949.31	-285.52
17	AVCC	949.31	-431.75
17	AVCC	949.31	-572.75
16	VREF IN	949.31	-769.55
	NOT CONNECTED	949.31	-861.39
	NOT CONNECTED	853.23	-949.31
15	TESTA	708.91	-949.31
14	VREF BOOST	379.27	-949.31
13	VREF OUT	51.27	-949.31
12	DVCC GUARD	-55.33	-949.31
12	DVCC	-165.21	-949.31
11	ARSTN	-724.37	-949.31
10	MCLKIN	-870.33	-949.31
9	IOVCC	-949.31	-692.51
8	DGNDS	-949.31	-491.61
8	DGND	-949.31	-360.41
7	SCAN EN	-949.31	-84.89
6	SYNC OUT	-949.31	85.67
5	CS	-949.31	441.55
4	SCLK	-949.31	664.59

NOTES:
1. Units are in μm. Number of pads: 32.
2. Minimum pad area (X*Y): 4720.0. Minimum pad value in X: 59.0. Minimum pad value in Y: 80.0.

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-08-01

Approved sources of supply for SMD 5962-16211 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1621101VXA	F8859	RHRDAC1612K02V
5962R1621101VXC	F8859	RHRDAC1612K01V
5962R1621101V9A	F8859	RHRDAC1612D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	STMicroelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.