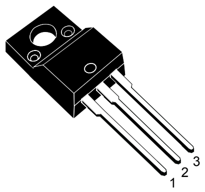
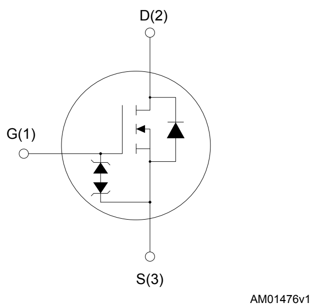
STFU13N80K5

Datasheet

N-channel 800 V, 370 mΩ typ., 12 A MDmesh K5 Power MOSFET in a TO-220FP ultra narrow leads package



TO-220FP
ultra narrow leads



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STFU13N80K5	800 V	450 mΩ	12 A

- Ultra-low gate charge
- Very low FoM (figure of merit)
- Zener-protected
- 100% avalanche tested

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STFU13N80K5

Product summary	
Order code	STFU13N80K5
Marking	13N80K5
Package	TO-220FP ultra narrow leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	800	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	12	A
	Drain current (continuous) at T_C = 100 °C	7.6	
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at T_C = 25 °C	35	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 12 A, di/dt = 100 A/μs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 640 V.*
3. *V_{DD} ≤ 640 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	3.57	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	148	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C[1]	-	-	50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A	-	370	450	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	870	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}$[1]	Equivalent output capacitance time related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	110	-	pF
$C_{o(er)}$[2]	Equivalent output capacitance energy related		-	43	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 12 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	29	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	16	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	14	A
I_{SDM} [1]	Source-drain current (pulsed)		-	-	56	A
V_{SD} [2]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	406	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	5.7	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	28	-	A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	600	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	7.9	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	26	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

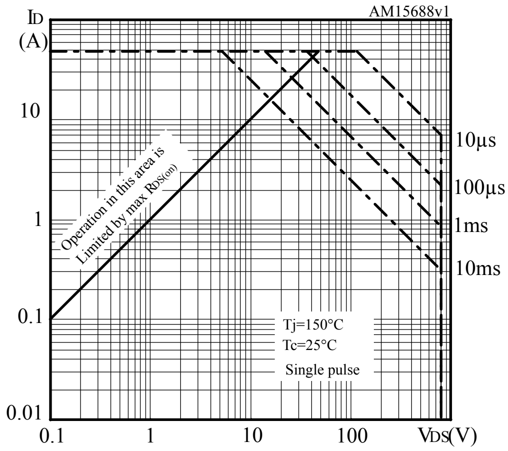


Figure 2. Normalized transient thermal impedance

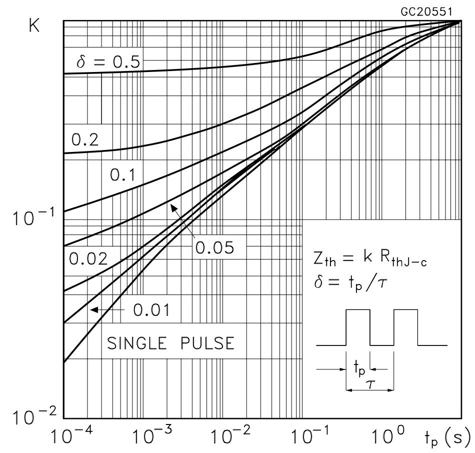


Figure 3. Typical output characteristics

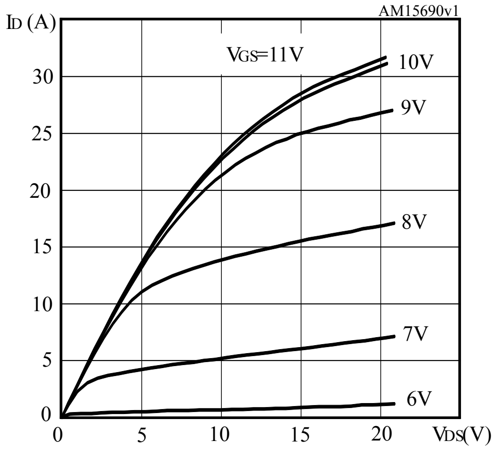


Figure 4. Typical transfer characteristics

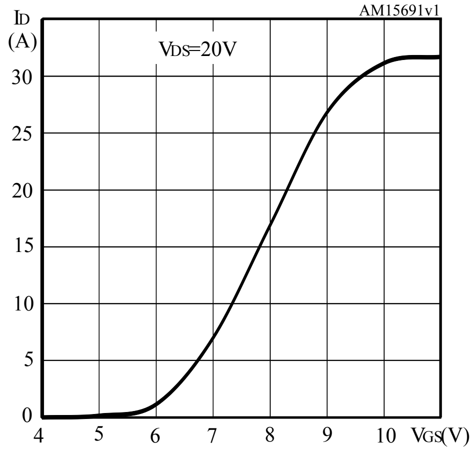


Figure 5. Typical gate charge characteristics

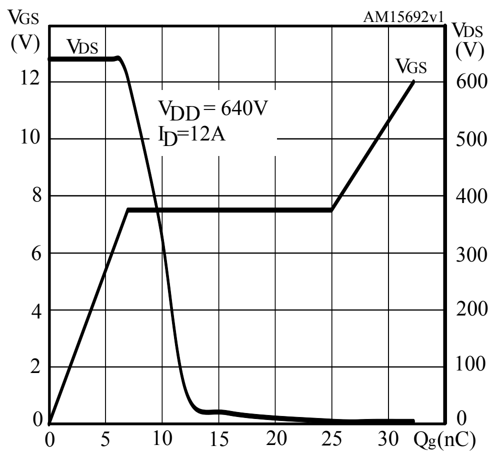


Figure 6. Typical drain-source on-resistance

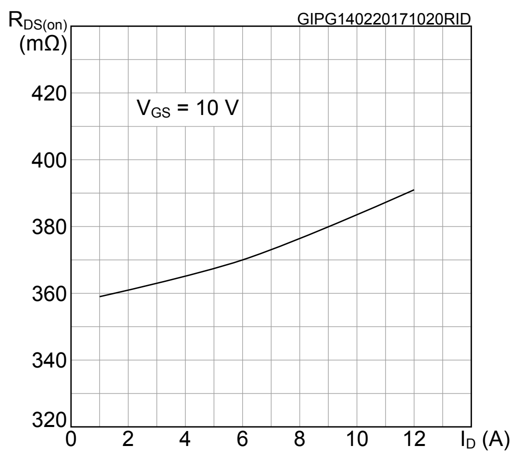


Figure 7. Typical capacitance characteristics

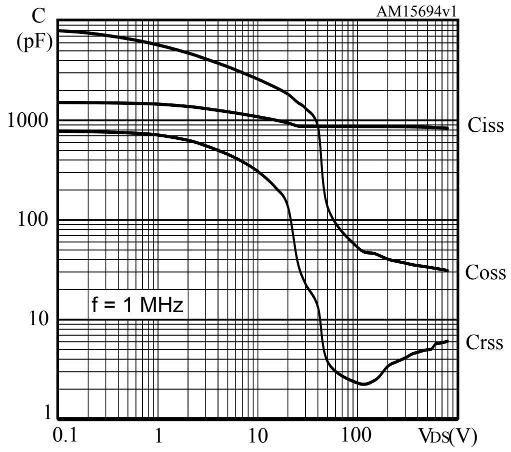


Figure 8. Typical output capacitance stored energy

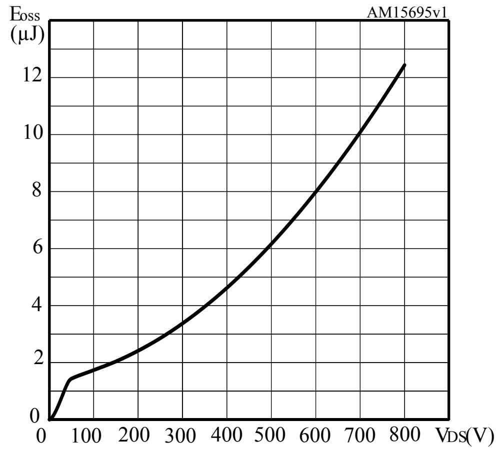


Figure 9. Normalized gate threshold vs temperature

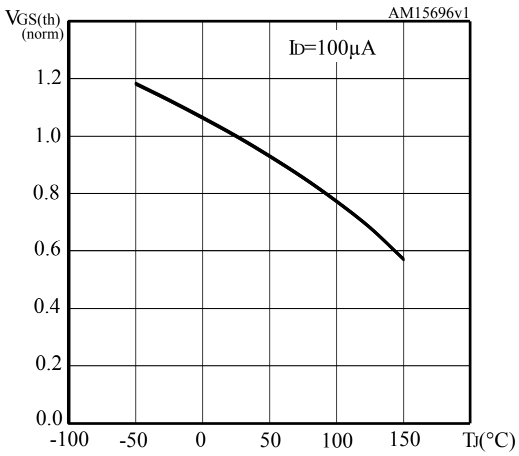


Figure 10. Normalized on-resistance vs temperature

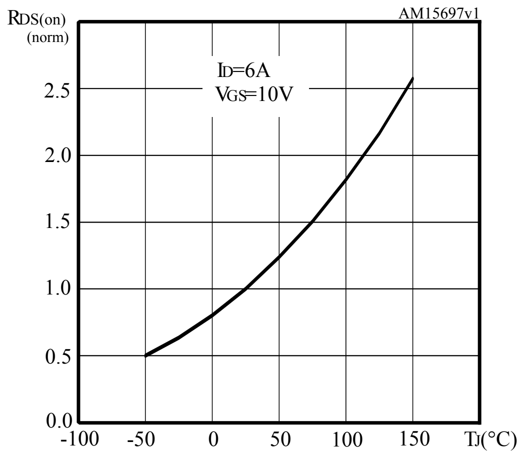


Figure 11. Normalized breakdown voltage vs temperature

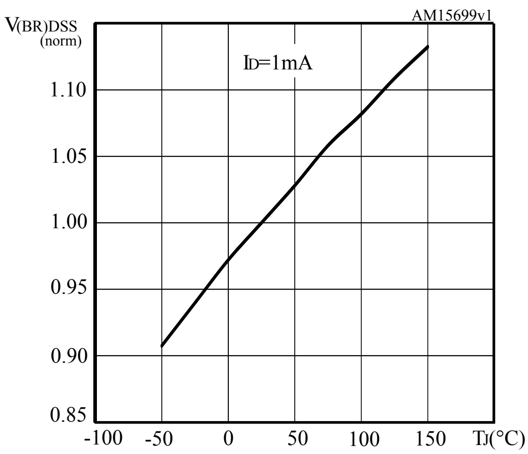
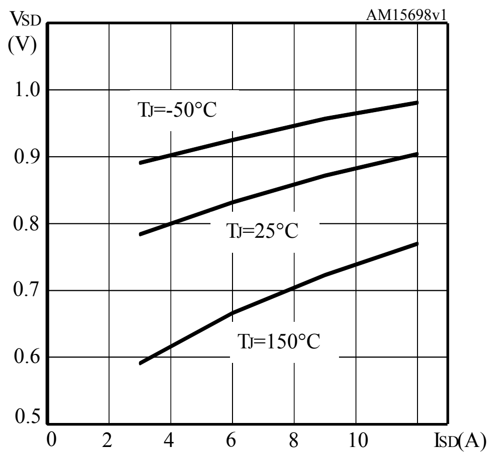


Figure 12. Typical reverse diode forward characteristics



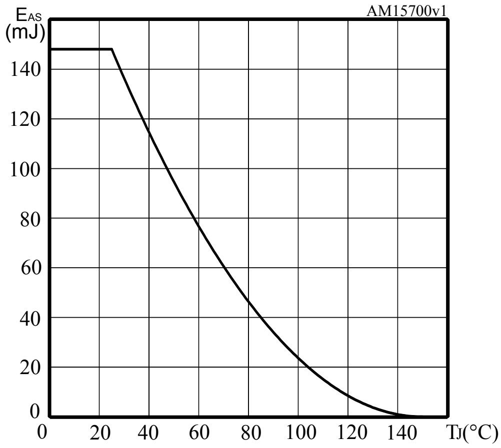


Figure 13. Maximum avalanche energy vs temperature

3 Test circuits

Figure 14. Test circuit for resistive load switching times

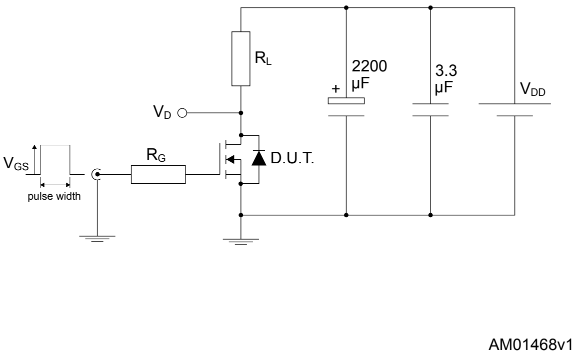


Figure 15. Test circuit for gate charge behavior

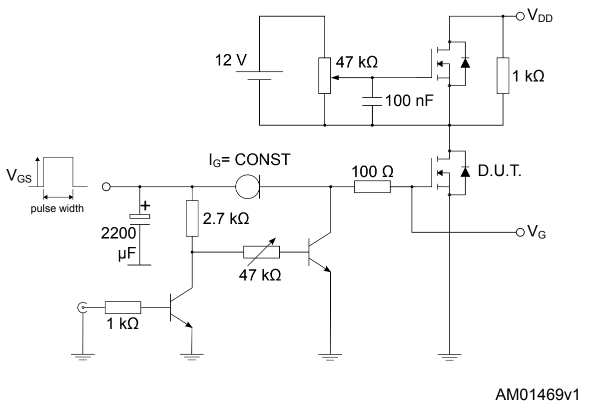


Figure 16. Test circuit for inductive load switching and diode recovery times

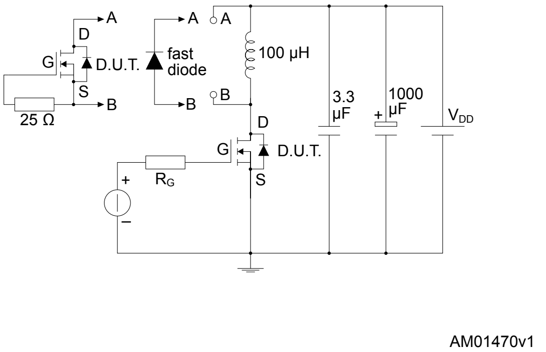


Figure 17. Unclamped inductive load test circuit

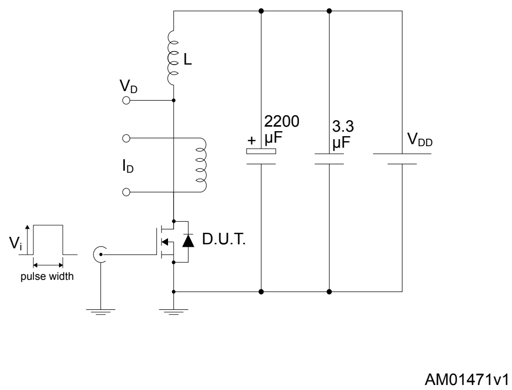


Figure 18. Unclamped inductive waveform

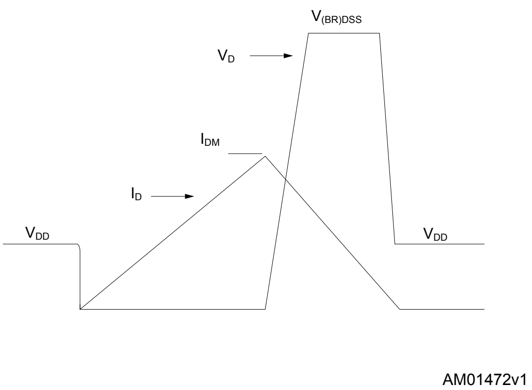
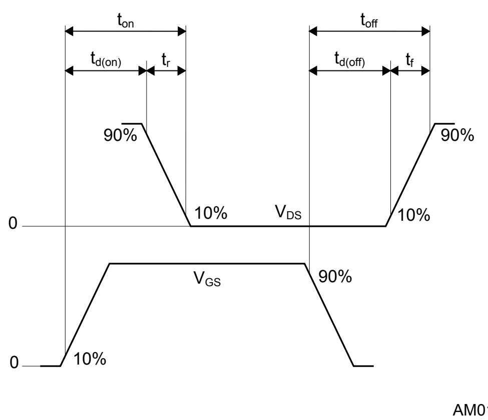


Figure 19. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 20. TO-220FP ultra narrow leads package outline

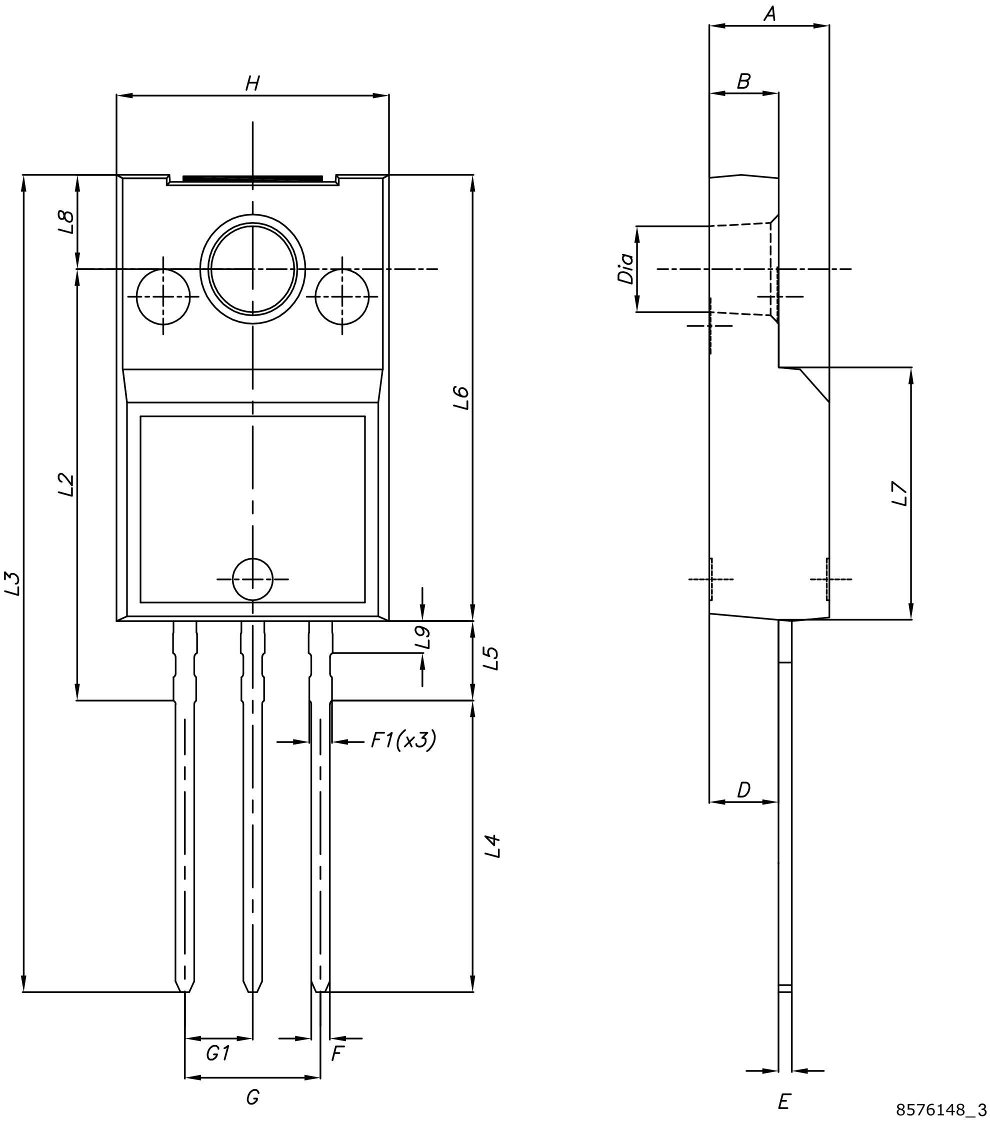


Table 8. TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
08-Oct-2015	1	First release.
14-Jul-2017	2	Modified *Figure 7: "Static drain-source on-resistance"*. Minor text changes.
03-Apr-2026	3	Updated Section 4: Package information. Minor text changes.

Contents