

ESD Protection Diode

Micro-Packaged Diodes for ESD Protection ESD7C, SZESD7C SERIES

The ESD7CxxD Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. Because of its small size, it is suited for use in cellular phones, portable devices, digital cameras, power supplies and many other portable applications.

Specification Features:

- Low Capacitance 6.2 pF to 13 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.047" x 0.047" (1.20 mm x 1.20 mm)
- Low Body Height: 0.020" (0.5 mm)
- Stand-off Voltage: 3.3 V, 5 V
- Low Leakage
- Response Time < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000-4-2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS

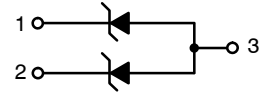
Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		± 8.0 ± 15	kV
Total Power Dissipation on FR-5 Board (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	240 1.9	mW mW/ $^\circ\text{C}$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	525	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature - Maximum (10 Second Duration)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.

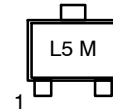
PIN 1. CATHODE
2. CATHODE
3. ANODE



MARKING DIAGRAM



SOT-723
CASE 631AA



L5 = Specific Device Code
M = Date Code

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
ESD7CxxDT5G	SOT-723 (Pb-Free)	8000 / Tape & Reel
SZESD7CxxDT5G	SOT-723 (Pb-Free)	8000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the table on page 2 of this data sheet.

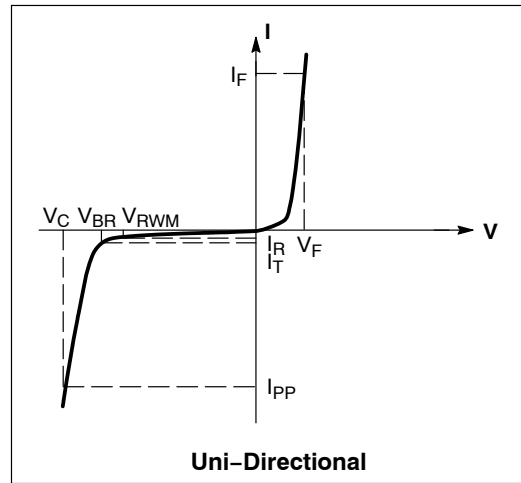
ESD7C, SZESD7C SERIES

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ $V_R = 0$ and $f = 1\text{ MHz}$

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 1.1\text{ V Max.}$ @ $I_F = 10\text{ mA}$)

Device (Note 2)	Device Marking	$V_{RWM}\text{ (V)}$	$I_R\text{ (}\mu\text{A)} @ V_{RWM}$	$V_{BR}\text{ (V)} @ I_T$ (Note 3)	I_T	C (pF) (Note 4)	C (pF) (Note 4)	V_C
		Max	Max	Min	mA	Typ	Max	Per IEC61000-4-2 (Note 5)
ESD7C3.3DT5G	L5	3.3	1.0	5.0	1.0	12	13	Figures 1 and 2 See Below (Note 6)
ESD7C5.0DT5G	L4	5.0	0.5	11	1.0	6.0	6.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Include SZ-prefix devices where applicable.
3. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C .
4. Capacitance of one diode at $f = 1\text{ MHz}$, $V_R = 0\text{ V}$, $T_A = 25^\circ\text{C}$.
5. For test procedure see Figures 3 and 4 and Application Note AND8307/D.
6. ESD7C5.0DT5G shown below. Other voltages available upon request.

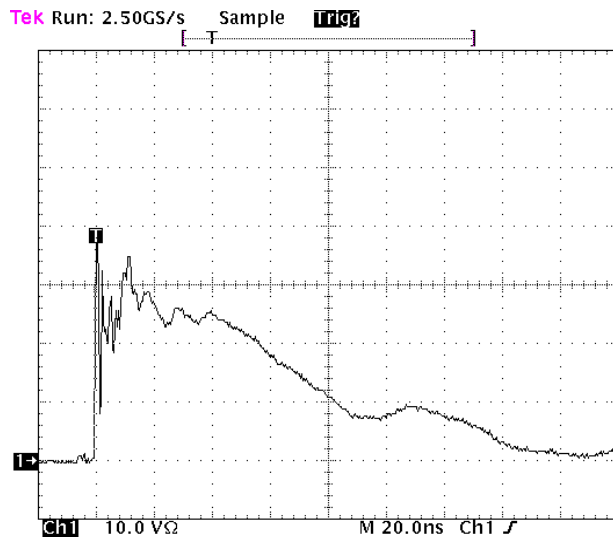


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000-4-2

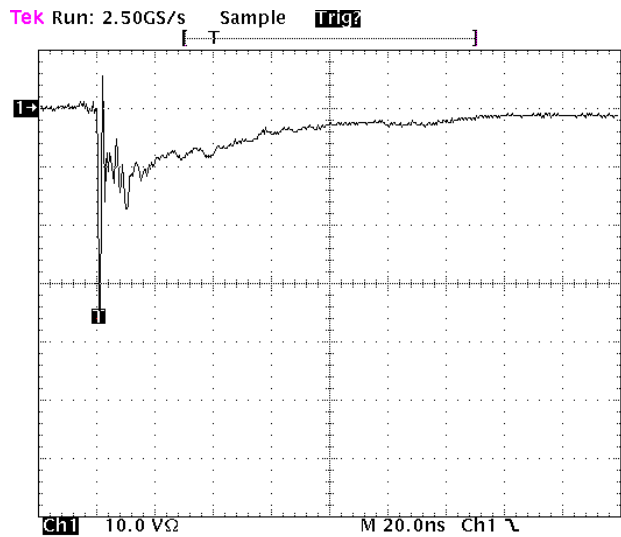


Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000-4-2

ESD7C, SZESD7C SERIES

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

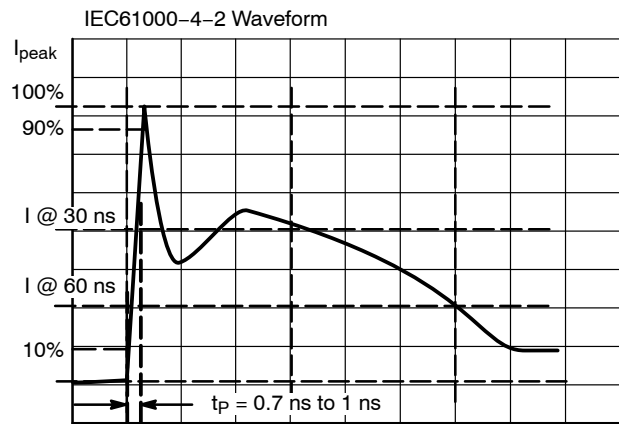


Figure 3. IEC61000-4-2 Spec

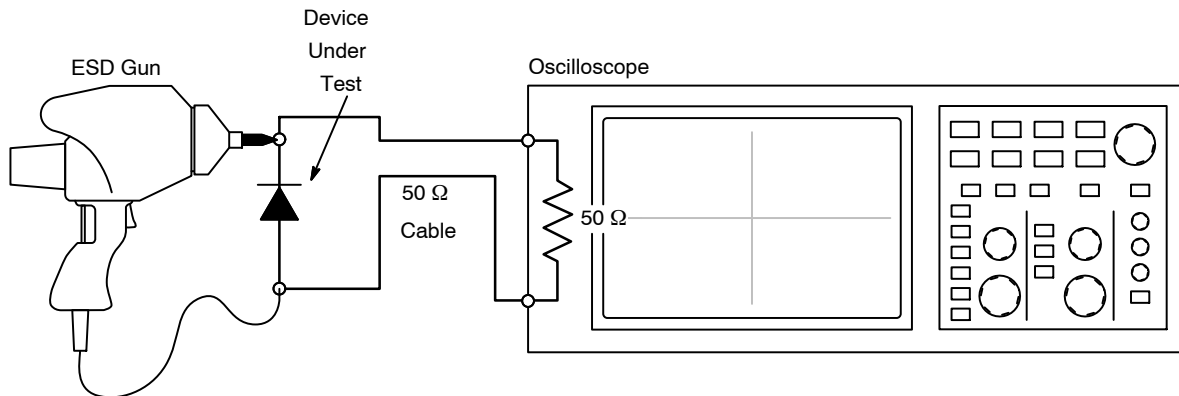


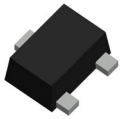
Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

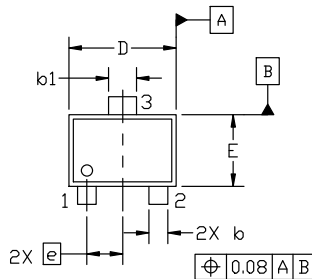


SOT-723 1.20x0.80x0.50, 0.40P
CASE 631AA
ISSUE E

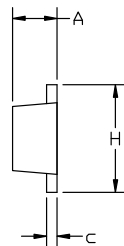
DATE 24 JAN 2024

NOTES:

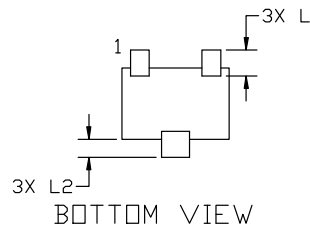
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



TOP VIEW

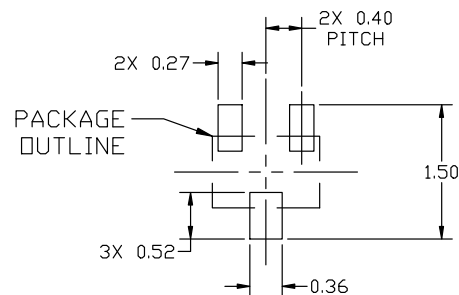


SIDE VIEW



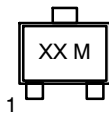
BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
c	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25



RECOMMENDED MOUNTING
FOOTPRINT

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLE 1: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 2: PIN 1. ANODE 2. N/C 3. CATHODE	STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. GATE 2. SOURCE 3. DRAIN
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DESCRIPTION:	SOT-723 1.20x0.80x0.50, 0.40P	PAGE 1 OF 1

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