Fully Integrated Switch-Mode One-Cell Li-Ion Charger with Full USB Compliance and Accessory Power Connection

Check for Samples: bq24180

FEATURES

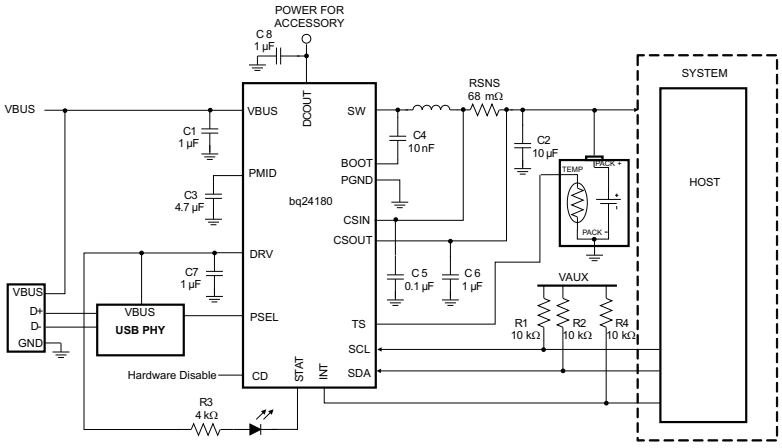
- Charge Faster than Linear Chargers From Current Limited Input Sources
- High-Accuracy Voltage and Current Regulation
  - Input Current Regulation Accuracy: ±5% (100mA, 500mA)
  - Charge Voltage Regulation Accuracy: ±0.5% (25°C), ±1% (0–125°C)
  - Charge Current Regulation Accuracy: ±5%
- Accessory Power Output (DCOUT)
- Input Voltage Based Dynamic Power Management
- Safety Limit Register for Maximum Charge Voltage and Current Limiting
- High-Efficiency Mini-USB/AC Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- 20-V Absolute Maximum and 16.5V Operation Input Voltage Rating
- Built-in Input Current Sensing and Limiting
- Integrated Power FETs for Up to 1.5-A Charge Rate
- Programmable Charge Parameters through I²C™ compatible Interface (up to 3.4 Mbps)
- Synchronous Fixed-Frequency PWM Controller Operating at 3 MHz With 0% to 99.5% Duty Cycle
- Safety Timer and Software Watchdog
- Reverse Leakage Protection Prevents Battery Drainage
- Thermal Regulation and Protection
- Status Outputs for Charging and Faults
- 25-Pin WCSP Package

APPLICATIONS

- Mobile Phones and Smart Phones
- Portable Media Players
- Handheld Devices

DESCRIPTION

The bq24180 is a compact, flexible, high-efficiency, USB-friendly switch-mode charge management device for single-cell Li-ion and Li-polymer batteries used in a wide range of portable applications. The charge parameters is programmable using an I²C compatible interface. The bq24180 integrates a synchronous PWM controller, power MOSFETs, input current sensing and overvoltage protection, high-accuracy current and voltage regulation, and charge termination, into a small WCSP package.



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I²C is a trademark of Phillips Electronics.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The bq24180 charges the battery in three phases: conditioning, constant current and constant voltage. Charge current is programmable using the I^2C interface. Additionally, the input current can be limited to a host programmable threshold to maintain maximum charge current from current-limited sources, such as USB ports. Charge is terminated based on user-selectable minimum current level. A software watchdog provides a safety backup for I^2C interface while a safety timer prevents overcharging the battery. During normal operation, bq24180 automatically restarts the charge cycle if the battery voltage falls below an internal threshold and automatically enters sleep mode or high impedance mode when the input supply is removed. The charge status is reported to the host using the I^2C interface. During the charging process, the bq24180 monitors its junction temperature (T_J) and reduces the charge current if T_J increases to 125°C. The bq24180 is available in 25-pin WCSP package.

ORDERING INFORMATION

PART NUMBER (1)(2)	V_{OVP}	I^2C ADDRESS
bq24180YFFR	16.5 V	6B
bq24180YFFT	16.5 V	6B

(1) The YFF package is available in the following options:
R – taped and reeled in quantities of 3,000 devices per reel.
T – taped and reeled in quantities of 250 devices per reel.
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		LIMITS	UNIT
Supply voltage range (with respect to PGND)	VBUS	–2 to 20	V
Input voltage range (with respect to and PGND)	SCL, SDA, PSEL, CSIN, CSOUT, DRV, DCOUT, INT	–0.3 to 7	V
Output voltage range (with respect to and PGND)	PMID, STAT	–0.3 to 20	V
	SW, BOOT	–0.7 to 20	
Voltage difference between CSIN and CSOUT inputs (VCSIN –VCSOUT)		±7	V
Voltage difference between BOOT and SW inputs (VBOOT –VSW)		–0.3 to 7	V
Output sink	INT	5	mA
	STAT	10	
Output current	DCOUT	1.5	A
	DRV	10	mA
Output current (average)	SW	2	A
T_A	Operating free-air temperature range	–30 to +85	°C
T_J	Junction temperature range	–40 to +125	°C
T_{stg}	Storage temperature	–45 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
WCSP-25	60°C/W(1)	1.57°C/W	540 mW	5.4 mW/°C

(1) Using JEDEC 2s2p PCB standard.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VBUS	4.0		16(1)	V
Operating junction temperature range, T_J	0		125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of Figure 2, V_{VBUS} = 5V, HZ_MODE=0, CD=0, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{VBUS}	V_{VBUS} supply current for control	V_{VBUS} > $V_{VBUS(min)}$, PWM switching		10		mA
		V_{VBUS} > $V_{VBUS(min)}$, PWM NOT switching			5	mA
		0°C< T_J < 85°C, EN=0 or HZ_MODE=1			650	µA
I_{VBUS_LEAK}	Leakage current from battery to VBUS pin	0°C< T_J < 85°C, V_{CSOUT} = 4.2 V, No input connected			5	µA
I_{BAT_DCOUT}	Battery Current when using DCOUT	DCOUT = enabled, V_{BAT} = 4.2V, DCOUT_ILIM=1A, I_{DCOUT}=750mA			800	µA
I_{BAT_HIZ}	Battery discharge current in High Impedance mode, (CSIN, CSOUT, SW pins)	0°C< T_J < 85°C, V_{CSOUT} = 4.2 V, No Input connected, DCOUT disabled SCL,SDA=0V or 1.8V			30	µA
		0°C< TJ < 85°C, VCSOUT = 4.2 V, High Impedance mode, DCOUT disabled, V_{VBUS} = 5V, SCL,SDA=0V or 1.8V			60	µA
VOLTAGE REGULATION						
V_{OREG}	Output charge voltage programmable range	Operating in voltage regulation, programmable	3.5		4.44	V
	Voltage regulation accuracy	T_A = 25°C	–0.5%		0.5%	
			–1%		1%	
CURRENT REGULATION - FAST CHARGE						
$I_{OCHARGE}$	Output charge current programmable range	V_{PRECHG} ≤ V_{CSOUT} < V_{OREG}, V_{VBUS}>V_{SLP}, R_{SNS} = 68 mΩ, Programmable	550		1550	mA
	Regulation accuracy for charge current across RSNS V_{IREG} = $I_{OCHARGE}$ × R_{SNS}	V_{ICHRG} = 37.4 mV to 44.2 mV	–3.5%		3.5%	
		V_{ICHRG} > 44.2 mV	–3.0%		3.0%	
PSEL, CD LOGIC LEVEL						
V_{IL}	Input low threshold level	PSEL, CD falling			0.4	V
V_{IH}	Input high threshold level	PSEL, CD rising	1.2			V
CHARGE TERMINATION DETECTION						
I_{TERM}	Termination charge current	V_{CSOUT} > V_{OREG}–V_{RCH} , V_{VBUS}>V_{SLP}, R_{SNS} = 68 MΩ, Programmable	25		200	mA
I_{TERM_dgl}	Deglitch time for charge termination	Both rising and falling, 2-mV over- drive, t_{RISE}, t_{FALL} = 100 ns		30		ms
	Regulation accuracy for termination current across R_{SNS} V_{IREG_TERM} = I_{OTERM} × R_{SNS}	V_{TERM} = 1.7 mV	–40%		40%	
		V_{TERM} = 3.4 mV to 6.8 mV	–16%		16%	
		V_{TERM} = 6.8 mV to 13.6 mV	–11%		11%	
		V_{TERM} ≥ 13.6 mV	–5.5%		5.5%	
	Battery Detection sink current before charge done			–550		µA
INPUT BASED DYNAMIC POWER MANAGEMENT						

ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 2, V_{VBUS} = 5V, HZ_MODE=0, CD=0, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN_DPM}	The threshold when input based DPM loop kicks in	Charge mode, programmable		4.15		4.71	V
	DPM loop kick-in threshold tolerance			–2%		2%	
FAULTY ADAPTER PROTECTION							
$V_{VBUS\ (MIN)}$	Faulty adapter threshold			3.6	3.8	4.0	V
	Deglitch time for Faulty adapter				30		ms
	Hysteresis for faulty adapter protection	V_{VBUS} Rising		100		200	mV
	Current source for faulty adapter protection			20	30	40	mA
t_{INT}	Detection Interval				2		s
INPUT CURRENT LIMITING							
I_{IN_LIMIT}	Input current limiting threshold	USB charge mode, current pulled from PMID	I_{IN_LIMIT} = 100 mA	90	95	100	mA
			I_{IN_LIMIT} = 500 mA	450	475	500	
			I_{IN_LIMIT} = 800 mA	700	755	800	
DCOUT							
R_{DCOUT}	DCOUT Pass FET on-resistance	I_{DCOUT} = 500 mA				300	mΩ
I_{LIM_DCOUT}	DCOUT current limit programmable range	Programmable via I^2C		350		1400	mA
t_{DGL_DCOUT}	Deglitch time from DCOUT current-limit event to DCOUT latch-off				14.5		ms
I_{LIM_DCOUT}	DCOUT current limit range	Programmable via I^2C	I_{LIM_DCOUT} = 350mA	270	350		mA
			I_{LIM_DCOUT} = 750mA	650	750		
			I_{LIM_DCOUT} = 1050mA	800	1050		
			I_{LIM_DCOUT} = 1400mA	1050	1400		
BATTERY RECHARGE THRESHOLD							
V_{RCH}	Recharge threshold voltage	Below VOREG		100	120	150	mV
	Deglitch time	V_{CSOUT} decreasing below threshold, t_{FALL} = 100 ns, 10-mV overdrive			130		ms
STAT OUTPUTS							
$V_{OL(STAT)}$	Low-level output saturation voltage, STAT	I_O = 10 mA, sink current				0.5	V
	High-level leakage current	Voltage on STAT pin is 5V				1	µA
$V_{OL(INT)}$	Low-level output saturation voltage, INT	I_O = 1 mA, sink current				0.4	V
	High-level leakage current	Voltage on INT pin is 5V				1	µA
I^2C BUS LOGIC LEVELS AND TIMING CHARACTERISTICS							
V_{OL}	Output low threshold level	I_O = 10 mA, sink current				0.4	V
	Input low threshold level	$V_{(pull\text{-}up)}$ = 1.8 V, SDA and SCL				0.4	V
	Input high threshold level	$V_{(pull\text{-}up)}$ = 1.8 V, SDA and SCL		1.2			V
$I_{(bias)}$	Input bias current	$V_{(pull\text{-}up)}$ = 1.8 V, SDA and SCL				1	µA
f_{SCL}	SCL clock frequency					3.4	MHz
SLEEP COMPARATOR							
V_{SLP}	Sleep-mode entry threshold, V_{BUS}-V_{CSOUT}	2.3 V ≤ V_{CSOUT} ≤ V_{OREG}, V_{VBUS} falling		0	40	100	mV
$V_{SLP\text{-}EXIT}$	Sleep-mode exit hysteresis	2.3 V ≤ V_{CSOUT} < V_{OREG}		140	200	260	mV
	Deglitch time for VBUS rising above V_{SLP}+V_{SLP_EXIT}	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns			30		ms
UVLO							
V_{UVLO}	IC active threshold voltage	V_{VBUS} rising		3.05	3.3	3.55	V
V_{UVLO_HYS}	IC active hysteresis	V_{VBUS} falling from above V_{UVLO}		120	150		mV
PWM							
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 500 mA, Measured from V_{VBUS} to PMID			110	210	mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMID to SW			130	250	mΩ

ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 2, V_{VBUS} = 5V, HZ_MODE=0, CD=0, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		125	210	mΩ
f_{OSC}	Oscillator frequency			3.0		MHz
	Frequency accuracy		–10%		10%	
D_{MAX}	Maximum duty cycle			99.5%		
D_{MIN}	Minimum duty cycle		0			
	Synchronous mode to non-synchronous mode transition current threshold(1)	Low-side MOSFET cycle-by-cycle current sensing		100		mA
V_{DRV}	Internal bias voltage regulator	I_{DRV} = 10 mA	5	5.2	5.45	V
I_{DRV}	DRV Output Current	External load on DRV	10			mA
V_{DO_DRV}	DRV Dropout Voltage (V_{VBUS} – V_{DRV})	I_{VBUS} = 1A, V_{VBUS} = 5 V, I_{DRV} = 10 mA			340	mV
		V_{UVLO} < V_{VBUS}<V_{SLP}		750		
PROTECTION						
V_{OVP}	Input OVP threshold voltage	Threshold over V_{VBUS} to turn off converter during charge	16	16.5	17	V
	V_{OVP} hysteresis	V_{VBUS} falling from above V_{OVP}		185		mV
V_{IN_HIGH}	Input High threshold	V_{VBUS} Rising, Threshold where I_{BAT} falls to 50 mA	9.5	9.8	10.1	V
	VIN_HIGH_USB hysteresis	V_{VBUS} falling from above V_{IN_HIGH}		150		mV
$t_{OVP-dgl}$	OVP deglitch time	V_{VBUS} rising or falling		32		ms
I_{LIMIT}	Cycle-by-cycle current limit for charge	Charge mode operation	1.8	2.4	3.0	A
V_{PRECHG}	Precharge to fast charge threshold	V_{CSOUT} rising	1.9	2.0	2.1	V
	VPRECHG hysteresis	V_{CSOUT} falling from above V_{PRECHG}		100		mV
I_{PRECHG}	Precharge charge charging current	V_{CSOUT} ≤ V_{SHORT} and V_{IN_HIGH} < V_{VBUS} < V_{OVP}	33.5	50.0	66.5	mA
T_{SHTDWN}	Thermal trip			165		°C
	Thermal hysteresis			10		°C
T_{CF}	Thermal regulation threshold	Charge current begins to taper down		120		°C
$t_{WATCHDOG}$	Timeout for the watchdog timer	Watchdog timer	12			s
	Safety timer accuracy		–20%		20%	
V_{HOT}	TS Hot Threshold	Corresponds to 55°C, V_{TS} Falling	0.153	0.160	0.169	V
	TS Hot Threshold Hysteresis	VTS Rising		12.5		mV
V_{WARM}	TS Warm Threshold	Corresponds to 45°C V_{TS} Falling	0.210	0.225	0.240	V
	TS Warm Threshold Hysteresis	V_{TS} Rising		12.5		mV
V_{COLD}	TS Cold Threshold	Corresponds to 5°C, V_{TS} Rising	1.06	1.10	1.14	V
	TS Cold Threshold Hysteresis	V_{TS} Falling		75		mV
I_{TS}	TS Bias Current		95	100	105	µA
	TS Open Resistance	Resistance on TS that translates to open circuit on TS	200			kΩ

(1) Bottom N-channel MOSFET always turns on for ~60 ns and then turns off if current is too low.

SIMPLIFIED BLOCK DIAGRAM

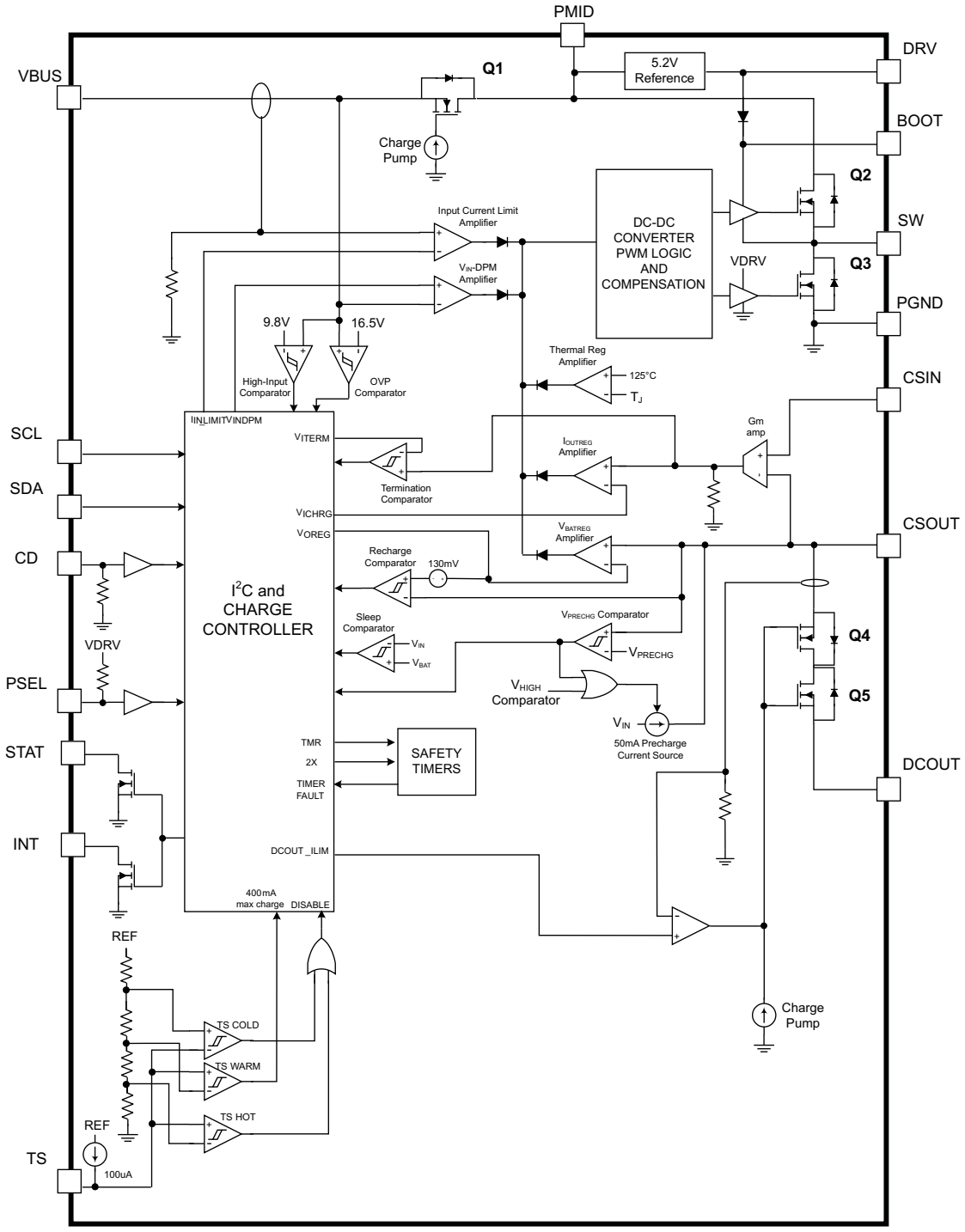
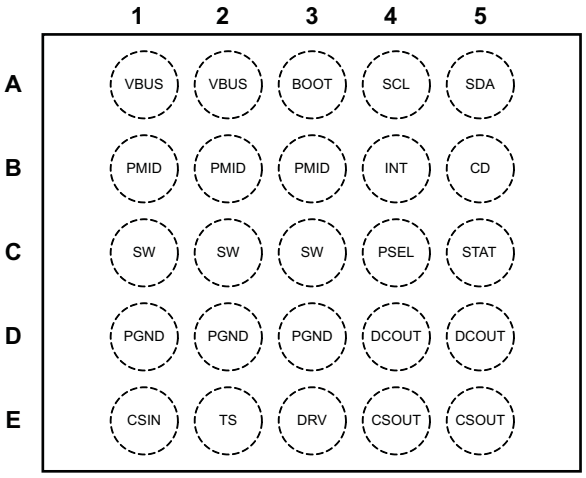


Figure 1. Simplified Block Diagram

DEVICE INFORMATION

PIN CONFIGURATION

TOP VIEW



2.2 mm x 2.4 mm 25-pin WCSP

PIN FUNCTIONS

NAME	PIN NO.	I/O	DESCRIPTION
VBUS	A1, A2	I/O	Charger Input Voltage. Connect to an input supply up to 16V. Bypass VBUS to PGND with a 1µF ceramic capacitor.
BOOT	A3	O	High-Side MOSFET Gate Driver Supply. Connect a 10nF ceramic capacitor (voltage rating above 10V) from BOOT pin to SW pin to supply the gate drive for the high side MOSFET.
SCL	A4	I	I^2C interface clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	A5	I/O	I^2C interface data. Connect SCL to the logic rail through a 10kΩ resistor.
PMID	B1, B2, B3	O	Connection Point Between Reverse Blocking MOSFET and High-Side Switching MOSFET. Bypass PMID to PGND with a minimum of 3.3µF ceramic capacitor. Use caution when connecting an external load to PMID. The PMID output is not current limited. Any short on PMID will result in damage to the IC.
INT	B4	O	Host Interface Status Output. INT is a low voltage open drain output used to signal charge status to the host processor. INT is pulled low during charging. When charging is complete or when charging is disabled, INT is high impedance. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT is enabled/disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 10kΩ resistor to communicate with the host processor.
CD	B5	O	Hardware Disable Input. Connect CD to GND to enable charge. Drive CD high to disable charge and place the bq24180 into high impedance mode. Toggling CD resets the safety timer when in DEFAULT mode, but does not reset the timer when in host mode. CD is pulled to PGND through a 100kΩ internal resistor.
SW	C1, C2, C3	O	Inductor Connection. Connect the switched side of the inductor to SW.
PSEL	C4	I	USB Source Detection Input. Drive PSEL high to indicate a USB source is connected to the input and the PC mode default values should be used. When PSEL is high, the IC starts up with a 100mA input current limit. Drive PSEL low to indicate that an AC Adapter is connected to the input. When PSEL is low, the IC starts up with no input current limit and a 1A charge current. PSEL has an internal 100kΩ pullup resistor.
STAT	C5	O	Status Output. STAT is an open drain output that is pulled low during charging. When charging is complete or when charging is disabled, STAT is high impedance. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. STAT is enabled/disabled using the EN_STAT bit in the control register. Connect STAT to a logic rail using an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
PGND	D1, D2, D3		Power ground. Connect to the ground plane for the circuit.
DCOUT	D4, D5	O	Accessory Power Output. DCOUT is connected to the battery through an internal pass FET. When enabled through I2C, DCOUT is connected to the battery. When disabled, DCOUT is high-impedance. Bypass DCOUT to PGND with at least a 1µF ceramic capacitor.
CSIN	E1	I	Charge Current-Sense Input. Battery current is sensed via the voltage drop across an external sense resistor. Bypass CSIN to PGND with a 0.1µF ceramic capacitor.

PIN FUNCTIONS (continued)

NAME	PIN NO.	I/O	DESCRIPTION
TS	E2	I	Battery Pack NTC Monitor. Connect TS to a 4.7kΩ NTC thermistor. During DEFAULT mode, when V_{TS} > V_{COLD} or V_{TS}<V_{HOT} charging is suspended. If V_{HOT} < V_{TS} < V_{WARM} charging current is reduced. The faults are reported by the I^2C interface. During host mode, the TS function is active, but does not affect charging. The faults are only reported by the I^2C interface.
DRV	E3	O	Gate Drive Supply. DRV is the supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with a 1µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected.
CSOUT	E4, E5	I	Battery voltage and Current Sense Input. Connect to the positive terminal of the battery pack. CSOUT is also the supply for the DCOUT output. Bypass CSOUT to PGND with 1µF ceramic capacitor.

TYPICAL APPLICATION CIRCUITS

VBUS = 5V, I_{IN_LIMIT} = 500mA, I_{CHARGE} = 1A, V_{BAT} = 3.5--4.44V (Adjustable), Safety Timer = 27 minute default w/ 12 seconds watchdog

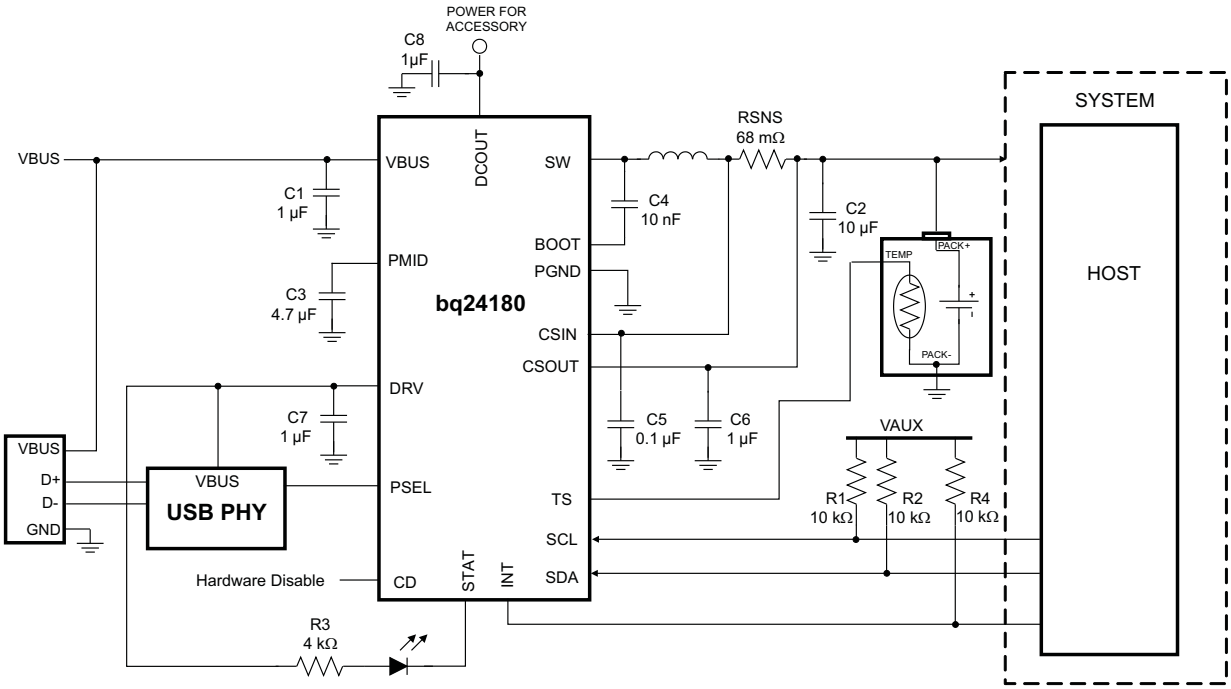


Figure 2. I²C Controlled 1-Cell USB Charger Application Circuit

TYPICAL CHARACTERISTICS

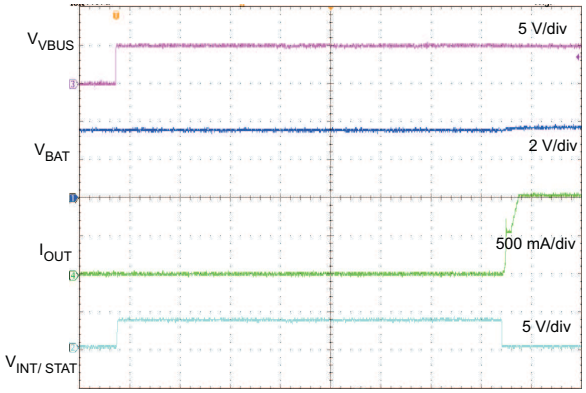


Figure 3. Adapter Insertion

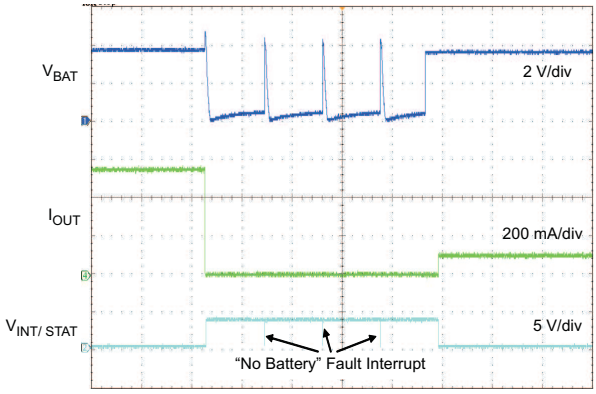


Figure 4. Battery Insertion/Removal

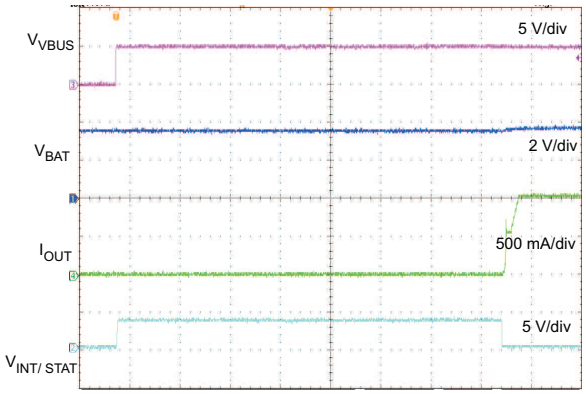


Figure 5. PWM Charging Waveforms

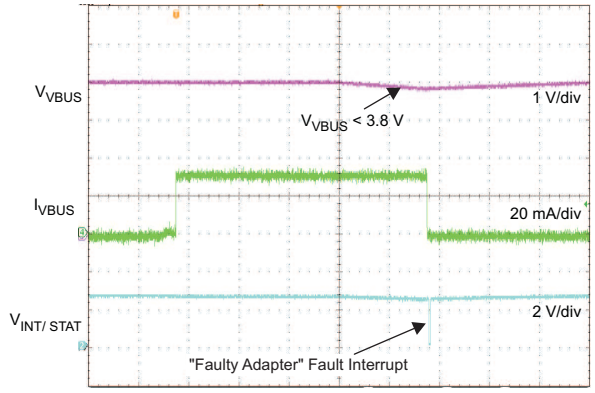


Figure 6. Faulty Adapter Detection

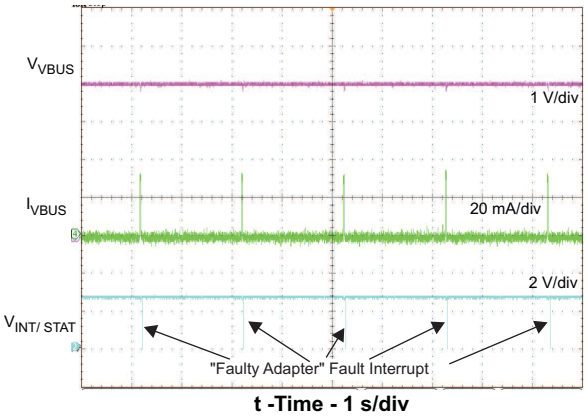


Figure 7. Faulty Adapter Detection (Showing Continuous Detection)

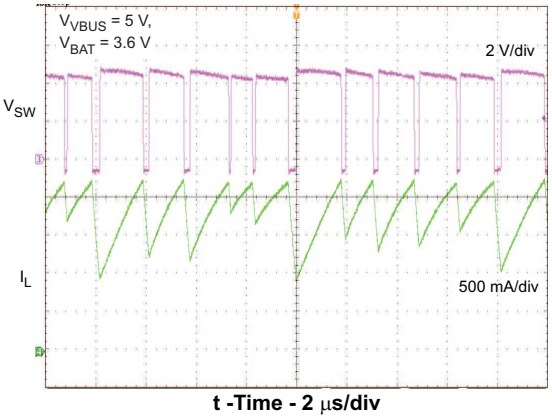


Figure 8. Cycle by Cycle Current Limit

TYPICAL CHARACTERISTICS (continued)

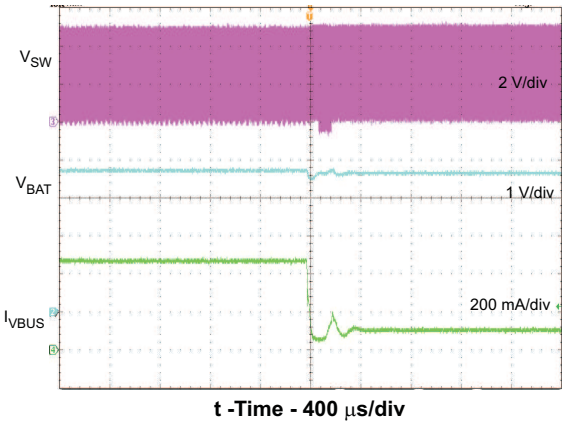


Figure 9. Input Current Limit Transition USB500 to USB100

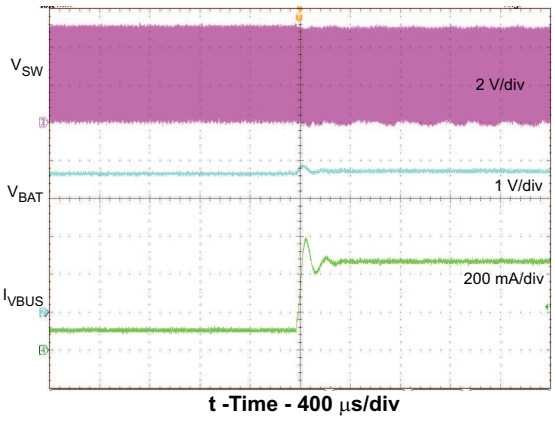


Figure 10. Input Current Limit Transition USB100 to USB500

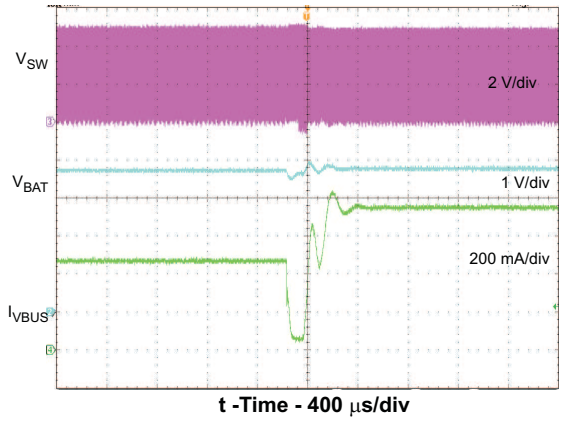


Figure 11. Input Current Limit Transition USB500 to 750mA

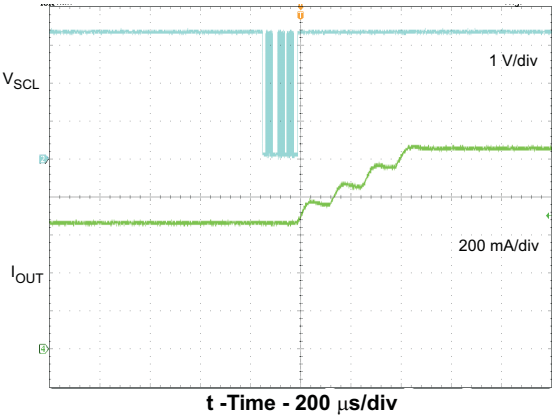


Figure 12. Charge Current Transition 550mA to 1.05A Using I^2C

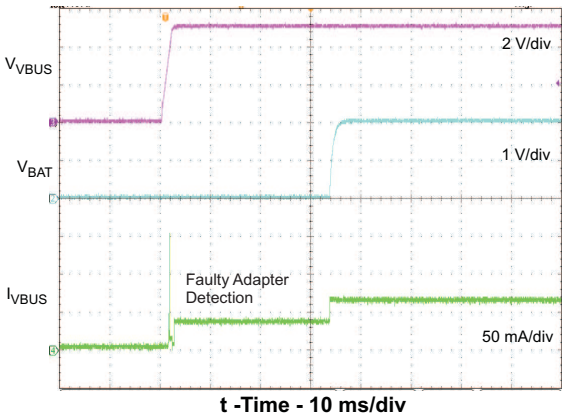


Figure 13. Startup Into Default Mode No Battery Connected

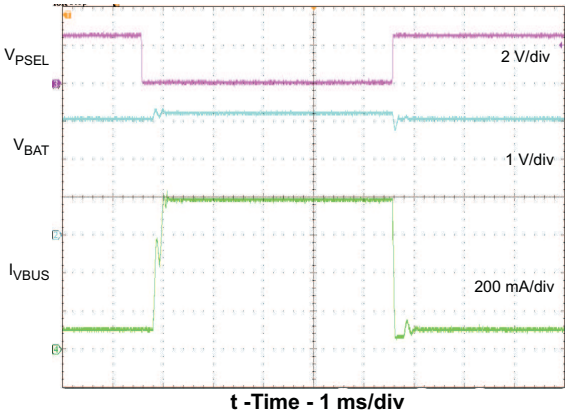


Figure 14. PSEL Transition

TYPICAL CHARACTERISTICS (continued)

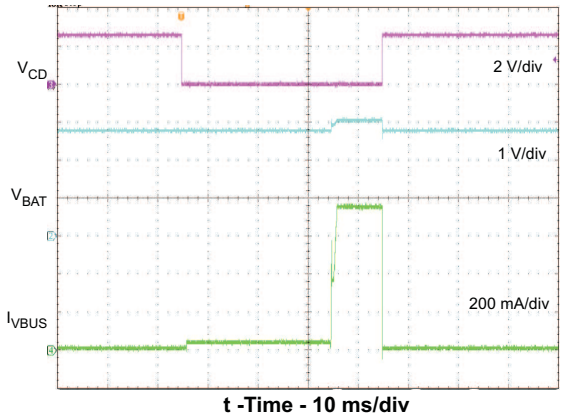


Figure 15. Enable/Disable Using CD

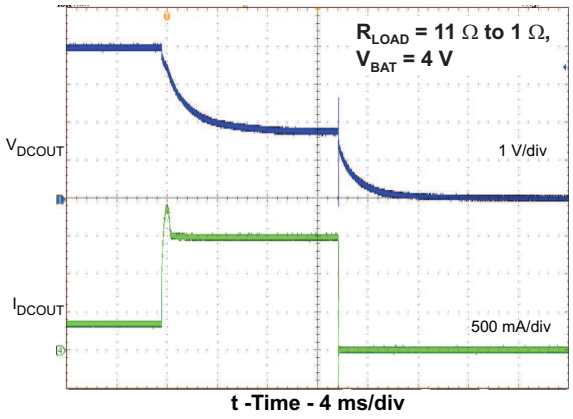


Figure 16. DCOUT OCP Response

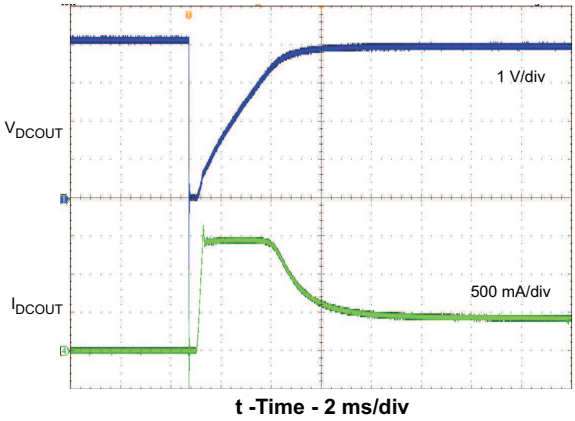


Figure 17. Hotplug 1000µF Capacitor into DCOUT

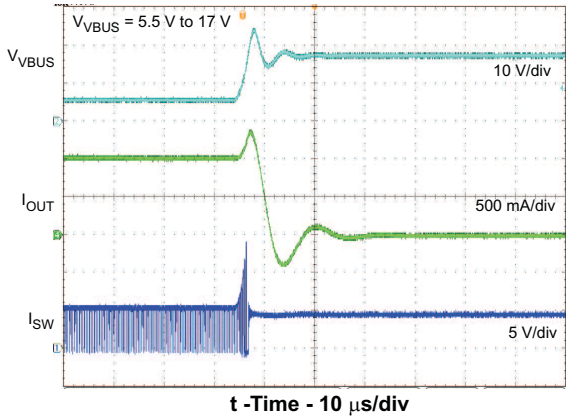


Figure 18. OVP Response

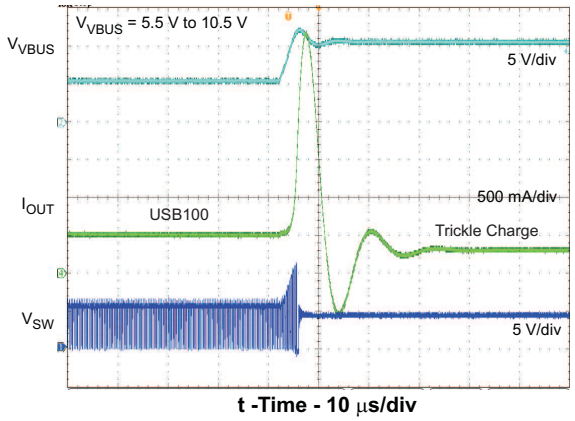


Figure 19. VINHIGH Response

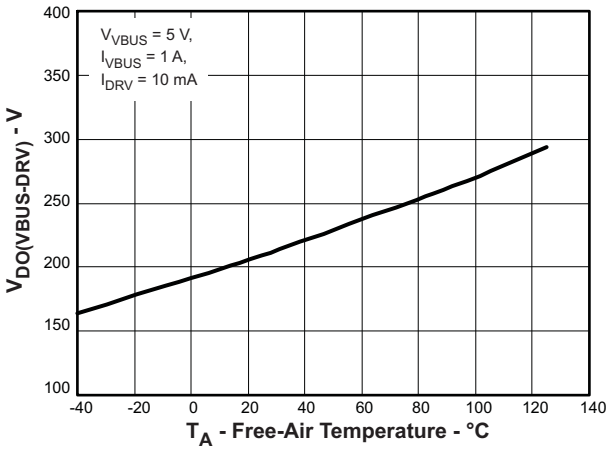


Figure 20. DRV Dropout vs T_A

TYPICAL CHARACTERISTICS (continued)

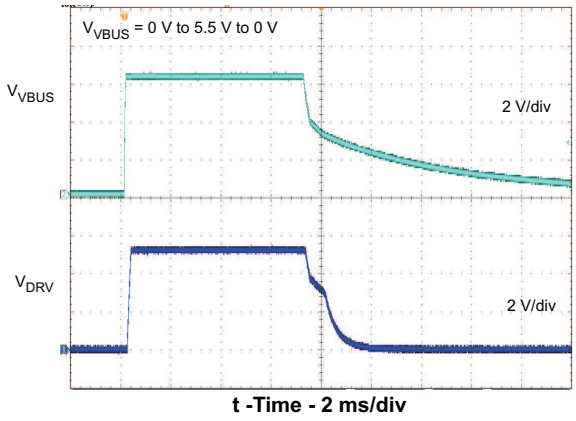


Figure 21. DRV Startup/Shutdown

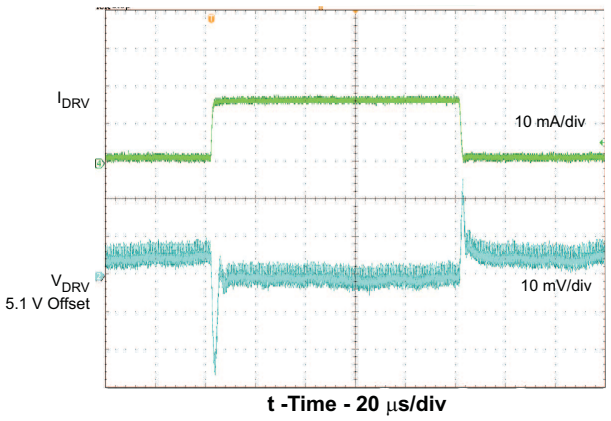


Figure 22. DRV Load Transient

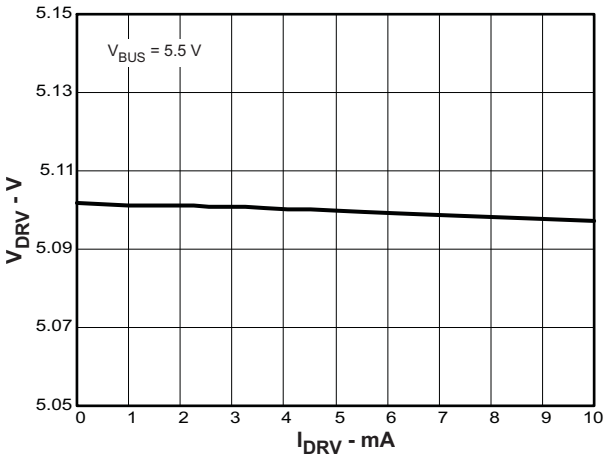


Figure 23. DRV Load Regulation

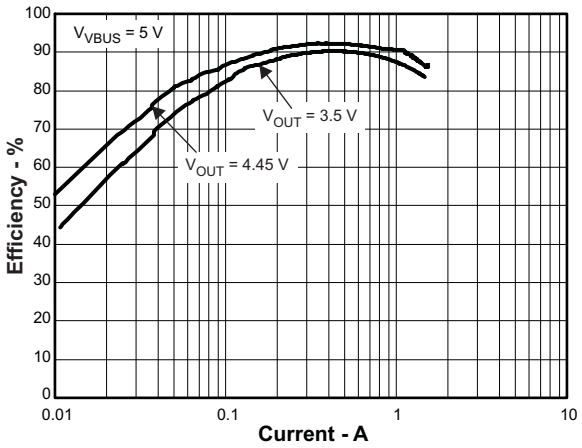


Figure 24. Charger Efficiency

DETAILED DESCRIPTION

The bq24180 is a highly integrated synchronous switch-mode charger featuring integrated MOSFETs and small external components, targeted at extremely space-limited portable applications powered by 1-cell Li-Ion or Li-polymer battery pack. For current limited power source, such as a USB host or hub, the high efficiency converter is critical in fully utilizing the input power capacity and quickly charging the battery. Due to the high efficiency in a wide range of the input voltage and battery voltage, the switching mode charger is a good choice for high speed charging with less power loss and better thermal management.

The bq24180 has two operation modes: charge mode and high impedance mode. In charge mode, the bq24180 supports a precision Li-ion or Li-polymer charging system for single-cell applications. In high impedance mode, the bq24180 stops charging and operates in a mode with very low current from IN and battery, to effectively reduce the power consumption when the portable device in standby mode. Through proper control, bq24180 achieves the smooth transition among different operation modes.

Charge Mode Operation

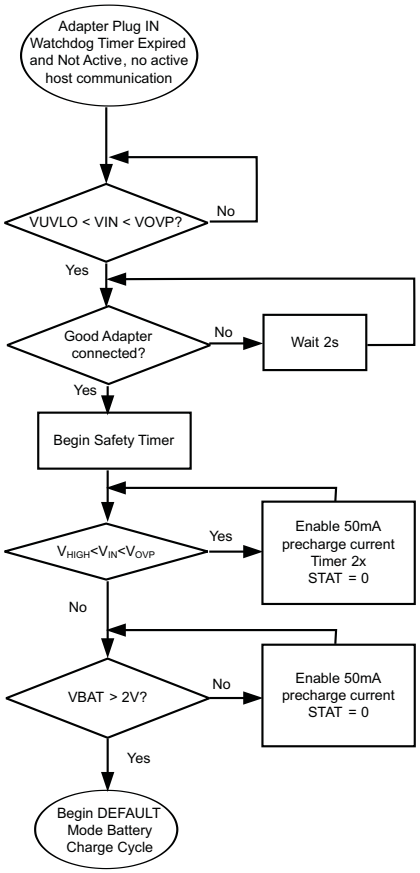


Figure 25. Startup on Adapter Plug-In in DEFAULT Mode

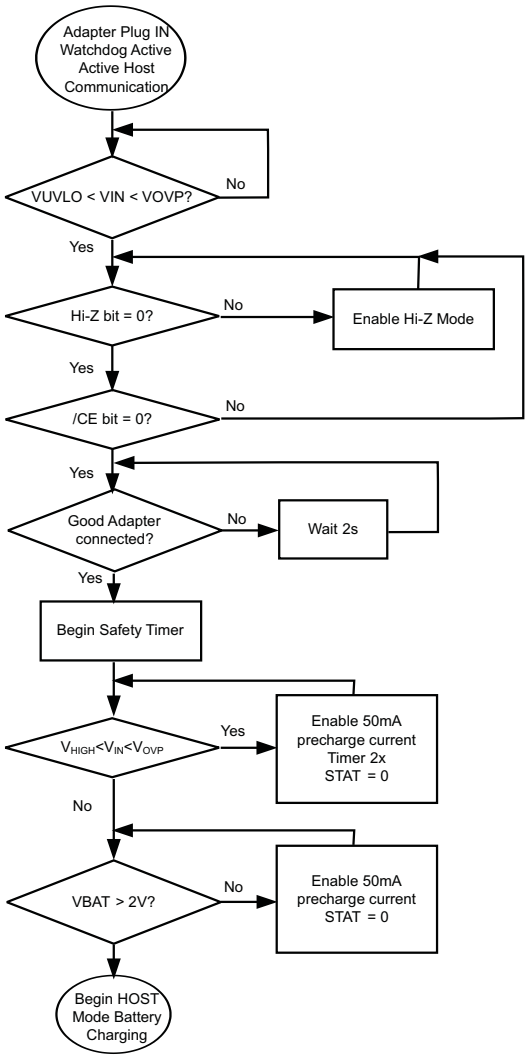


Figure 26. Startup on Adapter Plug-In in Host-Controlled Mode

Charge Profile

In charge mode, bq24180 has five control loops to regulate input voltage, input current, charge current, charge voltage and device junction temperature. During the charging process, all five loops are enabled and the one that is dominant will take over the control. The bq24180 supports a precision Li-ion or Li-polymer charging system for single-cell applications. Figure 27 indicates a typical charge profile without input current regulation loop and it is similar to the traditional CC/CV charge curve, while Figure 27 shows a typical charge profile when input current limiting loop is dominant during the constant current mode, and in this case the charge current is higher than the input current so the charge process is faster than the linear chargers. For bq24180, the input current limits, the charge current, termination current, and charge voltage are all programmable using I^2C interface.

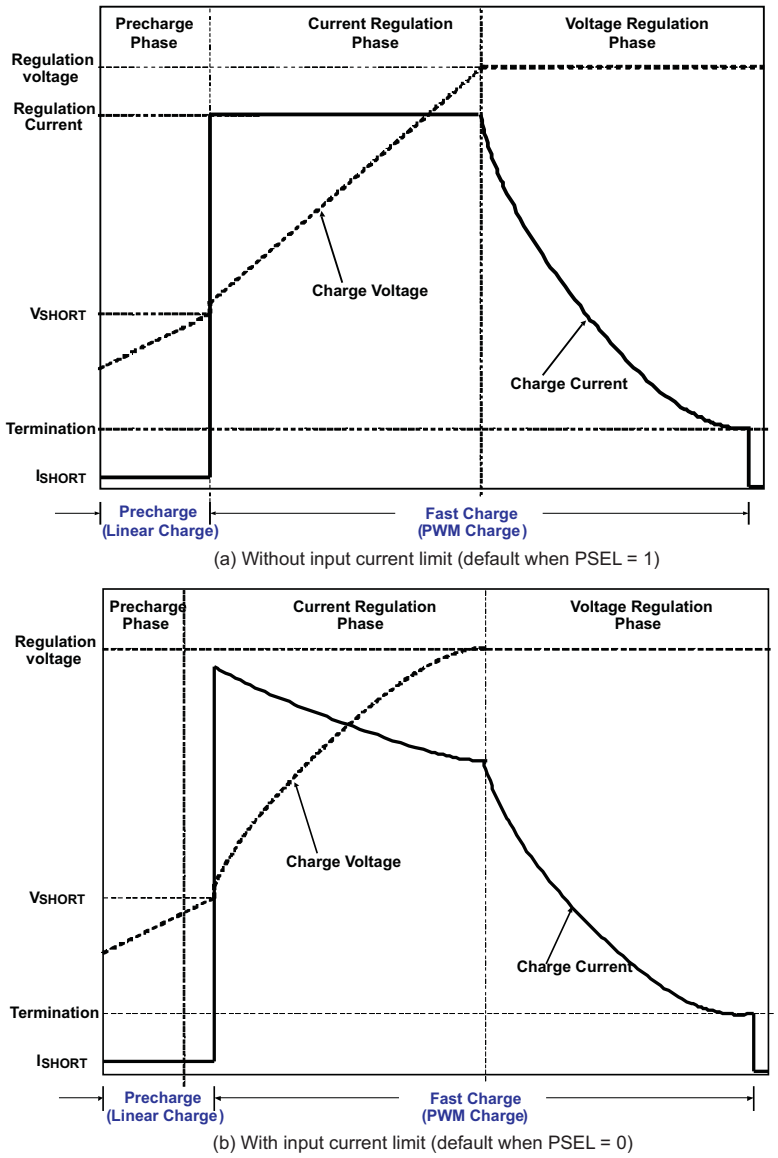


Figure 27. Typical Charging Profile of bq24180

PWM Controller in Charge Mode

The bq24180 provides an integrated, fixed 3 MHz frequency voltage-mode controller with Feed-Forward function to regulate charge current or voltage. This type of controller is used to help improve line transient response, thereby simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR. There is a 0.5V offset on the bottom of the PWM ramp to allow the device to operate between 0% to 99.5% duty cycles.

The bq24180 has two back to back common-drain N-channel MOSFETs at the high side and one N-channel MOSFET at low side. An input N-MOSFET (Q1) prevents battery discharge when VBUS is lower than $V_{VBUS\ (MIN)}$. The second high-side N-MOSFET (Q2) behaves as the switching control switch (see Figure 1). A charge pump circuit is used to provide gate drive for Q1, while a boot strap circuit with external boot-strap capacitor is used to boost up the gate drive voltage for Q2.

Cycle-by-cycle current limit is sensed through the internal sense MOSFETs for Q2 and Q3. The threshold for Q2 is set to a nominal 2.5-A peak current. The low-side MOSFET (Q3) also has a current limit that decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side N-channel MOSFET (Q3) before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side MOSFET is greater than 100mA to minimize power losses.

Battery Charging Process

At the beginning of precharge, while battery voltage is below the $V_{PRECHARGE}$ threshold, the bq24180 applies the 50mA precharge current, $I_{PRECHARGE}$, to the battery.

When the battery voltage is above $V_{PRECHARGE}$ and below V_{OREG}, the charge current ramps up to fast charge current, $I_{OCHARGE}$, or a charge current that corresponds to the input current of I_{IN_LIMIT}. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. The input current limit, I_{IN_LIMIT}, and fast charge current, $I_{OCHARGE}$, are programmable by the host. Once the battery voltage is close to the regulation voltage, V_{OREG}, the charge current is tapered down as shown in Figure 27. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the CSOUT and PGND pins. The bq24180 is a fixed single-cell voltage version, with adjustable regulation voltage (3.5V to 4.44V) programmed using the I^2C interface.

The bq24180 monitors the charging current during the voltage regulation phase. Once the termination threshold, I_{TERM}, is detected and the battery voltage is above the recharge threshold, the bq24180 terminates charge. The termination current level is programmable. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0, refer to I^2C section for details.

A new charge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the $V_{OREG-VRCH}$ threshold.
2. VBUS Power-on reset (POR), if battery voltage is below the $V_{PRECHARGE}$ threshold
3. CE bit toggle or RESET bit is set (Host controlled)

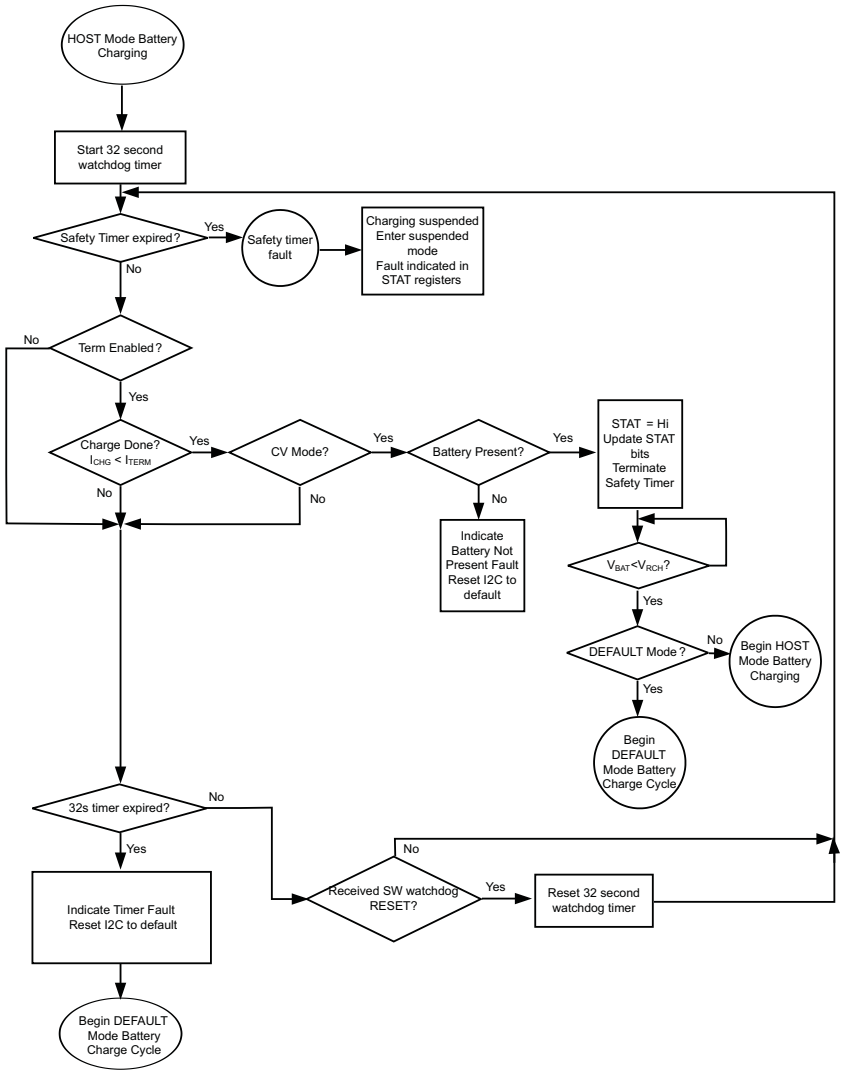


Figure 28. Host Mode Charging Process

DEFAULT Mode

DEFAULT mode is used when I^2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled and V_{BAT}>3.6V before I^2C communication is established
2. When the watchdog timer expires without a reset from the I^2C interface and the safety timer has not expired.
3. When the device comes out of any fault condition (sleep mode, OVP, faulty adapter mode, etc.) before I^2C communication is established

In default mode, the I^2C registers are reset to the default values. The 27 min safety timer is reset and starts when DEFAULT mode is entered. The default value for V_{OREG} is 3.6V, and the default value for I_{CHARGE} is 1A. The input current limit is determined by the PSEL input. If PSEL selects adapter mode, there is no input current limit. If PSEL selects PC mode, the input current limit is set to 100mA. Default mode is exited by programming the I^2C interface. Startup into DEFAULT mode is shown in Figure 29. Note that if termination is enabled and charging has terminated, a new charge cycle is NOT initiated when entering DEFAULT mode.

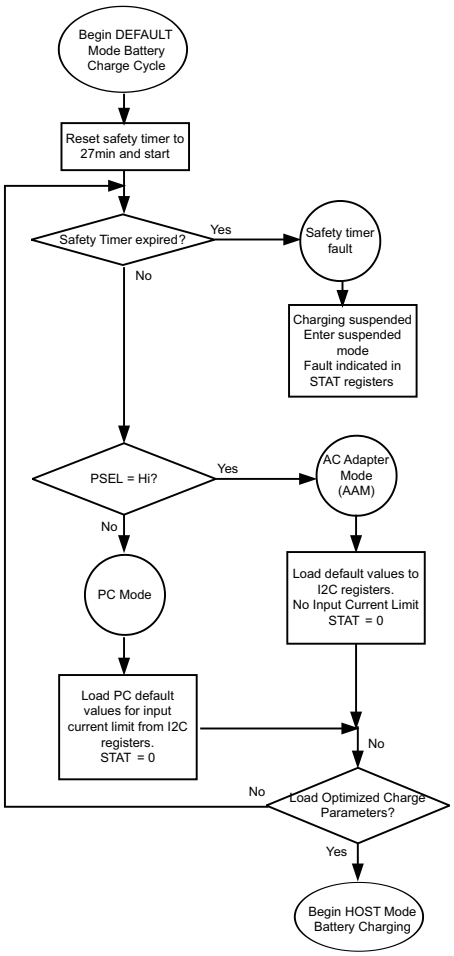


Figure 29. DEFAULT Mode Charging Process

Safety Timer and Watchdog Timer in Charge Mode

At the beginning of charging process, the bq24180 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is halted. The safety timer time is selectable using the I^2C interface. A single 128µs pulse is sent on the STAT and INT outputs and the STATx bits of the status registers are updated in the I^2C. The $\overline{EN}$ bit or power must be toggled in order to clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the V_{IN-DPM} Voltage/ Safety Timer Register. Changing the safety timer duration resets the safety timer.

In addition to the safety timer, the bq24180 contains a watchdog timer that monitors the host through the I^2C interface. Once a read/write is performed on the I^2C interface, a 12-second timer ($t_{WATCHDOG}$) is started. The 12-second timer is reset by the host using the I^2C interface. This is done by writing a "1" to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to “0” when the 12-second timer is reset. This process continues until battery is fully charged or the safety timer expires. If the 12-second timer expires, the IC enters DEFAULT mode where the default charge parameters are loaded, the safety timer restarts at 27 minutes and charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer as long as the 27 minute safety timer has not expired. Once the safety timer expires, charging is disabled. This function prevents continuous charging of a defective battery if the host fails to reset the safety timer. The watchdog timer flow chart is shown in Figure 30.

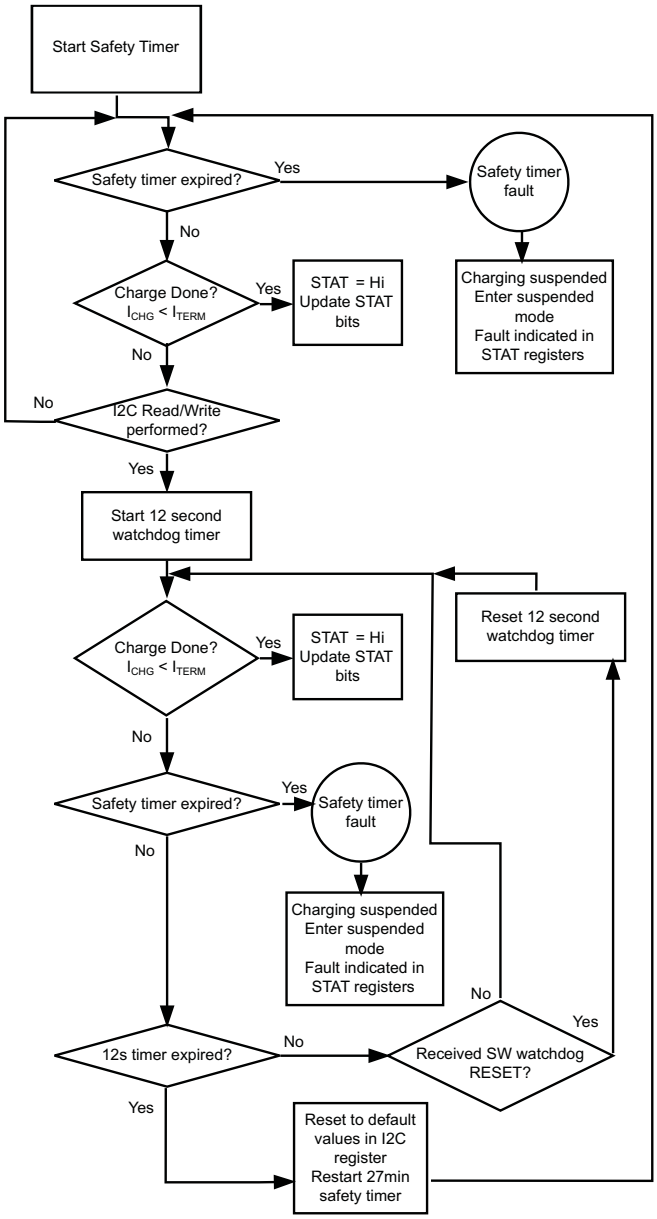


Figure 30. The Watchdog Timer Flow Chart for bq24180

Power Source Selector Input (PSEL)

The bq24180 contains a PSEL input that is used to program the input current limit during DEFAULT mode. Drive PSEL high to indicate a USB source is connected to the input and the PC mode default values should be used. When PSEL is high, the IC starts up with a 100mA input current limit and a 1A charge current. Drive PSEL low to indicate that an AC Adapter is connected to the input. When PSEL is high, the IC starts up with no input current limit and a 1A charge current. PSEL is internally pulled up to the DRV supply with a 100kΩ resistor.

Hardware Disable Input (CD)

The bq24180 contains a CD input that is used to disable the charger and place the bq24180 into high-impedance mode. Drive CD low to enable charge and enter normal operation. Drive CD high to disable charge and place the bq24180 into high-impedance mode. Driving CD high during DEFAULT mode resets the safety timer. Driving CD high during HOST mode suspends, but does NOT reset the safety timer. CD is internally pulled down to GND with a 100kΩ resistor.

LDO Output (DRV)

The bq24180 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.5V so it ideal to protect voltage sensitive USB circuits. The LDO is on whenever a VBUS supply is connected to the bq24180. The DRV is disabled under the following conditions:

1. Faulty adapter detected or VBUS < UVLO
2. Thermal Shutdown

AC Adapter Mode, Charge Current Limiting

After power is connected and startup is initiated, the PSEL input is read to determine the default startup values. If PSEL is 0, AC Adapter mode is selected. In AC Adapter mode, the charge current is regulated to maximize the charging time. The default parameters in AC Adapter mode are I_{CHARGE}=1A and V_{OUTREG}=3.6V. These values may be changed at any time using the I^2C interface. Additionally, if input current monitoring is required, this may be used during AC Adapter mode as well, but is disabled in DEFAULT mode.

PC Mode, Input Current Limiting

After power is connected and startup is initiated, the PSEL input is read to determine the default startup values. In PC mode, the input current is limited to maximize the charge rate of bq24180 without overloading the USB port. The input current for bq24180 can be limited to 100mA, 500mA or 800mA and is programmed in the control register. Once the input current reaches the input current limiting threshold, the charge current is reduced to prevent the input current from exceeding the programmed threshold. The input current sensing resistor and control loop are integrated into bq24180. The input current limit is disabled using I^2C control; refer to the definition of control register (01H) for detail. The default parameters in USB mode are I_{INLIM}=100mA and V_{OUTREG}=3.6V. Charge current may be monitored in PC mode as well, but by default it is set to a maximum such that the input current limit loop is active.

DCOUT Functionality

The bq24180 contains a DCOUT function that is used to connect a load to the battery through a switch. DCOUT is implemented using back to back MOSFETs (Q4 and Q5 in Figure 1) to connect DCOUT to the battery. This prevents reverse feeding the battery from DCOUT when DCOUT is disabled. DCOUT is a current limited source and can provide up to 1A to power additional accessories. The current limit is programmable from 370mA to 1.5A in 4 steps using the I^2C interface. Additionally, the DCOUT output is enabled or disabled using the I^2C interface. If the load on DCOUT reaches the current limit, the FET that connects DCOUT to the battery is turned off after the deglitch time (t_{dgl_DCOUT}), a single 128µs pulse is sent on the STAT and INT outputs and the FAULT_x bits of the status register are updated in the I^2C. The DCOUT may be enabled after the fault using the I^2C interface.

External NTC Monitoring (TS)

The bq24180 provides a TS input for monitoring an external NTC thermistor. A current is sourced to the NTC from the TS input and the voltage is monitored. There are 3 temperature thresholds that are monitored; the cold battery threshold (T_{NTC} < 5°C), the warm battery threshold (45°C < T_{NTC} < 55°C) and the hot battery threshold (T_{NTC} > 55°C). These temperatures correspond to the V_{HOT}, V_{WARM}, and V_{COLD} thresholds when using a 4.7kΩ NTC thermistor (β=3500). The TS input is monitored at all times, however, it only affects charging during default mode. During default mode, charging is suspended and timers are suspended when T_{NTC} < 5°C or T_{NTC} > 55°C. When 45°C < T_{NTC} < 55°C, the charging current is reduced to 400mA (max). In PC mode, the charge current remains at 100mA in this mode.

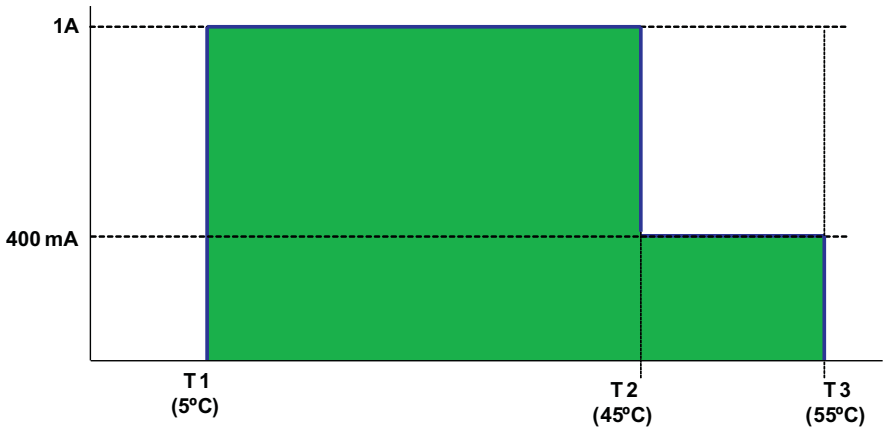


Figure 31. Charge Current During TS Conditions in Default Mode

When the bq24180 is not in default mode, the TS input is monitored and faults are displayed in the I^2C registers. If any of the 3 TS fault conditions occur, a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. The FAULT_x bits signal a general temperature fault. The TS_FAULTX bits in the NTC Monitor Register show the exact TS fault that has occurred.

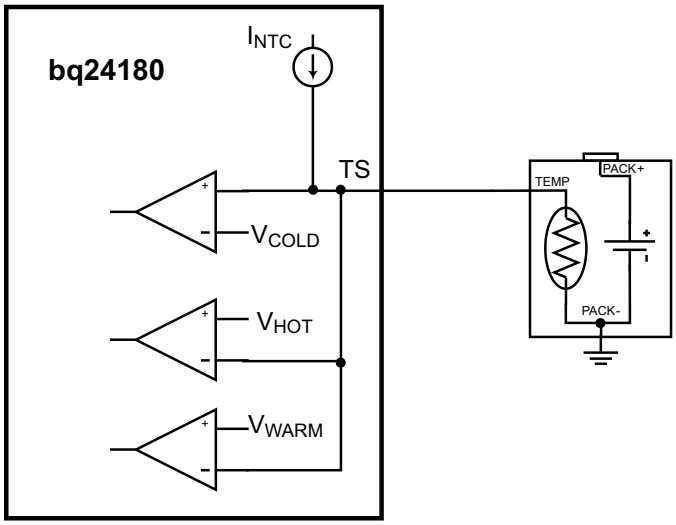


Figure 32. TS Circuit

Thermal Regulation and Protection

During the charging process, to prevent overheat of the chip, bq24180 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{CF}. The charge current is reduced to zero when the junction temperature increases about 10°C above T_{CF}. At any state, if T_J exceeds T_{SHTDWN}, bq24180 terminates charging and disables DCOUT in the I^2C register. During thermal shutdown mode, PWM is turned off, all timers are terminated and reset, and a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. A new charging cycle begins when T_J falls below T_{SHTDWN} by approximately 10°C. DCOUT must be enabled by the host after a thermal shutdown fault.

Input Voltage Protection in Charge Mode

Sleep Mode

The bq24180 enters the low-power sleep mode if the voltage on V_{VBUS} falls below sleep-mode entry threshold, $V_{CSOUT}+V_{SLP}$, and V_{VBUS} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{VBUS}. During sleep mode, both the reverse blocking switch Q1 and PWM are turned off. Once the input rises above the sleep threshold, the device returns to normal operation.

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, VBUS voltage will decease. Once the VBUS drops to V_{VBUS_LOW} (default 4.76V), the charge current is tapered down to prevent the further drop of VBUS. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set (B4 in Register 05H). This feature ensures IC compatibility with adapters with different current capabilities.

Faulty Adapter Detection

When an input source is connected to the bq24180, the device enter faulty adapter detection mode. In this mode, the IC sources 30mA to the battery for t_{INT}. After t_{INT}, the input voltage is monitored. If $V_{VBUS}>V_{IN(MIN)}$, the device continues the startup sequence. If $V_{VBUS}<V_{IN(MIN)}$, a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C and the process repeats until a good adapter is detected.

High-Input and Input Over-Voltage Protection

The bq24180 provides two levels over-voltage protection on the input. A high-input comparator disables the PWM operation and sources the 50mA precharge current to the battery when $V_{HIGH} < V_{VBUS} < V_{OVP}$. This allows for unregulated adapters to be used. The 50mA pulls the adapter voltage down to the usable voltage and then normal operation begins.

The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from V_{VBUS} to PGND). When $V_{VBUS} > V_{OVP}$, the bq24180 latches off the PWM converter, a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. Once the OVP fault is removed, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

Charge Status Outputs (STAT, INT)

The STAT and INT outputs are used to indicate operation conditions for bq24180. STAT and INT are pulled low during charging when EN_STAT bit in the control register (00H) is set to “1”. When charge is complete or disabled, INT and STAT are high impedance. When a fault occurs, a 128-µs pulse (interrupt) is sent out to notify the host. The status of STAT and INT during different operation conditions is summarized in Table 1. STAT drives an LED for visual indication. INT is available for connecting to the logic rail for host communication.

Table 1. STAT Pin Summary

CHARGE STATE	STAT and INT BEHAVIOR
Charge in progress and EN_STAT=1	Low
Other normal conditions	Open-drain
Charge mode faults: Timer fault, sleep mode, VBUS over voltage, VBUS UVLO, thermal shutdown	128-µs pulse, then open-drain

Control Bits in Charge Mode

$\overline{CE}$ Bit (Charge Enable)

The bit of $\overline{CE}$ in control register is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge.

RESET Bit

The bit of RESET in control register is used to reset all the charge parameters. Write '1" to RESET bit to reset all the charge parameters to default values and RESET bit is automatically cleared to zero once the charge parameters get reset. It is designed for charge parameter reset before charge starts and it is not recommended to set RESET bit when charging or boosting in progress.

Output Inductor and Capacitor Selection Guidelines

The bq24180 provides internal loop compensation. With this scheme, best stability occurs when LC resonant frequency, of, is approximately 40 kHz (20 kHz to 80 kHz). Equation 1 can be used to calculate the value of the output inductor, L_{OUT}, and output capacitor, C_{OUT}.

$$f_o = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 4.7µF and 47µF is recommended for C_{OUT}, refer to the application section for components selection.

Selecting Current Sense Resistor

Both the termination current range and charge current range are depending on the sensing resistor (R_{SNS}). The termination current step (I_{OTERM_STEP}) can be calculated using Equation 2:

$$I_{OTERM\_STEP} = \frac{V_{ITERM0}}{R_{SNS}} \quad (2)$$

Table 2 shows the termination current settings with two sensing resistors.

Table 2. Termination Current Settings for 68mΩ and 100mΩ Sense Resistors

BIT	V_{ITERM} (mV)	I_{TERM} (mA) R_{SNS} = 68 mΩ	I_{TERM} (mA) R_{SNS} = 100 mΩ
V_{ITERM2}	6.8	100	68
V_{ITERM1}	3.4	50	43
V_{ITERM0}	1.7	25	17
Offset	1.7	25	17

The charge current step ($I_{OCHARGE\_STEP}$) can be calculated using Equation 3:

$$I_{OCHARGE\_STEP} = \frac{V_{ICHRG0}}{R_{SNS}} \quad (3)$$

Table 3 shows the charge current settings with two sensing resistors.

Table 3. Charge Current Settings for 68 mΩ and 100 mΩ Sense Resistors

BIT	V_{IREG} (mV)	$I_{OCHARGE}$ (mA) R_{SNS} = 68 mΩ	$I_{OCHARGE}$ (mA) R_{SNS} = 100 mΩ
V_{ICHRG3}	54.4	800	544
V_{ICHRG2}	27.2	400	272
V_{ICHRG1}	13.6	200	136
V_{ICHRG0}	6.8	100	68
Offset	37.4	550	374

SERIAL INTERFACE DESCRIPTION

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq24180 device works as a slave and is compatible with the following data transfer modes, as defined in the I²C Bus™ Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as battery voltage remains above 2.5 V (typical). The I²C circuitry is powered from VBUS when a supply is connected. If the VBUS supply is not connected, the I²C circuitry is powered from the battery through CSOUT. The battery voltage must stay above 2.5V with no input connected in order to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as the HS-mode. The bq24150/1 device only supports 7-bit addressing. The device 7-bit address is defined as '1101011' (6BH).

F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 33. All I2C -compatible devices should recognize a start condition.

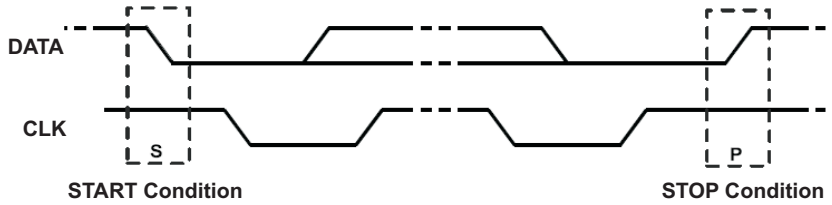


Figure 33. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 34). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 34) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

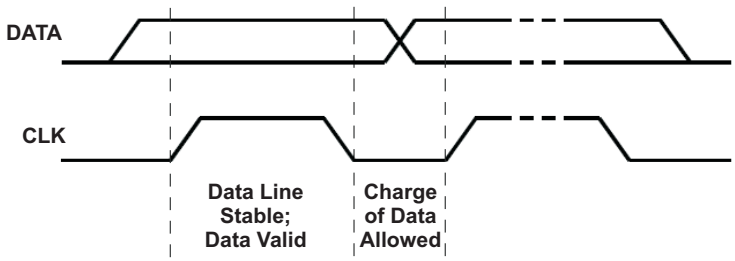


Figure 34. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the

receiver. the 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 35). This releases the bus and stops the communication link with the addressed slave. All I2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I2C logic from remaining in a incorrect state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

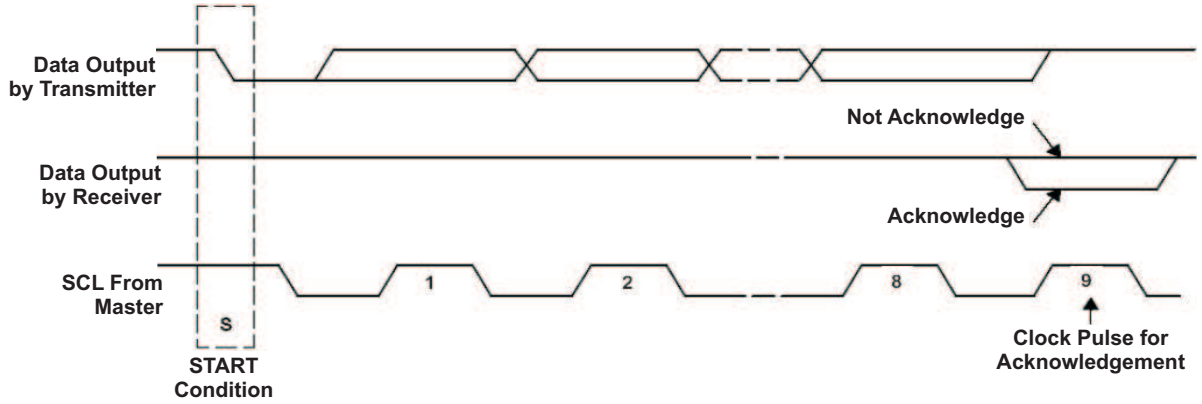


Figure 35. Acknowledge on the I2C Bus

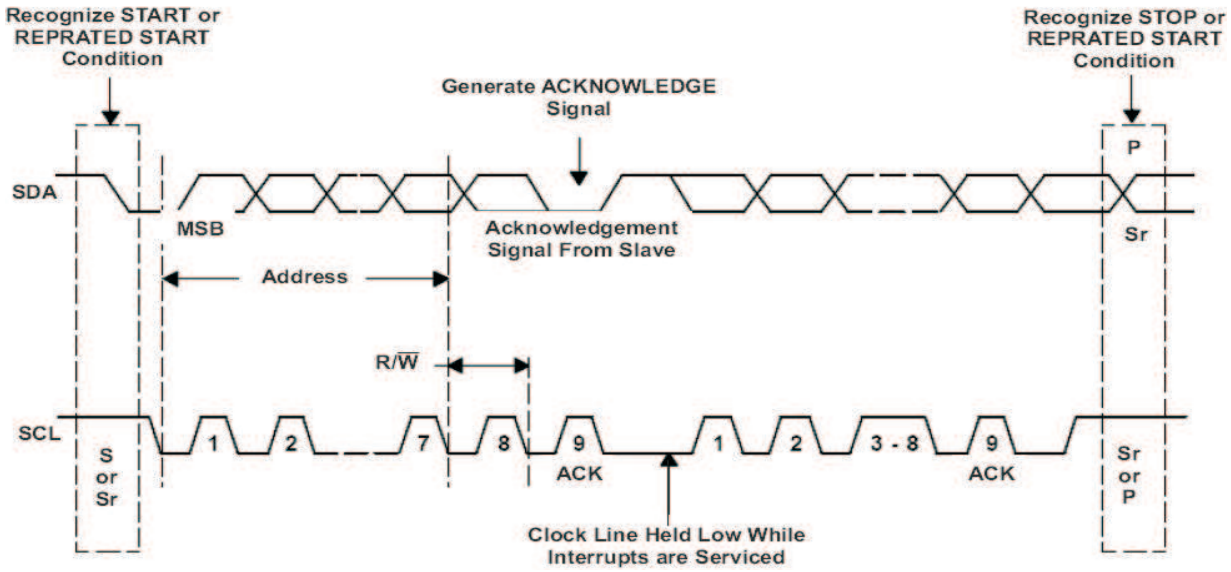


Figure 36. Bus Protocol

F/S Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code '00001XXX'. This transmission is made in F/S mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS mode and switches all the internal settings of the slave devices to support the F/S mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS mode. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I2C logic from remaining in a incorrect state.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

REGISTER DESCRIPTION

Status/Control Register (READ/WRITE) – Memory location: 00, Reset state: x1xx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	TMR_RST	Read/Write	Write: TMR_RST function, write "1" to reset the watchdog timer (auto clear) Read: 0 – PSEL indicates low, 1- PSEL indicates high
B6	EN_STAT	Read/Write	1-Enable STAT function, 0-Disable STAT function (default 1)
B5	STAT2	Read only	00-Ready, 01-Charge in progress, 10-Charge done, 11-Fault
B4	STAT1	Read only	
B3	NA	Read only	NA
B2	FAULT_3	Read only	Charge mode: 000-Normal, 001-VBUS OVP, 010-Sleep mode, 011- Faulty Adapter or VBUS<V_{UVLO}, 100-DCOUT Current Limit tripped, 101-Thermal shutdown or TS Fault, 110-Timer fault, 111-No battery
B1	FAULT_2	Read only	
B0(LSB)	FAULT_1	Read only	

Control Register (READ/WRITE) – Memory location: 01, Reset state: 0011 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	Iin_Limit_2	Read/Write	00-USB host with 100-mA current limit, 01-USB host with 500-mA current limit, 10-USB host/charger with 800-mA current limit, 11-No input current limit (default 00(1))
B6	Iin_Limit_1	Read/Write	
B5	DCOUT_ILIM1	Read/Write	00-DCOUT 350mA current limit, 01- DCOUT 750mA current limit, 10- DCOUT 1050mA current limit, 11- DCOUT 1400mA current limit (default 11)
B4	DCOUT_ILIM2	Read/Write	
B3	TE	Read/Write	1-Enable charge current termination, 0-Disable charge current termination (default 0)
B2	$\overline{CE}$	Read/Write	1-Charger is disabled, 0-Charger enabled (default 0)
B1	HZ_MODE	Read/Write	1-High impedance mode, 0-Not high impedance mode (default 0)
B0 (LSB)	DCOUT_EN	Read/Write	1-DCOUT Enabled, 0-DCOUT Disabled. (default 0)
(1) When in DEFAULT mode, the PSEL input determines the input current limit.			

Control/Battery Voltage Register (READ/WRITE) – Memory location: 02, Reset state: 0001 01XX

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	V_{OREG5}	Read/Write	Battery Regulation Voltage: 640mV (default 0)
B6	V_{OREG4}	Read/Write	Battery Regulation Voltage: 320mV (default 0)
B5	V_{OREG3}	Read/Write	Battery Regulation Voltage: 160mV (default 0)
B4	V_{OREG2}	Read/Write	Battery Regulation Voltage: 80mV (default 1)
B3	V_{OREG1}	Read/Write	Battery Regulation Voltage: 40mV (default 0)
B2	V_{OREG0}	Read/Write	Battery Regulation Voltage: 20mV (default 1)
B1	NA	Read/Write	NA
B0(LSB)	NA	Read/Write	NA

- Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 3.6V).

Vender/Part/Revision Register (READ only) – Memory location: 03, Reset state: 0100 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	Vender2	Read only	Vender Code: bit 2 (default 0)
B6	Vender1	Read only	Vender Code: bit 1 (default 1)
B5	Vender0	Read only	Vender Code: bit 0 (default 0)
B4	PN1	Read only	For I^2C Address 6BH: 00 – bq24180
B3	PN0	Read only	
B2	Revision2	Read only	000: Revision 1.0; 001: Revision 1.1 010-111: Future Revisions
B1	Revision1	Read only	
B0(LSB)	Revision0	Read only	

Battery Termination/Fast Charge Current Register (READ/WRITE)
Memory location: 04, Reset state: 1010 1011

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	Reset	Write only	Write: 1-Charger in reset mode, 0-No effect Read: always get "1"
B6	V_{ICHRG3}	Read/Write	Charge current sense voltage: 54.4mV— (default 0)
B5	V_{ICHRG2}	Read/Write	Charge current sense voltage: 27.2mV—(default 1)
B4	V_{ICHRG1}	Read/Write	Charge current sense voltage: 13.6mV— (default 0)
B3	V_{ICHRG0}	Read/Write	Charge current sense voltage: 6.8mV (default 1)
B2	V_{ITERM2}	Read/Write	Termination current sense voltage: 6.8mV (default 0)
B1	V_{ITERM1}	Read/Write	Termination current sense voltage: 3.4mV (default 1)
B0(LSB)	V_{ITERM0}	Read/Write	Termination current sense voltage: 1.7mV (default 1)

- Charge current sense voltage offset is 37.4mV and default charge current is 1050mA, if 68mΩ sense resistor is used.
- Termination threshold voltage offset is 1.7mV and default termination current is 100mA if a 68mΩ sense resistor is used.

V_{IN-DPM} Voltage/ Safety Timer Register – Memory location: 05, Reset state: XX0X X111

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	NA	Read/Write	NA
B6	NA	Read/Write	NA
B5	LOW_CHG	Read/Write	1 – Low charge current sense voltage of 23.8mV, 0 – Normal charge current sense voltage at 04H (default 0)
B4	DPM_STATUS	Read Only	1 – V_{IN}-DPM mode is active, 0 – V_{IN}-DPM mode is not active
B3	CD_STATUS	Read Only	1 – CD high, Charger disabled, 0 – CD low, Charger enabled
B2	V_{INDPM2}	Read/Write	V_{IN-DPM} voltage: 320 mV (default 1)
B1	V_{INDPM1}	Read/Write	V_{IN-DPM} voltage: 160 mV (default 1)
B0(LSB)	V_{INDPM0}	Read/Write	V_{IN-DPM} voltage: 80 mV (default 1)

- V_{IN-DPM} voltage offset is 4.15V and default V_{IN-DPM} threshold is 4.71V.

Safety Limit Register (READ/WRITE, Write only once after reset!)
Memory location: 06, Reset state: 0101 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	V_{MCHRG3}	Read/Write	Maximum charge current sense voltage: 54.4mV (default 0)
B6	V_{MCHRG2}	Read/Write	Maximum charge current sense voltage: 27.2mV (default 1)
B5	V_{MCHRG1}	Read/Write	Maximum charge current sense voltage: 13.6mV (default 0)
B4	V_{MCHRG0}	Read/Write	Maximum charge current sense voltage: 6.8mV (default 1)
B3	V_{MREG3}	Read/Write	Maximum battery regulation voltage: 160mV (default 0)
B2	V_{MREG2}	Read/Write	Maximum battery regulation voltage: 80mV (default 0)
B1	V_{MREG1}	Read/Write	Maximum battery regulation voltage: 40mV (default 0)
B0(LSB)	V_{MREG0}	Read/Write	Maximum battery regulation voltage: 20mV (default 0)

- Maximum charge current sense voltage offset is 550mA (default at 950mA) and the maximum charge current option is 1.55A, if 68-mΩ sensing resistor is used.
- Maximum battery regulation voltage offset is 4.2V (default at 4.2V) and maximum battery regulation voltage option is 4.44V.
- Memory location 06 resets only when V_{BAT} voltage drops below V_{SHORT} threshold (typ. 2.0V) goes to logic '0'. During reset, the maximum values in 06H keep the default value regardless of the write action to this register. After reset (V_{BAT}>V_{SHORT}), the maximum values for battery regulation voltage and charge current can be programmed many times until any writing to other register locks the safety limits. Programmed values exclude higher values from memory locations 02 (battery regulation voltage), and from memory location 04 (Fast charge current).

  If host accesses (write command) to some other register before Safety limit register, the default values hold!

NTC Monitor Register (READ/WRITE) – Memory location: 07, Reset state: 100X 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	2XTMR_EN	Read/Write	1 – Timer slowed by 2x when in thermal regulation or VIN_HIGH protection, 0 – Timer not slowed at any time (default 1)
B6	TMR_1	Read/Write	Safety Timer Time Limit 00 – 27 minute fast charge, 01 – 3 hour fast charge, 10 – 6 hour fast charge, 11 – Disable safety timers (default 00)
B5	TMR_2	Read/Write	
B4	NA	Read/Write	NA
B3	TS_/EN	Read/Write	1 – TS function disabled, 0 – TS function enabled (default 0)
B2	TS_FAULT2	Read only	TS Fault Mode: 000 – TS temp < 5°C or TS temp > 55°C, 010 – Normal, No TS fault, 011 – 45°C < TS temp < 55°C, 100–111 – TS Open
B1	TS_FAULT1	Read only	
B0(LSB)	TS_FAULT0	Read only	

POWER TOPOLOGIES

System Load After Sensing Resistor

One of the simple high-efficiency topologies connects the system load directly across the battery pack, as shown in Figure 37. The input voltage has been converted to a usable system voltage with good efficiency from the input. When the input power is on, it supplies the system load and charges the battery pack at the same time. When the input power is off, the battery pack powers the system directly.

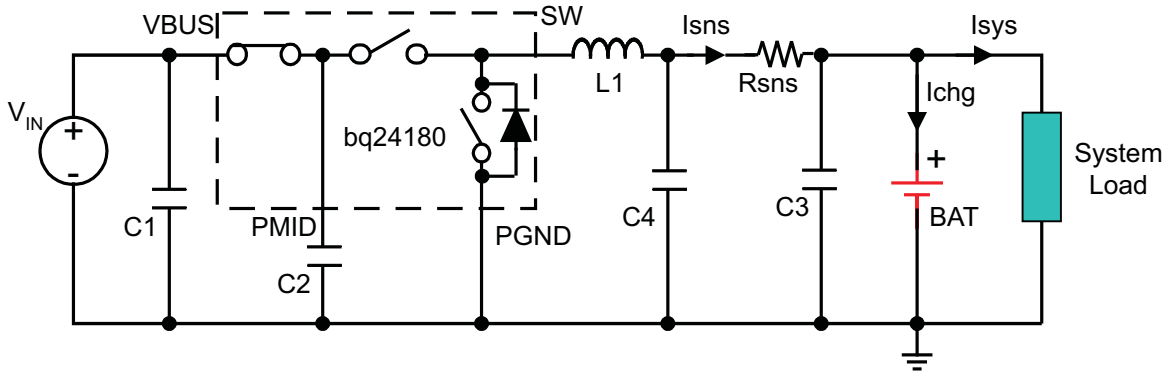


Figure 37. System Load After Sensing Resistor

The advantages:

- When the AC adapter is disconnected, the battery pack powers the system load with minimum power dissipations. Consequently, the time that the system runs on the battery pack can be maximized.
- It saves the external path selection components and offers a low-cost solution.
- Dynamic power management (DPM) can be achieved. The total of the charge current and the system current can be limited to a desired value by adjusting charge current. When the system current increases, the charge current drops by the same amount. As a result, no potential over-current or over-heating issues are caused by excessive system load demand.
- The total of the input current can be limited to a desired value by setting input current limit value. So USB specifications can be met easily.
- The supply voltage variation range for the system can be minimized.
- The input current soft-start can be achieved by the generic soft-start feature of the IC.

Design considerations and potential issues:

- If the system always demands a high current (but lower than the regulation current), the charging never terminates. Thus, the battery is always charged, and the lifetime may be reduced.
- Because the total current regulation threshold is fixed and the system always demands some current, the battery may not be charged with a full-charge rate and thus may lead to a longer charge time.
- If the system load current is large after the charger has been terminated, the voltage drop across the battery impedance may cause the battery voltage to drop below the refresh threshold and start a new charge. The charger would then terminate due to low charge current. Therefore, the charger would cycle between charging and terminating. If the load is smaller, the battery has to discharge down to the refresh threshold, resulting in a much slower cycling.
- In a charger system, the charge current is typically limited to about 10mA, if the sensed battery voltage is below 2V short circuit protection threshold. This results in low power availability at the system bus. If an external supply is connected and the battery is deeply discharged, below the short circuit protection threshold, the charge current is clamped to the short circuit current limit. This then is the current available to the system during the power-up phase. Most systems cannot function with such limited supply current, and the battery supplements the additional power required by the system. Note that the battery pack is already at the depleted condition, and it discharges further until the battery protector opens, resulting in a system shutdown.
- If the battery is below the short circuit threshold and the system requires a bias current budget lower than the short circuit current limit, the end-equipment will be operational, but the charging process can be affected depending on the current left to charge the battery pack. Under extreme conditions, the system current is

close to the short circuit current levels and the battery may not reach the fast-charge region in a timely manner. As a result, the safety timers flag the battery pack as defective, terminating the charging process. Because the safety timer cannot be disabled, the inserted battery pack must not be depleted to make the application possible.

- For instance, if the battery pack voltage is too low, highly depleted, or totally dead or even shorted, the system voltage is clamped by the battery and it cannot operate even if the input power is on.

System Load Before Sensing Resistor

The second circuit is very similar to first one; the difference is that the system load is connected before the sense resistor, as shown in Figure 38.

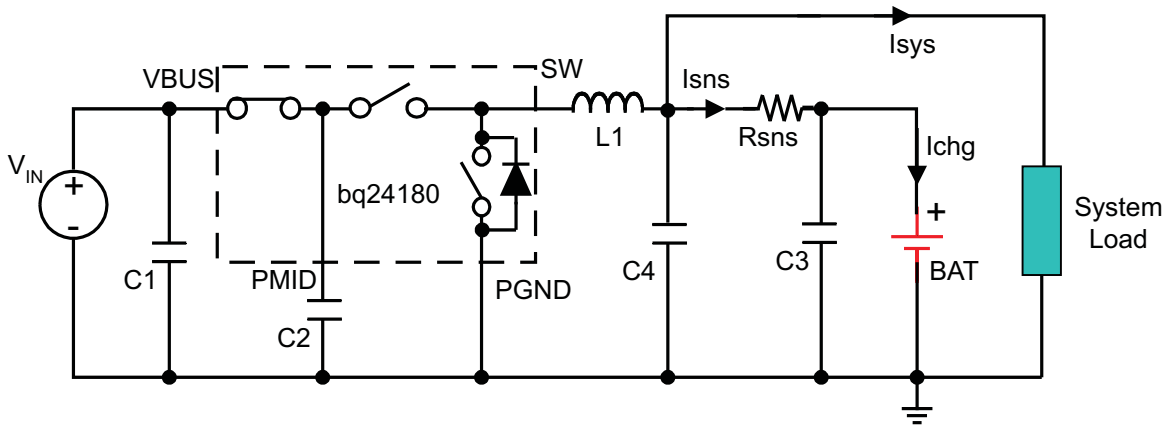


Figure 38. System Load Before Sensing Resistor

The advantages of system load before sensing resistor to system load after sensing resistor:

- The charger controller is based only on the current goes through the current-sense resistor. So, the constant current fast charge and termination functions work well, and are not affected by the system load. This is the major advantage of it.
- A depleted battery pack can be connected to the charger without the risk of the safety timer expiration caused by high system load.
- The host charger can disable termination and keep the converter running to keep battery fully charged, or let the switcher terminate when the battery is full and then run off of the battery via the sense resistor.

Design considerations and potential issues:

- The total current is limited by the IC input current limit, or peak current protection, or the thermal regulation but not the charge current setting. The charge current does not drop when the system current load increases until the input current limit is reached. This solution is not applicable if the system requires a high current.
- Efficiency declines when discharging through the sense resistor to the system.

DESIGN EXAMPLE FOR TYPICAL APPLICATION CIRCUITS

Systems Design Specifications:

- VBUS = 5 V
- $V_{(BAT)}$ = 4.2 V (1-Cell)
- $I_{(charge)}$ = 1.25 A
- Inductor ripple current = 30% of fast charge current

1. Determine the inductor value (L_{OUT}) for the specified charge current ripple:

$$L_{OUT} = \frac{VBAT \times (VBUS - VBAT)}{VBUS \times f \times \Delta I_L}$$

, the worst case is when battery voltage is as close as to half of the input voltage.

$$L_{OUT} = \frac{2.5 \times (5 - 2.5)}{5 \times (3 \times 10^6) \times 1.25 \times 0.3} \quad (4)$$

L_{OUT} = 1.11 µH

Select the output inductor to standard 1 µH. Calculate the total ripple current with using the 1-µH inductor:

$$\Delta I_L = \frac{VBAT \times (VBUS - VBAT)}{VBUS \times f \times L_{OUT}} \quad (5)$$

$$\Delta I_L = \frac{2.5 \times (5 - 2.5)}{5 \times (3 \times 10^6) \times (1 \times 10^{-6})} \quad (6)$$

ΔI_L = 0.42 A

Calculate the maximum output current:

$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

$$I_{LPK} = 1.25 + \frac{0.42}{2} \quad (8)$$

I_{LPK} = 1.46 A

Select 2.5mm by 2.0mm 1-µH 1.5-A surface mount multi-layer inductor. The suggested inductor part numbers are shown as following.

Table 4. Inductor Part Numbers

PART NUMBER	INDUCTANCE	SIZE	MANUFACTURER
LQM2HPN1R0MJ0	1 µH	2.5 x 2.0 mm	muRata
MIPS2520D1R0	1 µH	2.5 x 2.0 mm	FDK
MDT2520-CN1R0M	1 µH	2.5 x 2.0 mm	TOKO
CP1008	1 µH	2.5 x 2.0 mm	Inter-Technical

2. Determine the output capacitor value C_{OUT} using 40 kHz as the resonant frequency:

$$f_o = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (9)$$

$$C_{OUT} = \frac{1}{4\pi^2 \times f_0^2 \times L_{OUT}} \quad (10)$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (40 \times 10^3)^2 \times (1 \times 10^{-6})} \quad (11)$$

C_{OUT} = 15.8 µF

Select two 0603 X5R 6.3V 10-µF ceramic capacitors in parallel i.e., muRata GRM188R60J106M.

3. Determine the sense resistor using the following equation:

$$R_{(SNS)} = \frac{V_{(RSNS)}}{I_{(CHARGE)}} \quad (12)$$

The maximum sense voltage across sense resistor is 85 mV. In order to get a better current regulation accuracy, $V_{(RSNS)}$ should equal 100mV, and calculate the value for the sense resistor.

$$R_{(SNS)} = \frac{85mV}{1.25A} \quad (13)$$

$R_{(SNS)}$ = 68 mΩ

This is a standard value. If it is not a standard value, then choose the next close value and calculate the real charge current. Calculate the power dissipation on the sense resistor:

$P_{(RSNS)} = I_{(CHARGE)}^{2} \times R_{(SNS)}$

$P_{(RSNS)} = 125^{2} \times 0.068$

$P_{(RSNS)} = 0.106$ W

Select 0805 0.25-W 68-mΩ 2% sense resistor, i.e. Sosomu RL122OT-R068-G or RL0816T-R068-F 68-mΩ, 0.125W, 0603, 1%.

PCB LAYOUT CONSIDERATION

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from input to PGND, should be placed as close as possible to the bq24180. The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high frequency oscillation problems, proper layout to minimize high frequency current path loop is critical (see Figure 39). The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS(R1) back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path, see Figure 40).
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small-signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into VBUS, PMID and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- Place 4.7μF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1μF input capacitor as close to VBUS pin and PGND pin as possible to make high frequency current loop area as small as possible (see Figure 41).

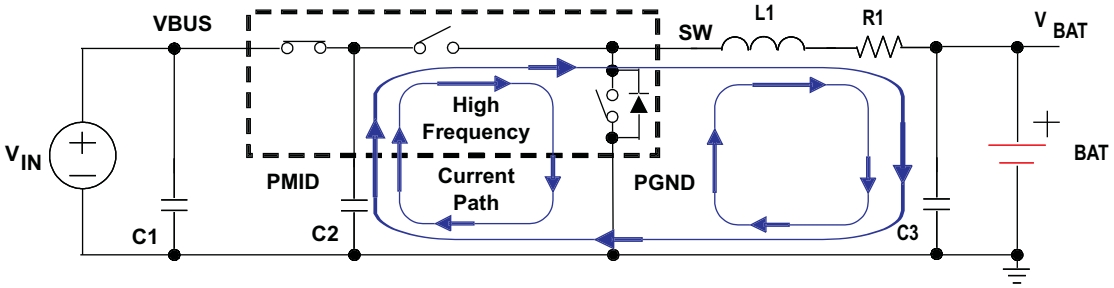


Figure 39. High Frequency Current Path

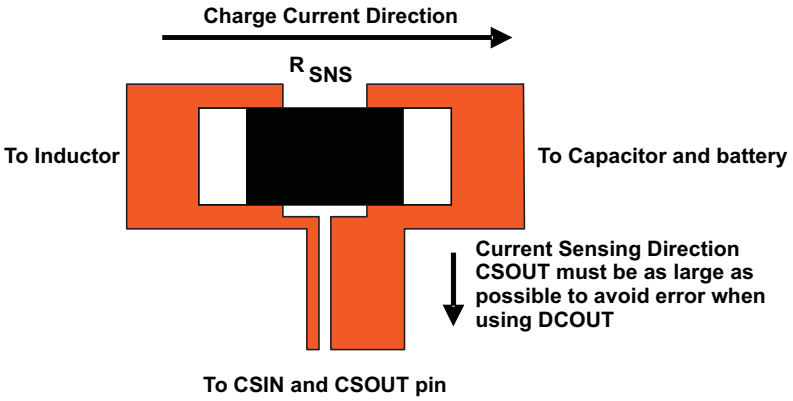


Figure 40. Sensing Resistor PCB Layout

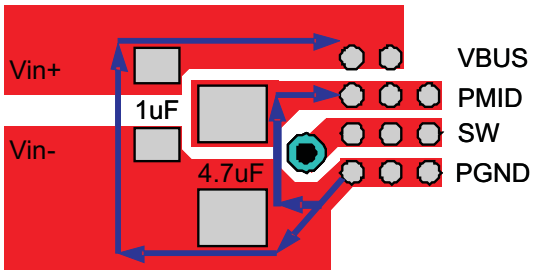
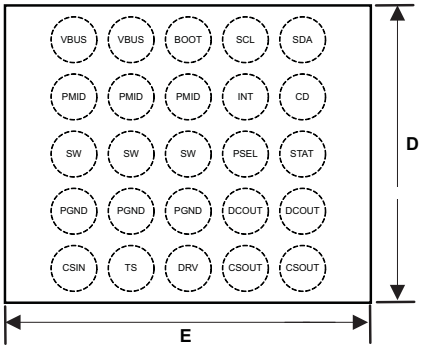


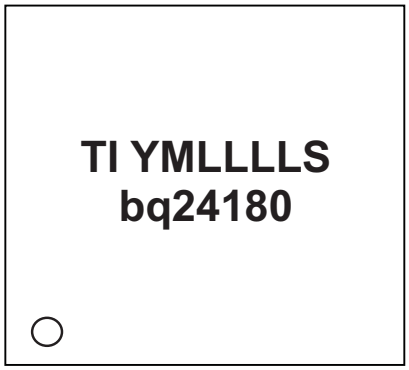
Figure 41. Input Capacitor Position and PCB Layout Example

PACKAGE SUMMARY

WCSP PACKAGE
(Top View)



CHIP SCALE PACKAGE
(Top Side Symbol For bq24180)



0-Pin A1 Marker, TI-TI Letters, YM- Year Month Date Code, LLLL-Lot Trace Code, S-Assembly Site Code

CHIP SCALE PACKAGING DIMENSIONS

The bq24180 devices are available in a 20-bump chip scale package (YFF, NanoFree™). The package dimensions are:

- D = 2.2 ± 0.05 mm
- E = 2.4 ± 0.05 mm

REVISION HISTORY

Changes from Original (February 2010) to Revision A	Page
• Changed ±7 to "-0.3 to 7 V" for "Voltage difference between BOOT and SW inputs (VBOOT –VSW)" parameter of the Absolute Maximum Ratings table.	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24180YFFR	Active	Production	DSBGA (YFF) | 25	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ24180
BQ24180YFFT	Active	Production	DSBGA (YFF) | 25	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ24180

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

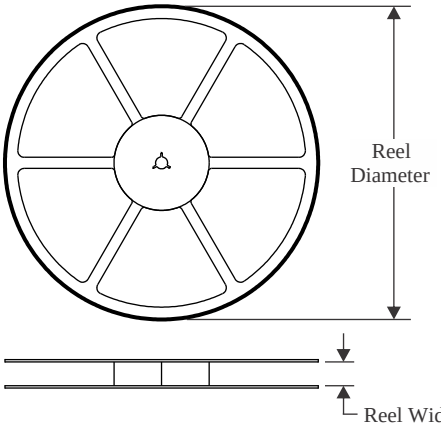
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

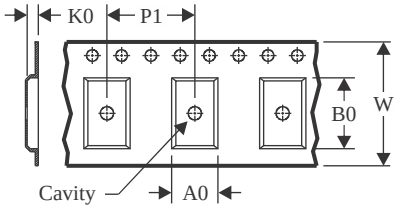
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

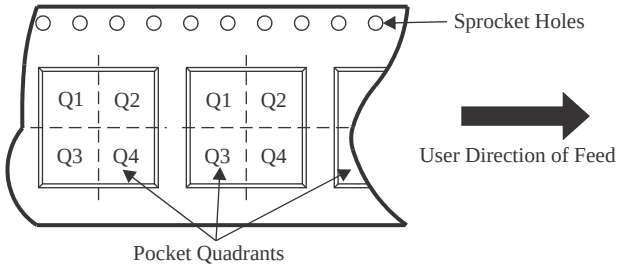


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

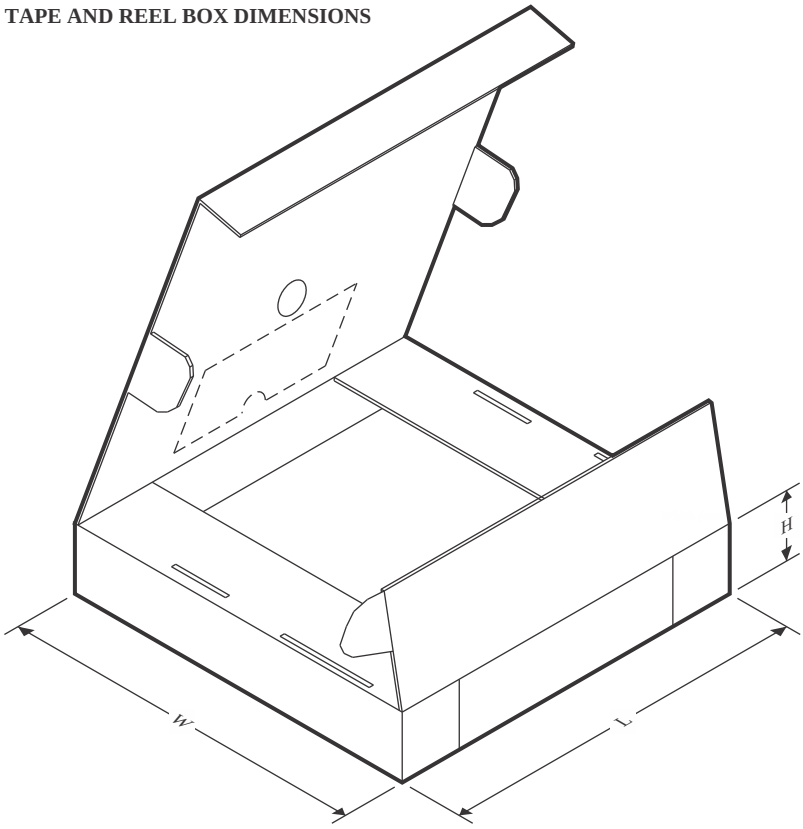
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

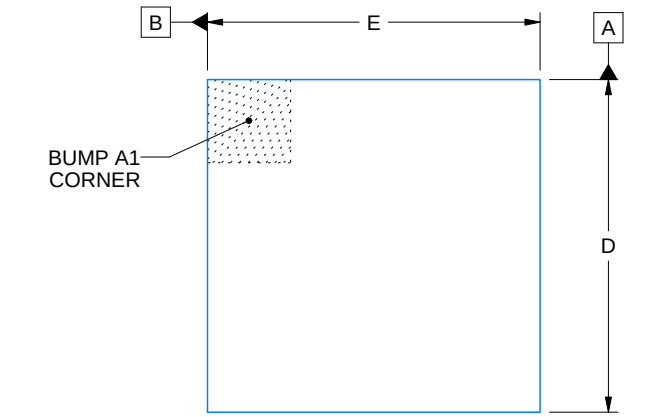
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24180YFFR	DSBGA	YFF	25	3000	180.0	8.4	2.38	2.4	0.8	4.0	8.0	Q1
BQ24180YFFT	DSBGA	YFF	25	250	180.0	8.4	2.38	2.4	0.8	4.0	8.0	Q1

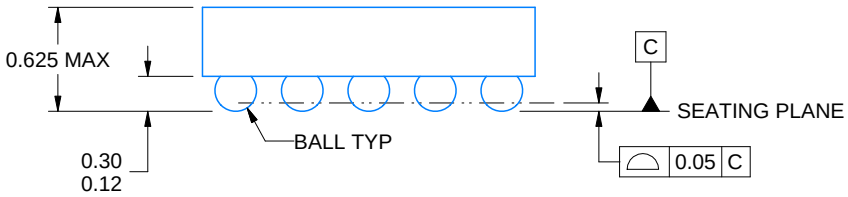
TAPE AND REEL BOX DIMENSIONS

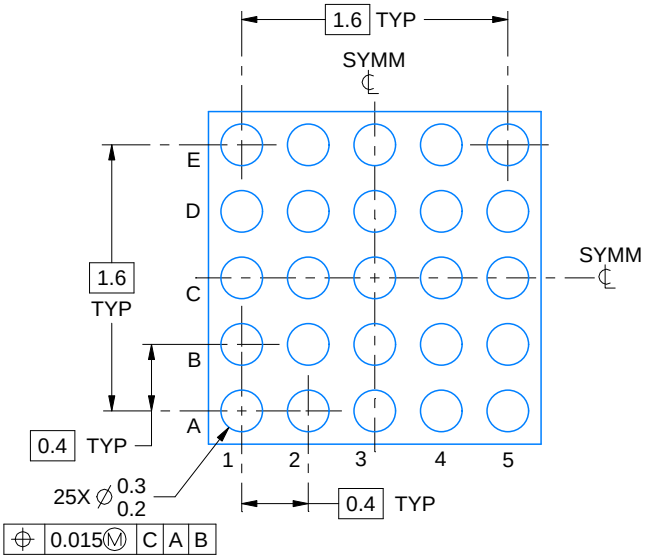


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24180YFFR	DSBGA	YFF	25	3000	182.0	182.0	20.0
BQ24180YFFT	DSBGA	YFF	25	250	182.0	182.0	20.0







D: Max = 2.398 mm, Min =2.338 mm

E: Max = 2.184 mm, Min =2.124 mm

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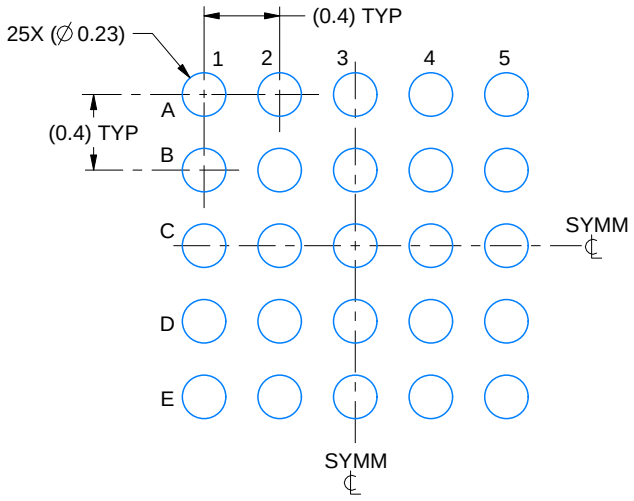
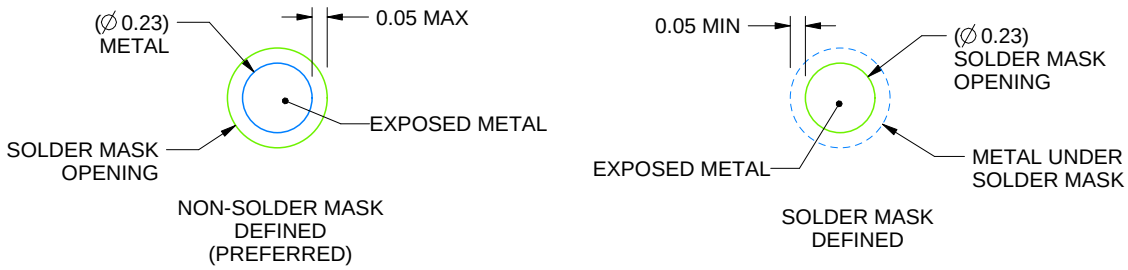
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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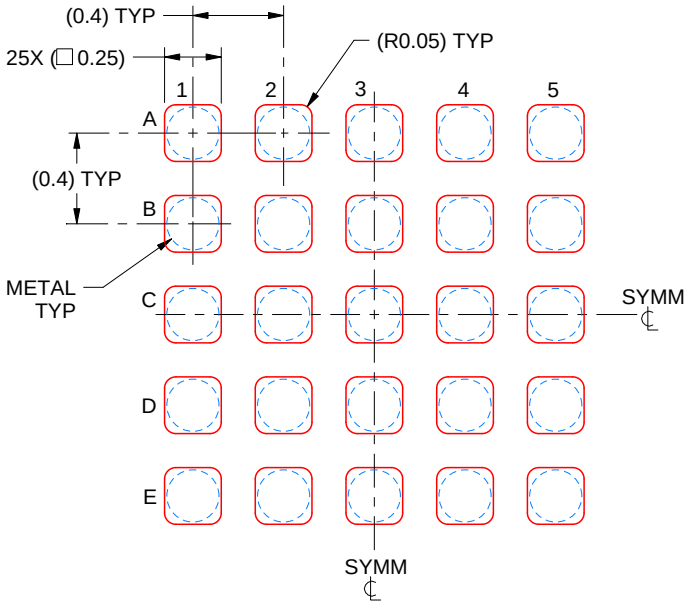
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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