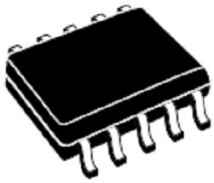
HVLED001B

High power factor flyback controller with constant voltage primary-sensing and ultra-low standby consumption

Datasheet - Production data



SSOP10

Features

- Quasi resonant (QR) topology
- Primary side regulation of output voltage
- Direct optocoupler connection for current loop regulation with feedback disconnection detection
- 800 V high voltage startup
- High power factor and low THD in universal range
- High efficiency and output stability in wide voltage and current range
- Extremely low standby power at no load condition
- Programmable frequency foldback
- Integrated input voltage detection for high power factor capability and protection triggering
- Latch-free device guarantee by smart auto-reload timer (ART)
- 0-10 and PWM dimming compatible
- Remote control pin

Applications

- Single-stage LED drivers with high power factor
- Two-stage LED drivers

Description

The HVLED001B is an enhanced peak current mode controller able to control mainly high power factor (HPF) flyback or buck-boost. Some other topologies such as buck, boost and SEPIC, can also be implemented.

Primary side regulation and optocoupler control can be applied independently on the chip, both exploiting precise regulation and very low standby power during no load conditions.

The innovative ST high voltage technology allows direct connection of the HVLED001B to the input voltage in order to both start up the device and to monitor the input voltage, without the need for external components.

Abnormal conditions like open circuit, output short-circuit, input over-voltage or under-voltage and circuit failures like open loop and overcurrent of the main switch are effectively controlled.

A smart Auto Recover Timer (ART) function is built in to guarantee an automatic application recovery, without any loss of reliability.

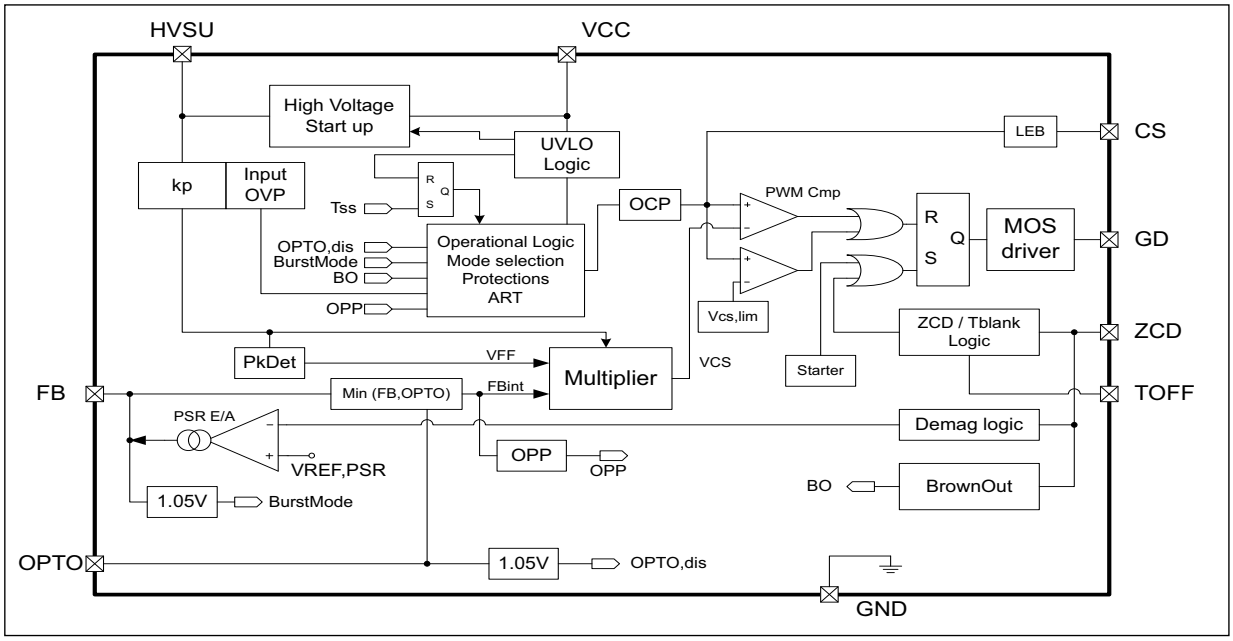
Table 1. Device summary

Order code	Package	Packaging
HVLED001BY	SSOP10	Tube
HVLED001BTR		Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Typical application - HPF flyback

Figure 2. Primary side regulated (PSR) application

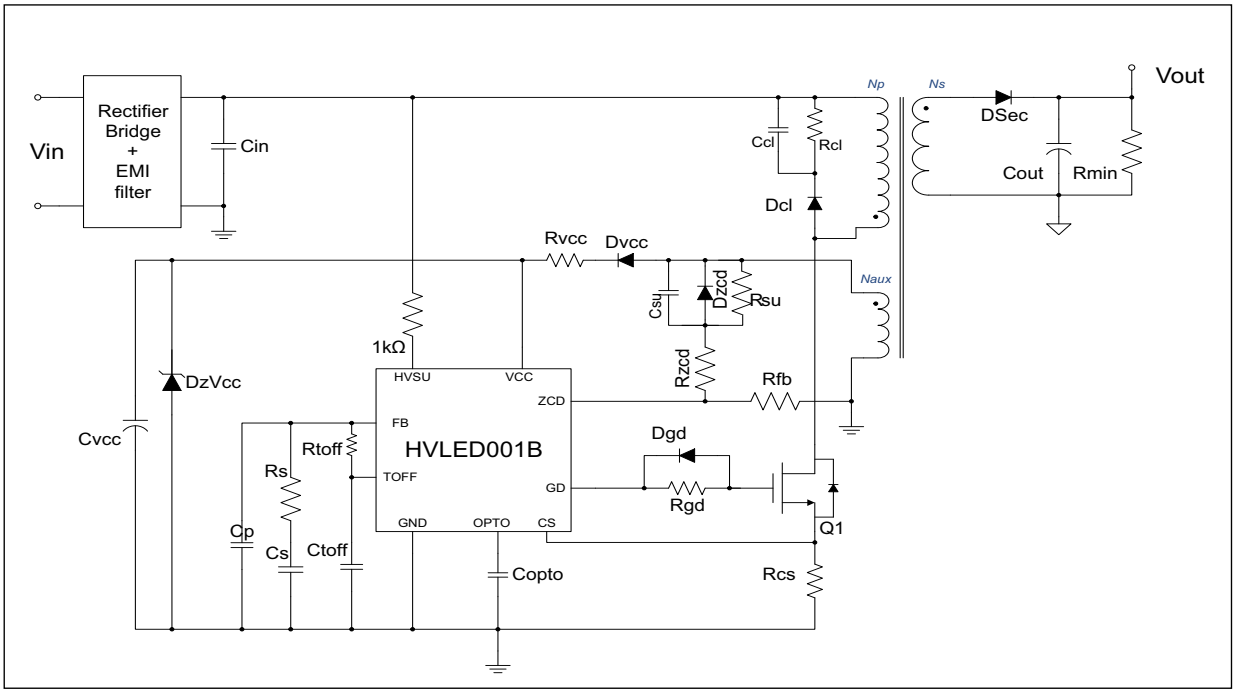
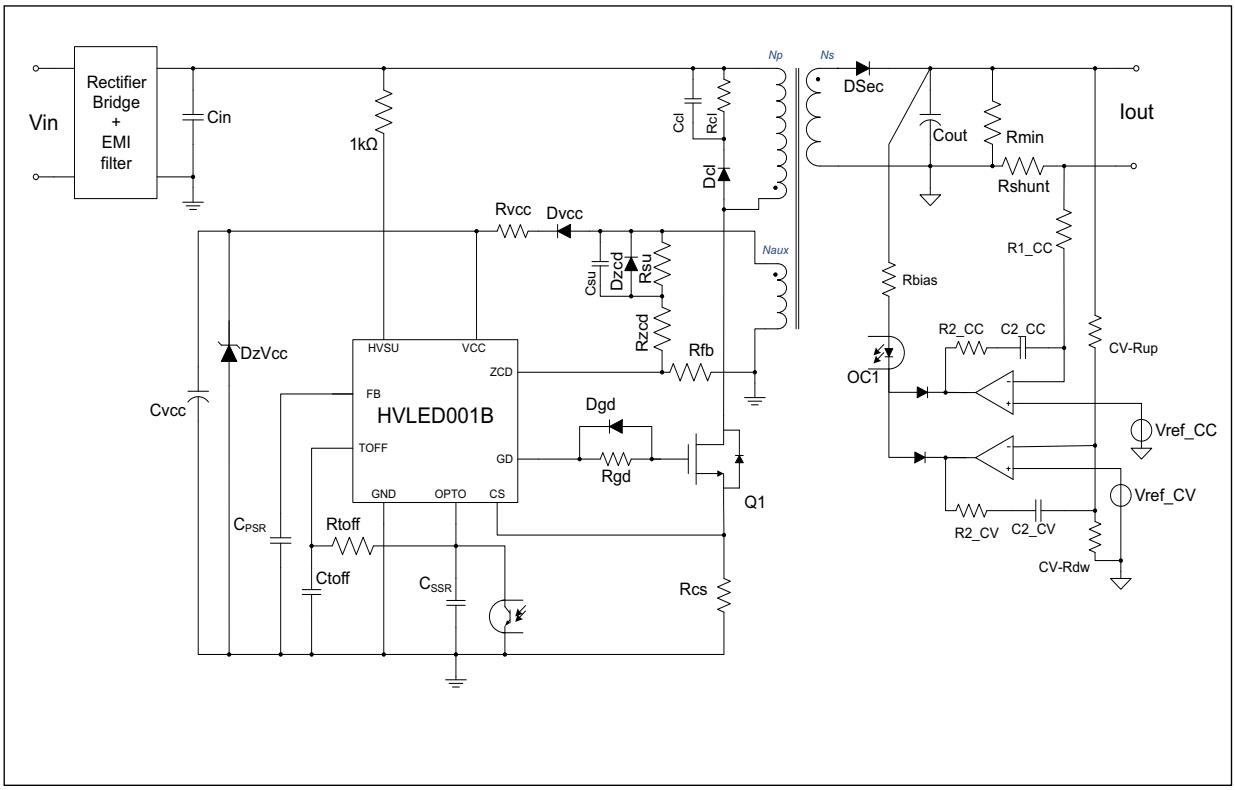


Figure 3. Secondary side regulated (SSR) application



3 Pin settings

Figure 4. Pin connection

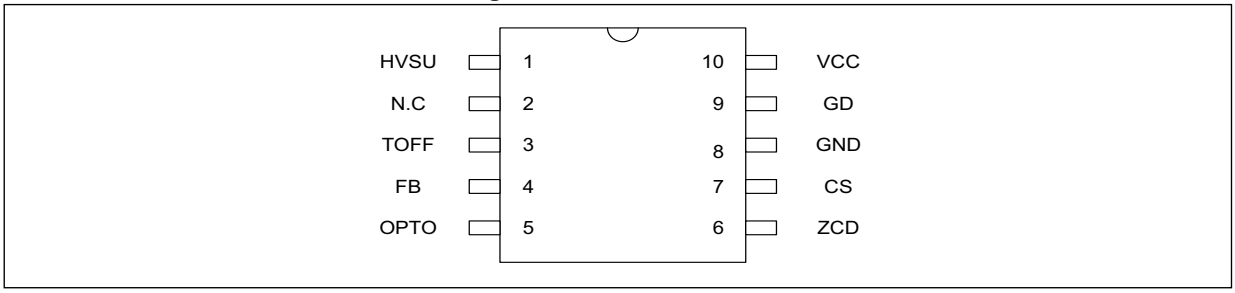


Table 2. Pin description

Symbol	Pin	Description
HVSU	1	High voltage startup and input voltage detection. The pin, able to withstand 800 V, is to be tied to the input voltage using a low value resistor (1 kΩ typ.). It embeds the internal start-up unit that charges the capacitor connected between the VCC pin and GND pin during startup and low consumption. During operational mode, the voltage at this pin is used to both measure the input voltage and detect input over-voltages.
N.C.	2	Not connected pin.
TOFF	3	A blanking time, starting from first valley detection, can be set applying a voltage to this pin. This variable blanking time is used to skip resonant valleys and, then, to fold back the operating frequency. A null blanking time is obtained leaving the pin unconnected.
FB	4	Output of the error amplifier of primary side regulation loop regulation. The pin is intended to be connected to the compensation network for primary side regulation. An upper threshold VOFP detects an overload. Burst mode is also related to the voltage applied to this pin.
OPTO	5	Input for optocoupler in secondary side control loop. This pin is intended to be connected to the collector of the optocoupler. The OPTO pin voltage is internally applied to an OR structure together with FB voltage to feed the internal multiplier. Low consumption mode is invoked pulling this pin lower than the VOPTO,dis threshold that features as burst mode level when OPTO is in use.
ZCD	6	Multiple function pin able to detect the Zero Current instant, to sense the output voltage for the primary side regulation and the input voltage for brownout detection. A negative-going edge triggers the MOSFET's turn-on, while an internal starter unit is active to generate the triggering signal when not externally available (e.g. startup).
CS	7	Input to the current sense comparator for the power regulation. A second level overcurrent (OCP) threshold detects abnormal currents (e.g.: due to transformer's saturation) and, on this occurrence, activates the second level overcurrent protection procedure.
GND	8	Reference pin.

Table 2. Pin description (continued)

Symbol	Pin	Description
GD	9	Gate driver output. The output stage is able to drive the power MOSFET's and IGBT's gate.
VCC	10	Supply voltage of the IC. Internal UVLO logic prevents the operation at voltages that are insufficient for the efficient gate driving or signal processing. Both a bulk capacitor (typically around 22 µF) and a high frequency filter capacitor (100 nF ceramic, mounted as close as possible to the device) are connected between this pin and GND. An internal clamp structure prevents accidental low energy spikes damaging the device.

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
VHVSU,bd	HVSU	HVSU breakdown voltage	IHVSU < 100 µA, DC V_{CC} = 15 V	800	-	V
VHVSU,neg	HVSU	HVSU negative voltage	IHVSU source < 2 mA	- 0.3	-	V
VGD	GD	Maximum swing voltage		- 0.3	V_{CC}	V
VCS	CS	Current sense applied voltage		- 0.3	7	V
VZCD	ZCD	ZCD pin voltage		-	7	V
			Negative, Isource < 1 mA	- 0.3	-	V
VFB	FB	FB voltage		- 0.3	3.6	V
VOPTO	OPTO	OPTO voltage	Stop mode	- 0.3	3.6	V
VCC, MAX.	VCC	IC supply voltage		-	18	V
VTOFF	TOFF	Maximum applied voltage		- 0.3	7	V

Note: Where not otherwise indicated the AMR are intended to be applied when $V_{CC} > V_{CC,on}$. When $V_{CC} < V_{CC,on}$ the minimum between the indicated value and V_{CC} + 0.3 V has to be considered.

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	120	°C/W
T_J	Junction temperature operating range	-40 to 125	°C
T_{stg}	Storage temperature range	-55 to 150	°C

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Max.	Unit	Remarks
VCC	V_{CC} supply voltage	$VCC_{,su}$	18	V	
VHV,op	HVSU operative voltage	0	480	V	Linearity not guaranteed between 480 V and Vsurge
VFB	FB pin regulation voltage range	1.085	2.8	V	
VOPTO	OPTO pin regulation voltage range	1.085	2.8	V	
VCS,op	CS pin operative voltage	0	VCS,lim	V	
VZCD	ZCD pin operative voltage	Self limited	3.3	V	Isource < 1 mA
IZCD_sink	ZCD pin operative current	IBO	650	µA	
VTOFF	TOFF pin operative voltage	0	3.3	V	

5 Electrical characteristics

(T_j = -40 °C to 125 °C, 25 °C production tested, VCC = 15 V, unless otherwise specified.)

Table 6. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
Vcc,on	VCC	Turn-on threshold	(1)	11.9	13.2	14.6	V
Vcc,su	VCC	Low consumption mode activation	Low consumption mode(1)	7.3	7.9	8.5	V
			Startup	1.3	1.5	1.7	V
Vcc,shd	VCC	V_{CC} for IC reset	Low consumption(1)	6.3	6.84	7.4	V
Supply current							
Istartup	VCC	Start-up current	Startup, Vcc < Vcc,on	-	125	160	µA
ICC	VCC	Operating supply current	No switching(2)	-	2	3	mA
			See relevant graph	-			
Iq	VCC	Quiescent current	Low consumption mode, OPTO = 0 V	-	480	600	µA
High voltage start-up generator							
VHV	HVSU	Breakdown voltage	IHV < 100 µA	800	-	-	V
VHVstart	HVSU	Start voltage	IVcc < 100 µA	40	46	55	V
Icharge,su	VCC	Initial charging current	VHVSU > VHvstart, Vcc < 1 V	0.3	0.56	0.7	mA
Icharge	VCC	V_{CC} charge current	VHVSU > VHvstart, Startup, V_{CC} < Vcc,on	2	3.4	4	mA
IHV, ON	HVSU	ON-state current	VHVSU > VHvstart, Vcc < 1 V	0.3	0.65	1.1	mA
			VHVSU > VHvstart, Startup, Vcc < Vcc,on	2.3	4	5	
IHV, OFF	HVSU	OFF-state leakage current	VHVSU = 400 V, Active mode	-	18	30	µA
Input voltage sensing							
Vsurge	HVSU	Surge protection threshold		500	570	620	V
Feedback input							
VFB,os	FB	FB voltage for minimum VCS	Active mode(3) (4)	0.9	1	1.12	V
kp	FB	Multiplier gain	Active mode, VFBint = 2.0 V, VHVSU = 300 V(4)	0.32	0.4	0.48	-
IFBsrc	FB	FB pin pull-up current	Active mode, VZCD,off = 2.0 V, VFB = 1.65 V	0.7	1	1.3	mA

Table 6. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
IFBsnk	FB	FB pull-down current	Active mode, VZCD,off = 3.2 V, VFB = 1.65 V	1.3	1.9	2.5	mA
VBm	FB	Burst mode (1.5 ms) threshold	Active mode(3)	0.97	1.054	1.11	V
VBm2	FB	Burst mode (4 ms) threshold	Active mode(3)	0.86	0.9	0.94	V
Tbm	FB	Burst mode repetition rate	VFB = 0.95 V	1.1	1.5	1.9	ms
Tbm2	FB	Burst mode repetition rate	VFB = 0.75 V	3.2	4.0	4.8	ms
VOPP	FB, OPTO	Over Power protection threshold	Active mode(3)	2.8	-	-	V
TOPP	FB, OPTO	Max. Active mode duration after FBint clamping	VFBint > VOPP(5)	75	100	125	ms
PSR function							
VREF,PSR	FB	PSR loop reference	Tamb = 25 °C(6)	2.55	2.6	2.65	V
			Over all temperature range(6) (7)	2.5	2.6	2.7	
gm	FB	Transconductance	ΔIFB = ± 10 µA, VFB = 1.65 V(7)	1.5	2.3	3	mS
Current sense input							
VCS,lim	CS	Current sense reference clamp	VHVSU = DC voltage, VFB = VOPTO = 3.3 V(8)	700	750	810	mV
VCS,min	CS	Current sense minimum level		30	55	80	mV
ICS	CS	Current sense pin bias current	VCS = 500 mV(7)	-	2.5	3.5	µA
TLEB	CS	Leading edge blanking		140	340	470	ns
VOCP	CS	Saturation protection threshold	During Ton(7)	1	1.1	1.2	V
TOCP	CS	Max. stop state duration after OCP	tpulse = 1 µs, amplitude 2 V	0.75	1	1.25	ms
ZCD input							
VZCD,arm	ZCD	ZCD arming threshold	After Tblank,min(6)	0.23	0.3	0.38	V
VZCD,trig	ZCD	ZCD triggering threshold	Negative going edge(6)	0.14	0.2	0.26	V
TBLANK,min	ZCD	ZCD min. blanking time	From MOS turn-off	1.3	1.75	2.5	µs
TBLANK,var	ZCD	ZCD programmable blanking time	VTOFF = 0 V(9), from 1st ZCD trig after TBLANK,min	55	80	115	µs

Table 6. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Twait	ZCD	ZCD waiting time after TBLANK elapse		4.6	6.5	9	µs
VZCD,cl_l	ZCD	ZCD negative clamping voltage	IZCD src = 1 mA	-230	-100	-	mV
IZCDb	ZCD	ZCD pin biasing current	VZCD = 0.1 to 2.6 V(7)	-	-	1	µA
IBO	ZCD	Brownout detection level	Sourcing during ON-time	75	100	125	µA
TBO	ZCD	Brownout detection time	IZCD < IBO(5)	75	100	125	ms
Timing							
Trec	-	Recovery time after Opto failure, Analogue disable or Brownout	(5)	1.8	2.5	3.2	s
TSS	-	Internal time to activate the timed protections	After first startup(5)	0.6	0.85	1.1	s
Gate driver							
VGDH	GD	Output high voltage	IGD,source = 5 mA	14.5	-	-	V
VGDL	GD	Output low voltage	IGD,sink = 5 mA	-	-	0.1	V
Isource	GD	Output source peak current	VGD = 7.5 V(7)	0.48	0.66	-	A
Isink	GD	Output sink peak current	VGD = 7.5 V(7)	0.83	1.2	-	A
Tf	GD	Fall time	CGD = 1 nF, from 13.5 V to 1.5 V	-	5	-	ns
Tr	GD	Rise time	CGD = 1 nF, from 1.5 V to 13.5 V	-	30	-	ns
VGD,shd	GD	Maximum voltage during shut-down	V_{CC} < Vcc,shd , IGD = 2 mA	-	1	1.5	V
OPTO input							
VOPTO,dis	OPTO	Disabling threshold		0.97	1.054	1.11	V
VOPTO,bias	OPTO	OPTO biasing voltage	Tamb = 25 °C(3)	-	3.2	-	V
			Over whole temp. range(7) (3)	2.9	-	-	
IOPTO,bias	OPTO	OPTO biasing current	VOPTO = 0 V	110	148	185	µA
ROPTO	OPTO	Internal parallel resistor		35	45	55	kΩ
TOFF characteristics							
VTOFF,fix	TOFF	Minimum fixed TBLANK voltage	(7)	-	2	-	V
koff	TOFF	TOFF characteristic slope	(7) (9)	-	40	-	µs/V

Table 6. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
ITOFFpu	TOFF	Pull-up current	VTOFF = 0 V Tamb = 25 °C	10	-	13	µA
			VTOFF = 0 V(7)	6.5	12	16.5	µA
VTOFF,bias	TOFF	Internal bias voltage	(7),	-	2.5	-	V

1. Parameters in tracking group 1
2. Calculated during testing procedure as difference between measured Icc and FB source current
3. Parameters in tracking group 2
4. Kp parameter includes the overall tolerances of the multiplier block defined as per note (8)
5. Parameter calculated
6. Parameters in tracking group 3
7. Parameters not tested in production
8. See *Section 7.2.1 Equation 1*
9. $TBLANK.var = koff \cdot (VTOFF, fix - VTOFF)$

6 Typical electrical characteristic

6.1 Parameter graphs

Figure 5. ICC vs. Fsw @ VCC = 15V

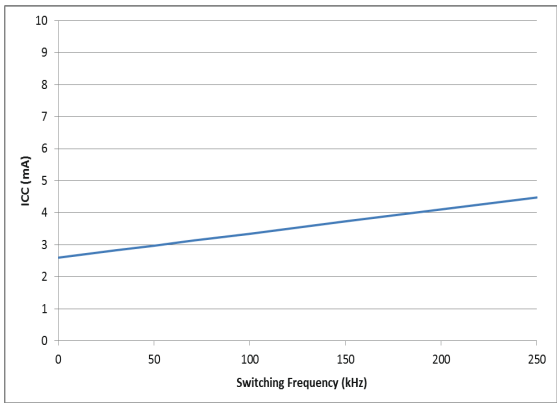


Figure 6. VCC,on and VCC,su vs. Tj

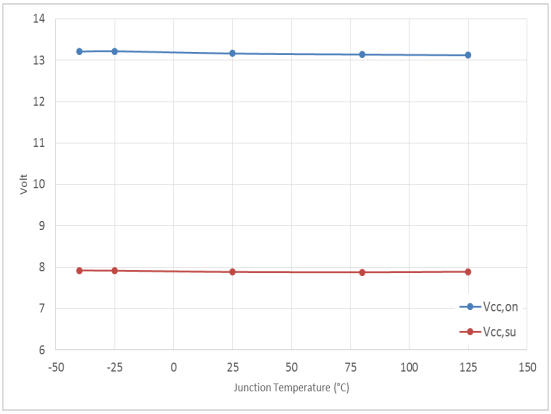


Figure 7. Icharge and Icharge,su vs. Tj

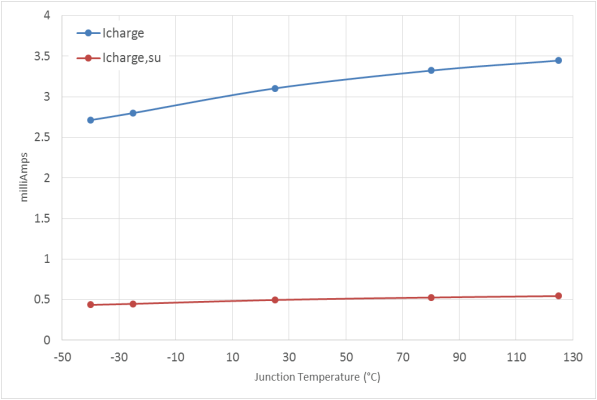


Figure 8. IFB,src and IFB,snk vs. Tj

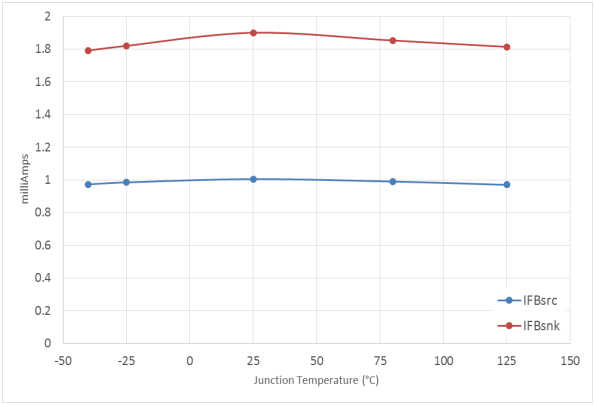


Figure 9. Vbm, Vbm2 and VOPTO,dis vs. Tj

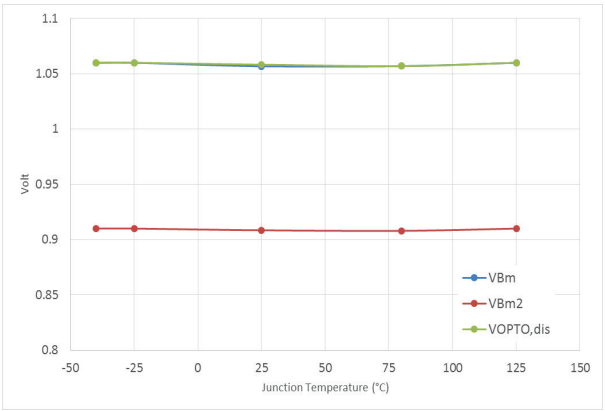


Figure 10. Tbm and Tbm2 vs. Tj

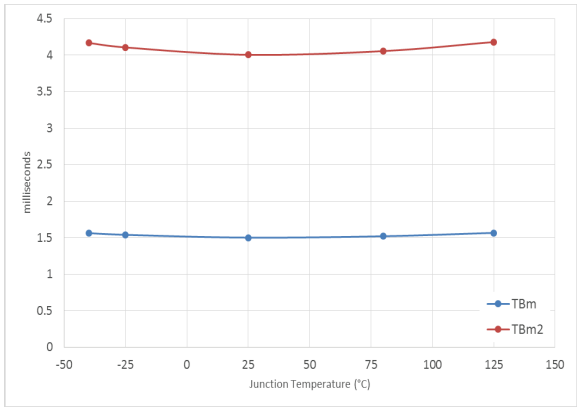


Figure 11. VZCD,arm and VZCD,trig vs. Tj

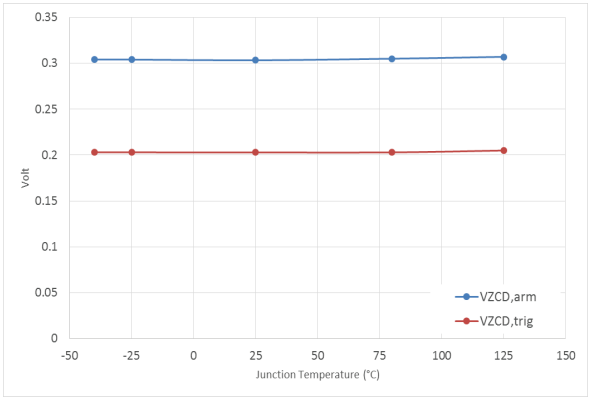


Figure 12. VCS,lim vs. Tj

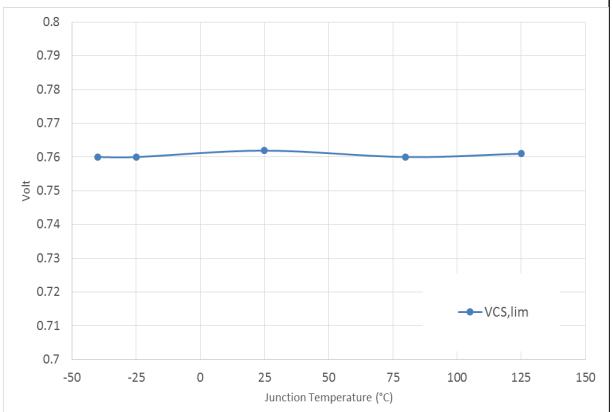


Figure 13. VREF,PSR vs. Tj

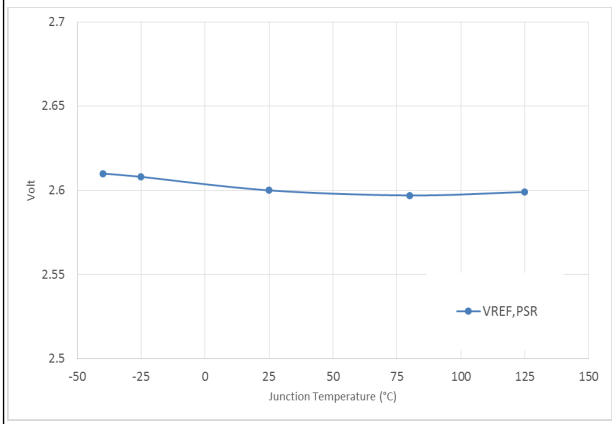


Figure 14. IFB vs. VZCD sample

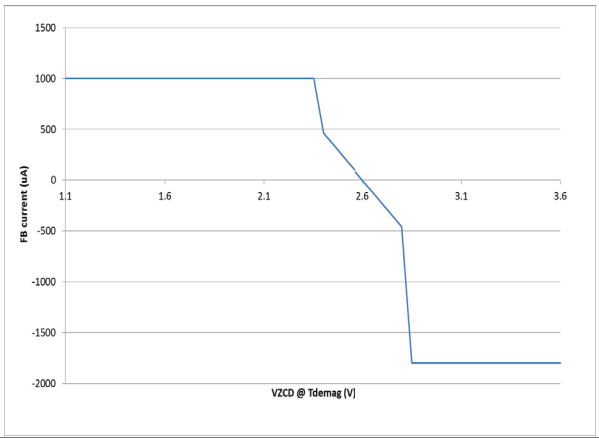


Figure 15. TBLANK,min vs. Tj

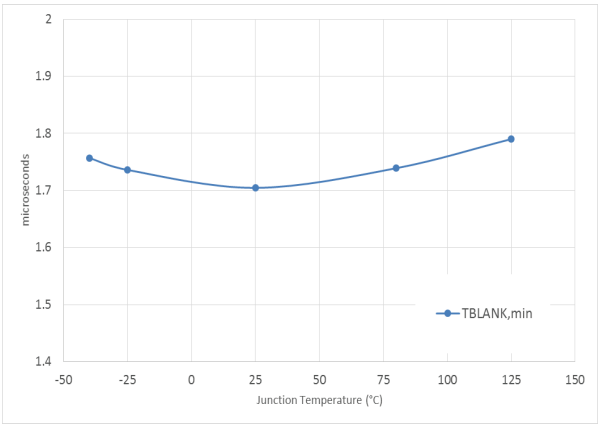
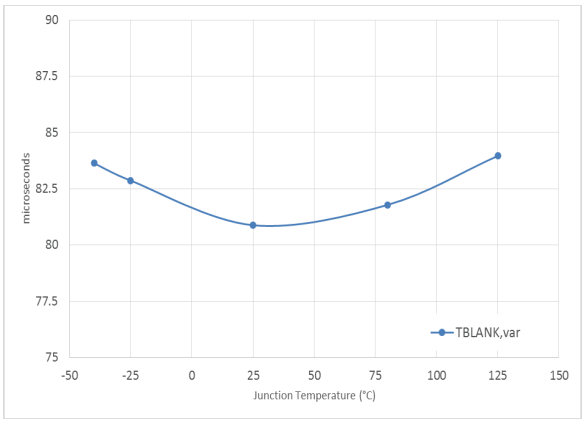


Figure 16. TBLANK,var vs. Tj



7 Application information

7.1 Operating modes

The HVLED001B QR flyback controller is able to operate either as a single-stage high power factor (HPF) flyback controller or as a DC/DC flyback controller in dual-stage topologies. It's enhanced features are mainly intended to simplify the design and the management of constant current applications (LED drivers).

Application schematics of the two main topologies are reported in *Figure 17* and *Figure 18*.

Figure 17. High power factor flyback - Primary side regulated constant output voltage

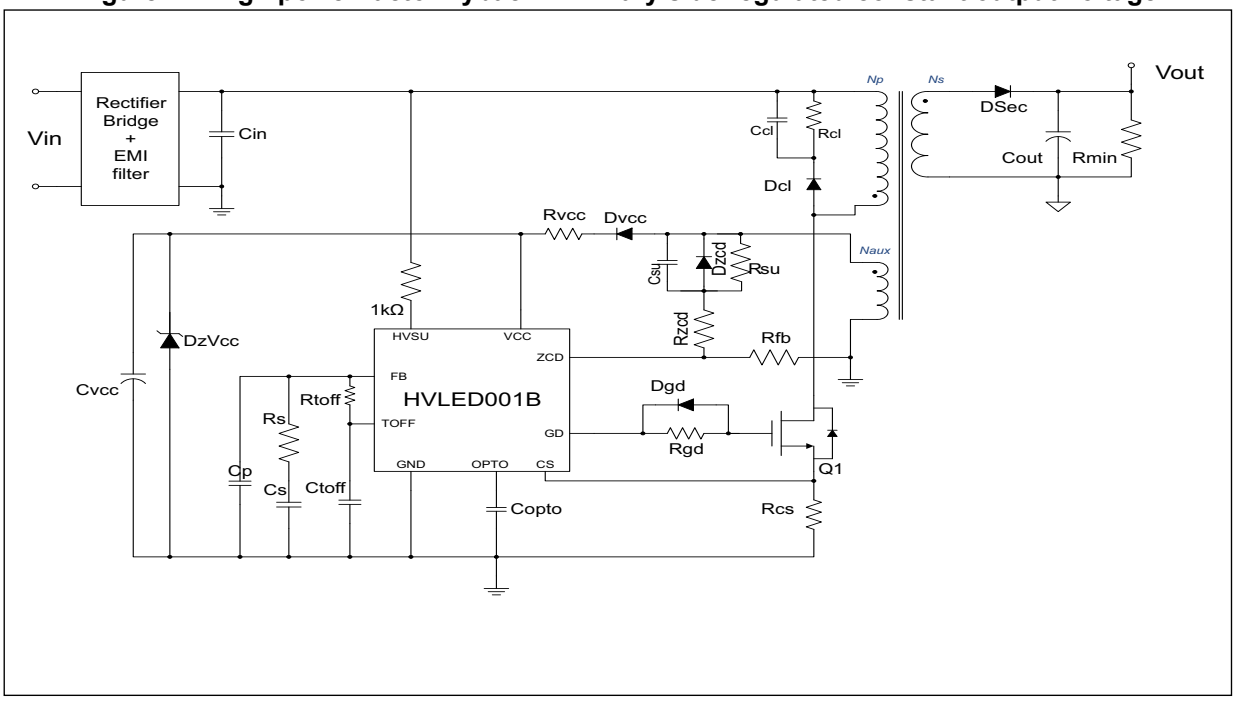
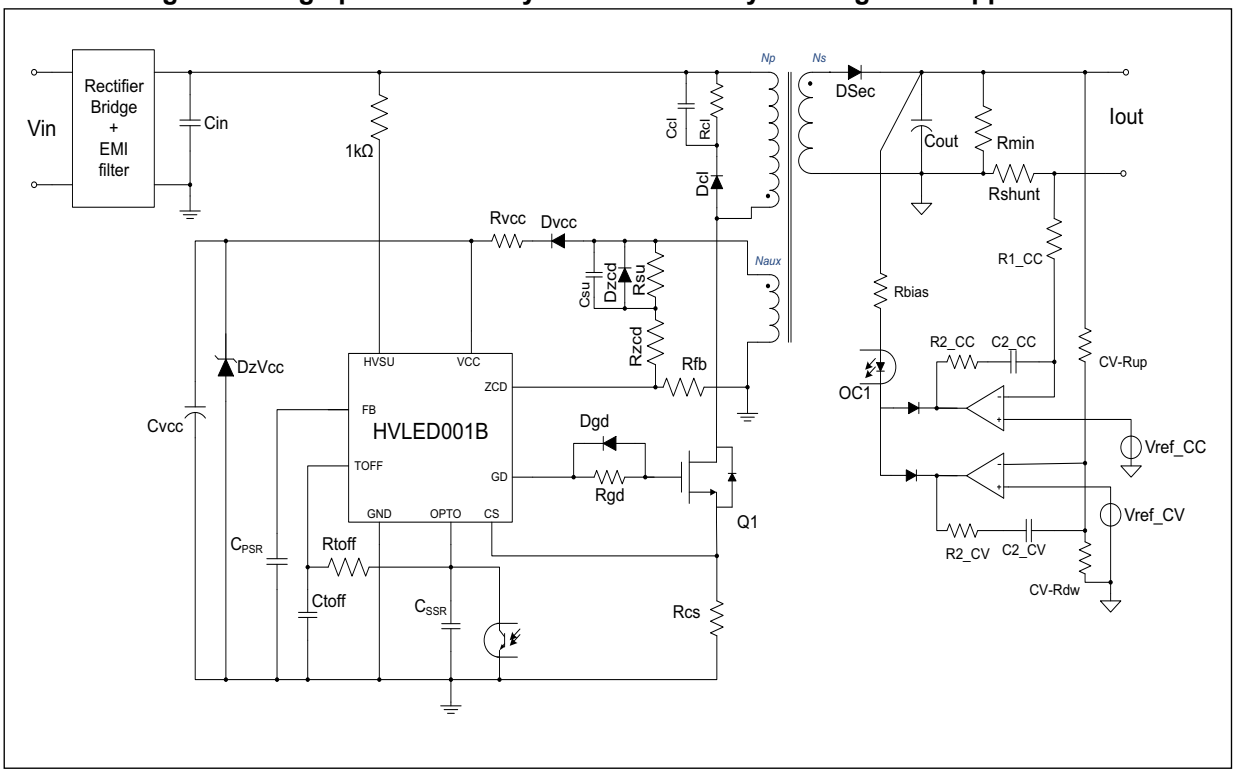


Figure 18. High power factor flyback – secondary side regulated application



The HVLED001B has five main operating modes: Start-up mode, Ramp-up mode, Active mode, Stop mode and Low consumption mode.

7.1.1 Start-up mode

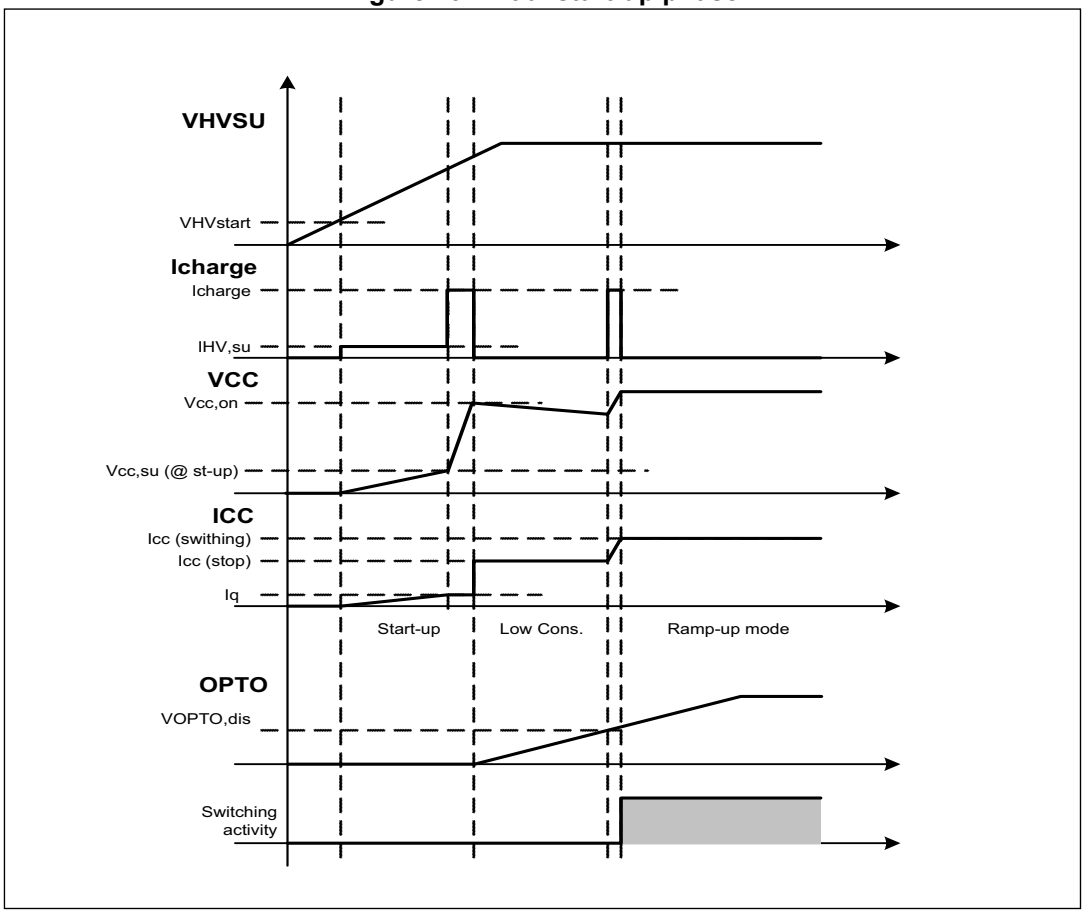
This state is entered to begin the switching activity (during application's turn-on or exiting from the low consumption state). The HVSU is involved in the mechanism of VCC charging; all other peripherals, except the UVLO and logic supply, are turned off to minimize the start-up time.

Start-up mode ends when the OPTO and FB pins are within respective range of operations and VCC is higher than VCC,on threshold.

When the device is turned on for the first time or, in other words, when VCC crosses upwards of the VCC,shd threshold, start-up mode invokes ramp-up mode.

When start-up mode is entered after a low consumption mode, start-up mode invokes active mode.

Figure 19. Initial start-up phase



7.1.2 Ramp-up mode

This is a particular operational mode, identical to active mode, where timed protections (Brownout and Over Power Protection - see relevant graphs) are ignored. This mode ends after a fixed period (Tss) since the first crossing upwards of VCC voltage. After Tss, the IC enters active mode.

7.1.3 Active mode

This is the normal operational mode. During this state the external MOSFET is driven according to signals coming from the application in order to regulate the desired output parameter in closed loop (peak current control method).

Active mode is exited when abnormal conditions are present or VCC drops below the VCC,su threshold. The HVSU is inactive during active mode.

7.1.4 Low consumption mode

This state is intended to stop the switching activity reducing the power consumption to a minimum level.

During this state the VCC is kept between VCC,su and VCC,on by the high voltage startup unit (HVSU) delivering Icharge to the output capacitor.

7.1.5 Stop mode

This state is intended to stop the switching activity without turning off the entire function set, to quickly restart when abnormal or disabling conditions end. During this state the power consumption is not minimized and the HVSU is not enabled. In case the OPTO pin drops below the disabling threshold or VCC voltage drops below the VCC,su voltage and the IC state evolves into low consumption state.

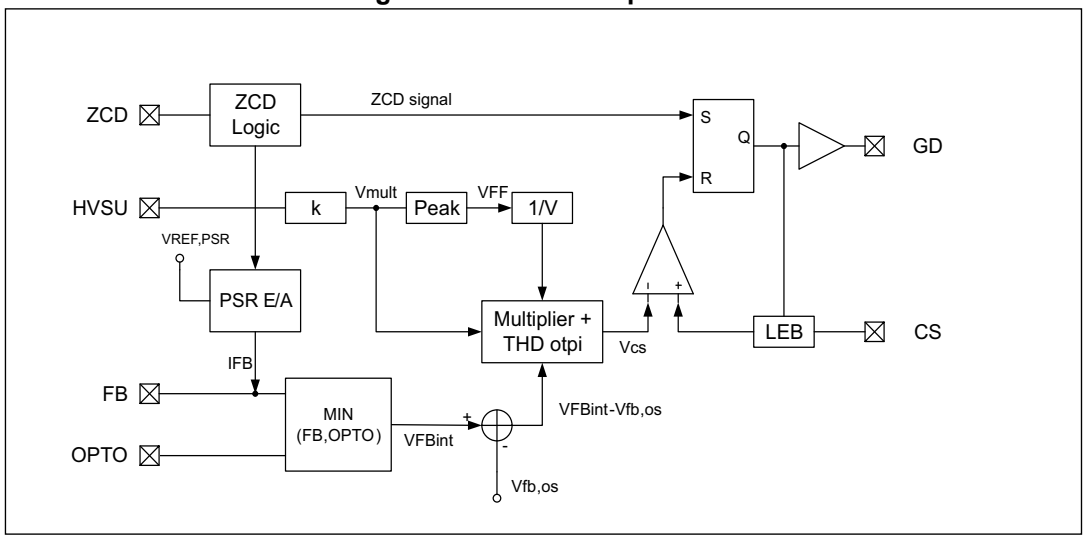
Note: ***IMPORTANT: HVSU charges VCC so any other external voltage (including auxiliary winding) must be de-coupled using a Diode (e.g. 1N4148).***

7.2 Control loop

The control loop is based on the current mode Quasi Resonant flyback control scheme and is therefore performed turning off the MOSFET when the peak of its source current reaches the threshold set by the control loop, and turning the MOSFET on in correspondence with the resonant valley following the primary side demagnetization input.

A detail of the block involved in this scheme is shown in *Figure 20*.

Figure 20. Control loop blocks



7.2.1 Current sense input

The peak of the primary current is read across a shunt resistor placed between the MOSFET‘s source and compared with a threshold equal to:

Equation 1

$$V_{CS} = k_p \cdot \frac{V_{HVSU}}{V_{HVSU,pk}} \cdot \left(V_{FB\,\mathrm{int}} - V_{FB,os}\right)$$

Where the term $V_{HVSU,pk}$ is the maximum value of the HVSU voltage within around 20 ms and is used to compensate the dependency on the input voltage of the open loop gain transfer function. The gain k_p collects all the proportional terms between HVSU voltage and CS threshold.

A leading edge blanking time (LEB) is applied after MOSFET‘s turn-on.

VCS signal is upper limited to a value that depends on the OPTO voltage and is lower limited to 60 mV.

A second level OCP threshold is present to temporarily stop the switching activity in case of inductor saturation.

7.2.2 Feedback input

The OPTO pin is intended to be connected directly to the collector of the optocoupler that provides the galvanic insulation to the control loop, while the FB pin is the output of the error amplifier for the Primary side control loop of the output voltage (PSR) (see *Section 7.2.4*). A suitable pick-up capacitor can be connected to the OPTO pin while suitable compensation network for PSR is placed between FB and ground.

The FB voltage is also used as input parameter for burst mode operation described in the relevant paragraph.

These pins embed a protection to stop the switching activity in case of excessive power delivery (OPP protection).

7.2.3 Zero current detection

The zero level detection is performed by a trigger logic that operates as follows:

a) The logic is armed if ZCD voltage is higher than VZCD,arm after Tblank,min starting from GD turn-off instant.

b) The logic is triggered to turn on the MOSFET when a falling edge crosses ZCD,trig threshold. A small additional delay between ZCD triggering and GD turn-on is there to turn on the MOSFET in correspondence if the bottom of resonance valley.

The advanced ZCD logic is able to discriminate between normal operation, output short-circuit or start-up condition.

An internal blanking time prevents any triggering signal to activate the MOSFET at the very beginning of the OFF-time, where spurious resonances could be present. As a result, the first falling edge occurring after the blanking time turns on the MOSFET.

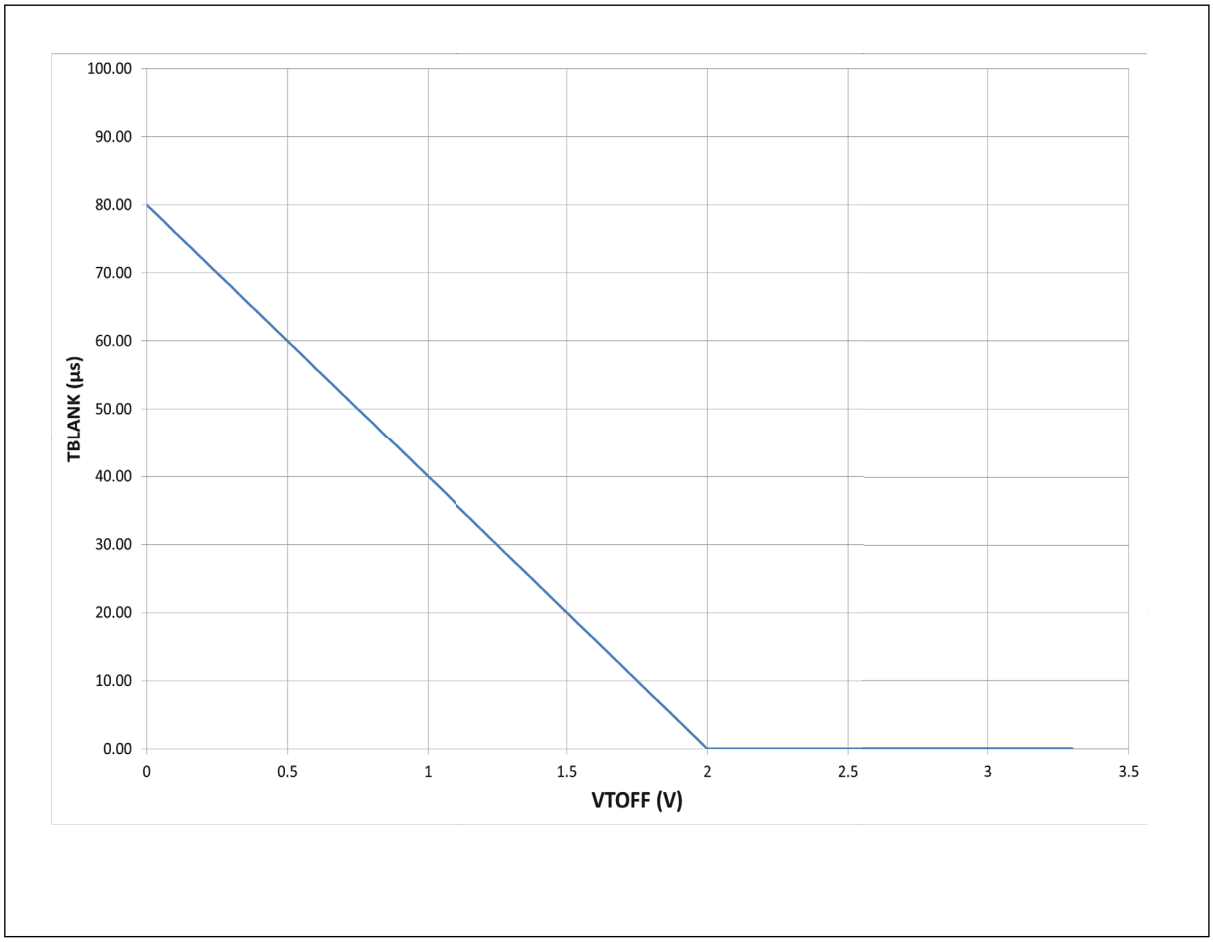
To ensure a proper operation, the transformer has to be designed to guarantee that the inductor's demagnetization time is longer than TBLANK (@ VTOFF > VTOFF,fix) when the V_{CS} value (*Equation 1*) is higher than 0.7 V (typ.).

The TOFF pin is intended to apply an additional blanking time following the first ZCD triggering event. If the pin is left unconnected, null blanking time is provided. The TBLANK,var value depends on TOFF voltage as illustrated in *Figure 21*.

An internal starter provides the triggering signal whenever a valid arming signal is not detected.

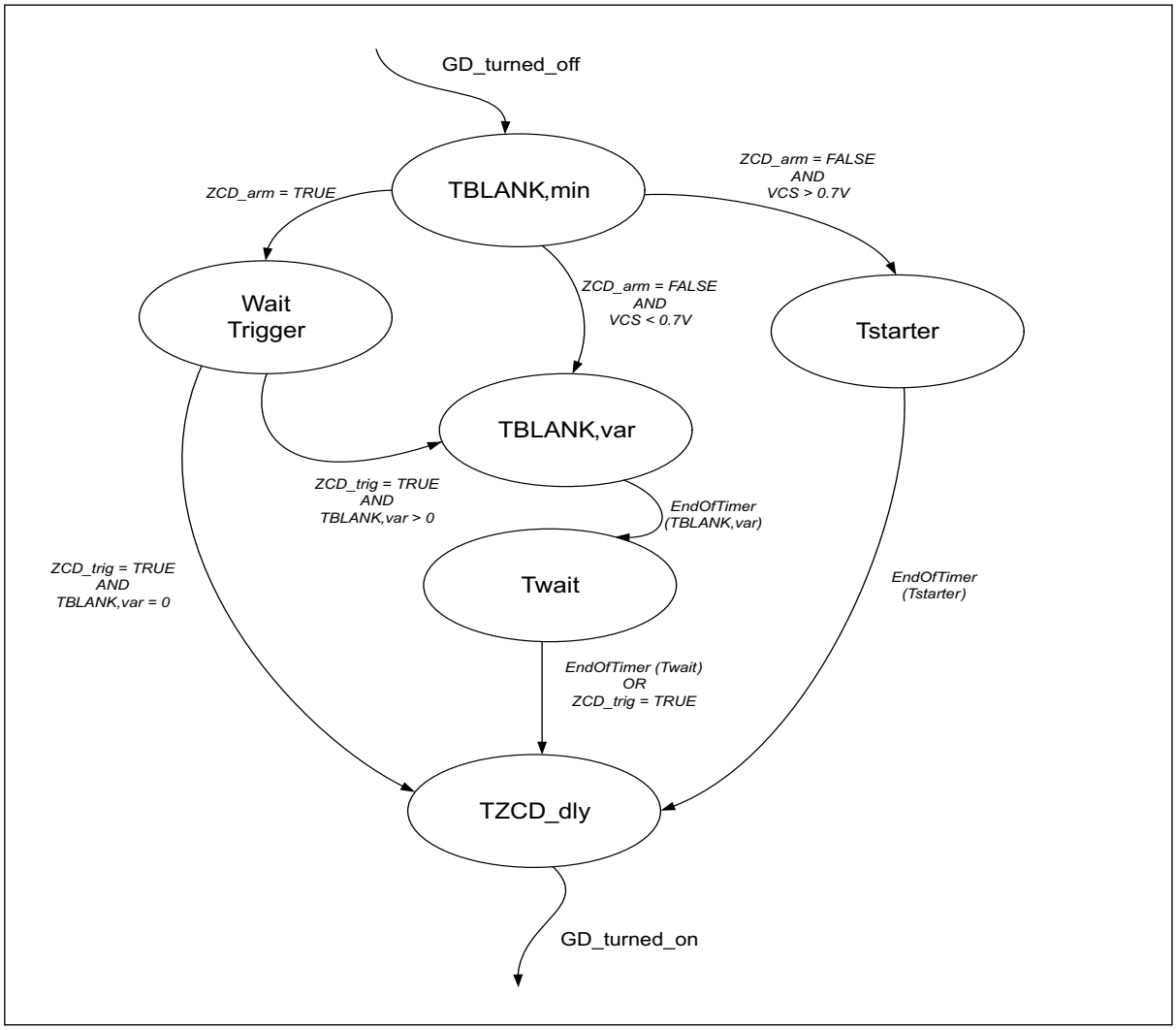
The ZCD pin embeds a negative clamp to limit the negative going current.

Figure 21. TBLANK,var time vs. TOFF voltage



The blanking time management algorithm is reported in *Figure 22*.

Figure 22. TBLANK,var time vs. TOFF voltage



7.2.4 Primary side regulation feature

The ZCD pin is also used as input of the PSR error amplifier (E/A). The reference voltage of this loop is internally fixed to VREF,PSR and applied to the non-inverting input of the E/A. The output of such error amplifier is connected to the FB pin where the relevant compensation network has to be connected.

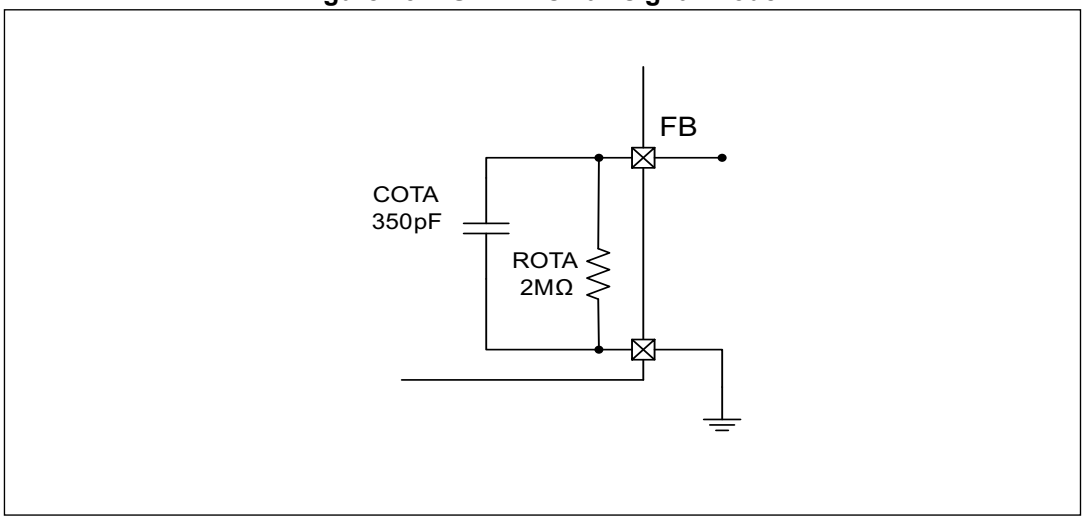
In a flyback or buck-boost topology the output voltage can be read from primary side using an auxiliary winding of the power magnetic: in this case the output voltage is obtained using the following equation:

Equation 2

$$V_{out} = VREF,PSR \cdot \frac{N_{SEC}}{N_{AUX}} \cdot \left(1 + \frac{Rzcd}{Rfb}\right)$$

The internal small signal model of the PSR E/A is obtained by considering the voltage gain (G_V = 73 dB) and the Gain Bandwidth product (GBWP = 1 MHz) and is illustrated in *Figure 23*:

Figure 23. PSR E/A small signal model



7.2.5 Burst mode operation

As soon as either the FB pin or OPTO pin drops below, respectively, Vbm or VOPTO,dis the burst mode operating mode is entered. On this occurrence, the switching activity is temporarily interrupted. If the PSR loop is controlling the application, the output voltage value is refreshed every Trep by means of the generation of four switching pulses.

On the other hand, if the optocoupler is controlling the loop, the IC remains disabled until the OPTO pin is above VOPTO,dis and the FB pin is above Vbm.

During IC inactivity, VCC consumption is minimized.

7.3 Gate driver

The output stage, connected to VCC potential and capable of 300 mA source and 600 mA sink current, is suitable to drive high current MOSFETs. The resulting managed power can be greater than 150 W.

7.4 IC supply management

The IC's voltage supply is managed by the UVLO circuitry together with high voltage startup unit and reference generators. These logics also define supply currents during different operating conditions.

7.4.1 VCC supply management

The IC is designed to operate with a range of supply voltage to ensure an optimum gate driving. An active limiting device is embedded to prevent low energy fluctuations to bring the VCC voltage above the technological constraints.

Both the active mode and the low consumption mode exhibit very low supply currents in order to meet energy saving regulation.

The VCC pin can be driven independently from the HVSU pin's connection, for example when auxiliary supply voltage is present. In this case the HVSU pin will be used solely to monitor input voltage.

A bulk capacitor, having a capacitance of around 22 µF, followed by a ceramic capacitor, having a typical capacitance of 100 nF and connected very tight to the VCC pin, are necessary to properly sustain the VCC voltage during all operating phases.

7.4.2 High voltage startup

High voltage startup (HVSU) circuitry is primarily intended to provide the start-up current to the VCC pin and maintain the IC responsive during low consumption modes.

This structure is able to sustain at least 800 V to avoid any damage in case of a surge or burst on the stage's input.

The overall structure is OFF until input voltage reaches VHVSU,start threshold; after that it sources a minimum current (Icharge,su) to charge the VCC pin up to Vcc,su threshold. This condition prevents the IC from severe damage in the case of short-circuit on the VCC pin.

At this VCC voltage a higher current (Icharge) is provided to VCC to reach the VCC,on threshold. On this occurrence the ramp-up mode is invoked and the HVSU is turned off.

During other active mode phases and stop mode the HVSU is OFF.

If low consumption mode is entered, the HVSU unit is turned on.

Table 7 summarizes the HVSU behavior in all IC conditions.

Table 7. HVSU operating modes

Operating condition	VCC range	OFF	Icharge,su	Icharge
All states if VIN < VHVSU,ON		X	-	-
Startup (logic startup)	0 V … Vcc,su	-	X	-
Startup (IC startup)	Vcc,su … Vcc,on	-	-	X
Active mode and Ramp-up mode	Vcc,su … VCC,MAX	X	-	-
Stop mode	Vcc,su … VCC,MAX	X	-	-
Low consumption mode	Vcc,su → Vcc,on (rising)	-	-	X
Low consumption mode (after the end of entering conditions)	Vcc,su … Vcc,on	-	-	X

7.5 Auto restart timer (ART)

The Auto Restart Timer unit is responsible for the generation of the protection's intervals and of the restart times after low consumption mode. A summary of all possible combinations of times is described in each protection section.

7.6 Protections

A comprehensive set of protections is embedded to ensure a high level of reliability of the final application using a limited number of components.

7.6.1 Over current protection (OCP)

To prevent any damage to active components in case of inductor saturation the MOSFET is immediately turned off by fast OCP protection. On this occurrence the IC temporarily enters stop state for a time equal to TOCP.

7.6.2 Input over voltage protection (I-OVP)

Disturbances of the input voltage like surges or bursts may increase the voltage applied to the transformer primary side. At worst, an excessive input voltage could be applied to the application. These occurrences may result in MOSFET damage during the OFF state when the drain voltage rises to Vin plus reflected voltage, eventually above the maximum absolute rating of the MOSFET itself.

An input voltage higher than VSurge, measured by the HVSU structure, immediately stops the IC. An internal hysteresis improves the noise rejection of this feature. This protection is always active.

7.6.3 Brownout protection (BO)

The current sourced by the ZCD pin's negative clamp during ON-time is compared to a minimum value to determine whether the input voltage is lower than the input range specification (Brownout protection). If a value lower than IBO for a time longer than TBO, managed by the ART, is detected, the IC is stopped for Trec and then restarted.

When the protection is triggered, the ART performs the auto-relaoding procedure after Trec. Brownout protection is active during active mode, but blanked during ramp-up mode.

Referring to the typical application schematic, the brownout level can be obtained adjusting the transformer turn ratio and ZCD resistor configuration. The following equation regulates the relationship between said level and external components.

Equation 3

$$Vbrown,out = \frac{N_{PRI}}{N_{AUX}} \cdot (R_{FB} + R_{BO}) \cdot I_{BO}$$

7.6.4 Over power protection (OPP)

This protection detects either the over-load condition or the absence of the optocoupler control (no pull-down) or for more than a time equal to TOPP and switches off the application putting the device in low consumption mode. This prevents the output power from rising above excessive values due to the loss of control.

The ART manages the TOPP interval and performs the auto-reloading procedure after Trec. The OPP is active during active mode, but blanked during ramp-up mode.

7.6.5 Output over voltage protection (oOVP)

In the case of ZCD sampled voltage being well above the VREF,PSR voltage (around 3 V), OTA provides an extra sink current (2 mA typ.) to the FB pin to speed up the energy transfer reduction and limiting the output voltage overshooting.

7.7 Disable and monitor feature

The OPTO pin can also be used as disabling mean to externally disable the IC: when pulled to ground the device enters low consumption mode, while, when the OPTO pin is left free, the internal biasing mean pulls up the voltage above the threshold entering the ramp-up mode procedure.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 SSOP10 package outline

Figure 24. SSOP10 package mechanical data

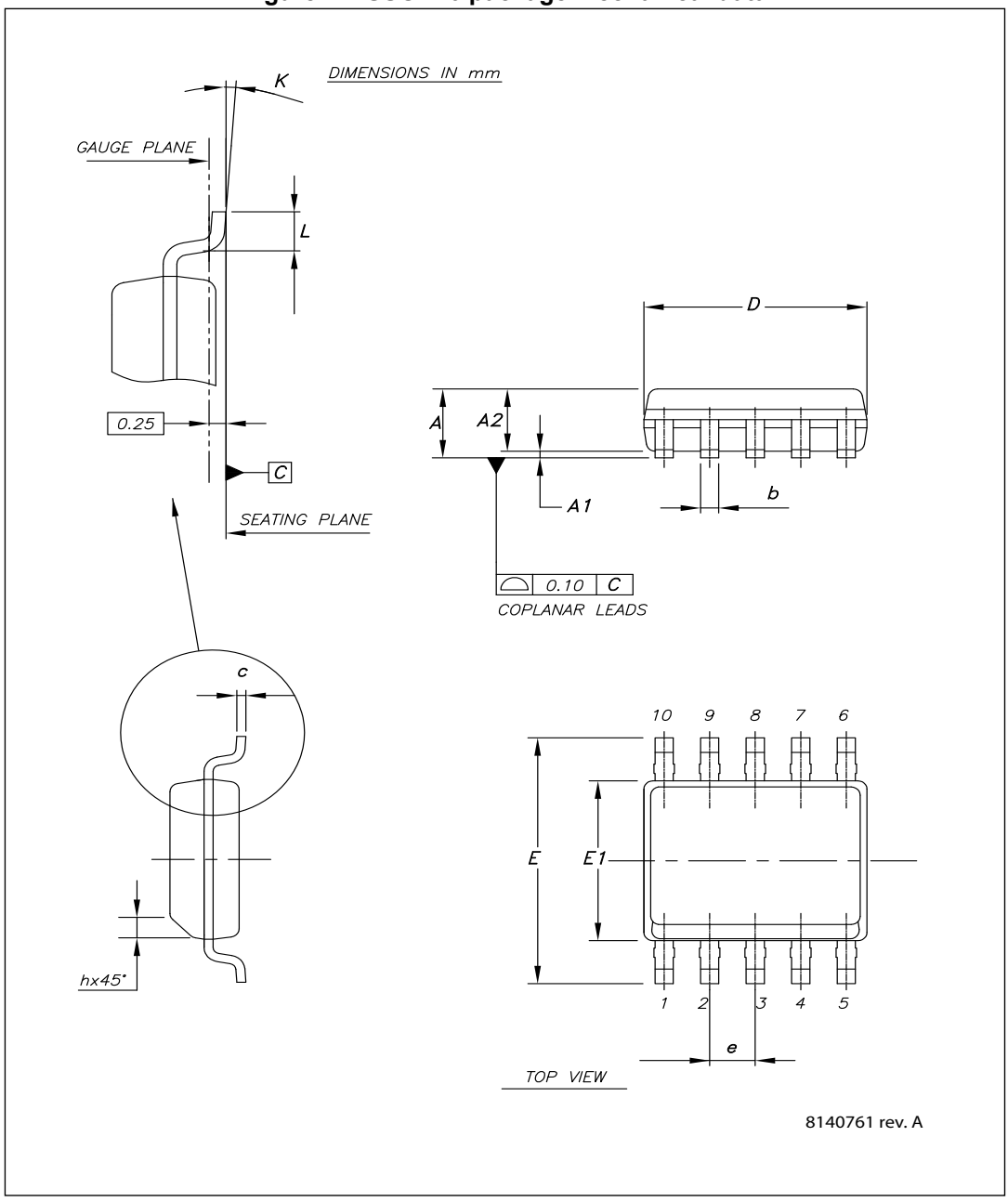


Table 8. SSOP10 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e	-	1	-
h	0.25	-	0.50
L	0.40	-	0.90
K	0°	-	8°

9 Revision history

Table 9. Document history

Date	Revision	Changes
3-Sept-2018	1	Initial version.
15-Jan-2019	2	Updated *Table 6*.

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