

# Dual N- and P-Channel Enhancement Mode Field Effect Transistor

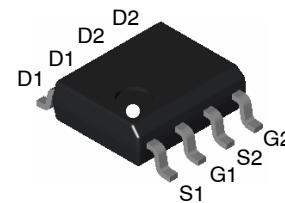
## SI4532DY

### General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

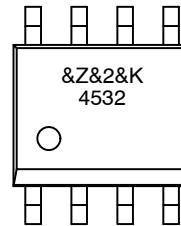
### Features

- N-Channel 3.9 A, 30 V
  - ◆  $R_{DS(ON)} = 0.065 \Omega$  @  $V_{GS} = 10 \text{ V}$
  - ◆  $R_{DS(ON)} = 0.095 \Omega$  @  $V_{GS} = 4.5 \text{ V}$
- P-Channel -3.5 A, -30 V
  - ◆  $R_{DS(ON)} = 0.085 \Omega$  @  $V_{GS} = -10 \text{ V}$
  - ◆  $R_{DS(ON)} = 0.190 \Omega$  @  $V_{GS} = -4.5 \text{ V}$
- High Density Cell Design for Extremely Low  $R_{DS(ON)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Dual (N & P-Channel) MOSFET in Surface Mount Package
- This Device is Pb-Free and Halide Free



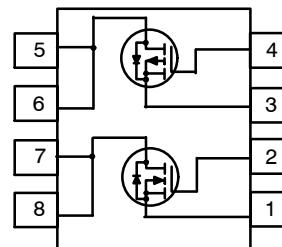
SOIC8  
CASE 751EB

### MARKING DIAGRAM



&Z = Assembly Site  
 &2 = 2-Digit Date Code  
 &K = 2-Digits Lot Run Traceability Code  
 4532 = Specific Device Code

### PIN CONNECTION



### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
SI4532DY	SOIC8 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Unit
$V_{DSS}$	Drain–Source Voltage	30	-30	V
$V_{GSS}$	Gate–Source Voltage	20	-20	V
$I_D$	Drain Current – Continuous (Note 1a)	3.9	-3.5	A
	Drain Current – Pulsed	20	-20	
$P_D$	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	N-Ch	30	-	-	V	
		$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	P-Ch	-30	-	-		
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch	-	-	1	$\mu\text{A}$	
		$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch	-	-	-1		
$I_{GSSF}$	Gate–Body Leakage, Forward		$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	All	-	-	100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse		$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	All	-	-	-100	

## ON CHARACTERISTICS (Note 2)

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1	-	3	V
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-1	-	-3	
$R_{DS(\text{on})}$	Static Drain–Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.9 \text{ A}$	N-Ch	-	0.053	0.065	$\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$		-	0.081	0.095	
		$V_{GS} = -10 \text{ V}, I_D = -2.5 \text{ A}$	P-Ch	-	0.06	0.085	
		$V_{GS} = -4.5 \text{ V}, I_D = -1.8 \text{ A}$		-	0.095	0.19	
$I_{D(\text{on})}$	On–State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	N-Ch	15	-	-	A
		$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	P-Ch	-15	-	-	
$g_{FS}$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 3.9 \text{ A}$	N-Ch	-	7	-	S
		$V_{DS} = -15 \text{ V}, I_D = -2.5 \text{ A}$	P-Ch	-	5	-	

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit			
<b>DYNAMIC CHARACTERISTICS</b>										
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	N-Ch	—	235	—	pF			
			P-Ch	—	420	—				
			N-Ch	—	150	—	pF			
$C_{oss}$	Output Capacitance		P-Ch	—	140	—				
			N-Ch	—	49	—	pF			
	Reverse Transfer Capacitance		P-Ch	—	60	—				
<b>SWITCHING CHARACTERISTICS</b> (Note 2)										
$t_{d(on)}$	Turn-On Delay Time		$V_{DD} = 10\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\Omega$	N-Ch	—	7	13	ns		
				P-Ch	—	9	18			
$t_r$	Turn-On Rise Time			N-Ch	—	18	29	ns		
				P-Ch	—	8	16			
$t_{d(off)}$	Turn-Off Delay Time		$V_{DD} = -10\text{ V}$ , $I_D = -2.5\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\Omega$	N-Ch	—	15	27	ns		
				P-Ch	—	18	29			
$t_f$	Turn-Off Fall Time			N-Ch	—	0.8	8	ns		
				P-Ch	—	6	12			
$t_{rr}$	Drain-Source Reverse Recovery Time		$I_F = 1.7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch	—	—	80	ns		
				P-Ch	—	—	80			
$Q_g$	Total Gate Charge		$V_{DS} = 10\text{ V}$ , $I_D = 3.9\text{ A}$ , $V_{GS} = 10\text{ V}$	N-Ch	—	3.7	15	nC		
				P-Ch	—	5	15			
$Q_{gs}$	Gate-Source Charge			N-Ch	—	0.9	—	nC		
				P-Ch	—	1.7	—			
$Q_{gd}$	Gate-Drain Charge			N-Ch	—	1.9	—	nC		
				P-Ch	—	1.8	—			

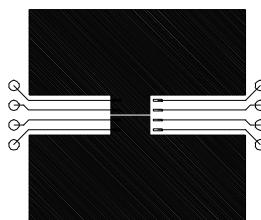
**DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	—	—	1.7	A
				P-Ch	—	—	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 1.7\text{ A}$ (Note 2)	N-Ch	—	0.75	1.2	V
			P-Ch	—	-0.75	-1.2	

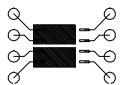
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## NOTES:

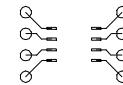
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C}/\text{W}$  when mounted on a  $0.05\text{ in}^2$  pad of 2 oz copper.

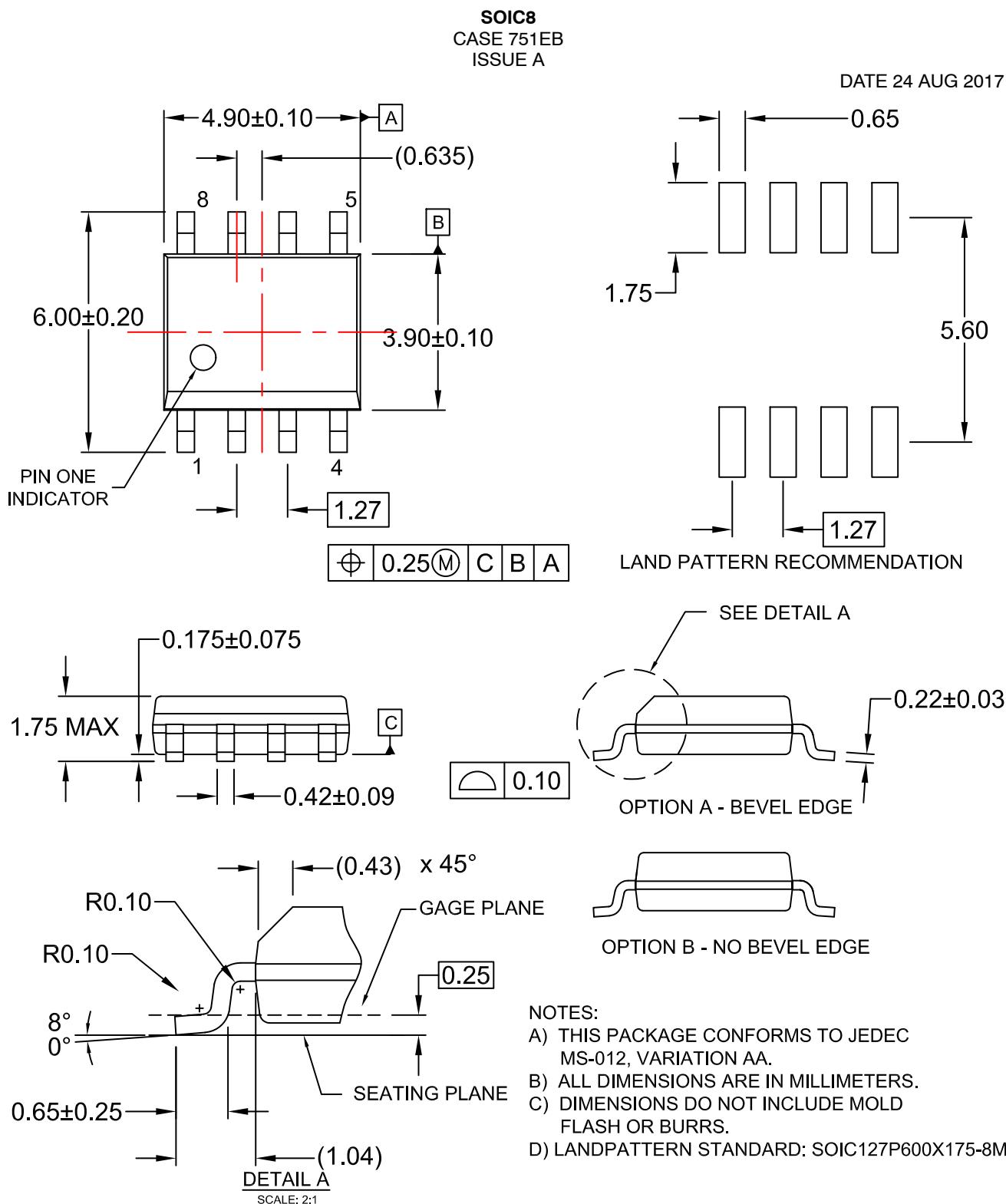


b)  $125^\circ\text{C}/\text{W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz copper.



c)  $135^\circ\text{C}/\text{W}$  when mounted on a minimum mounting pad.

2. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$



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