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MC74VHCT138A

3-to-8 Line Decoder

The MC74VHCT138A is an advanced high speed CMOS 3−to−8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled, three Binary Select inputs (A0 − A2) determine which one of the outputs ($\overline{Y0}$ − $\overline{Y7}$) will go Low. When enable input E3 is held Low or either $\overline{E2}$ or $\overline{E1}$ is held High, decoding function is inhibited and all outputs go high. E3, $\overline{E2}$, and $\overline{E1}$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because they have full 5.0 V CMOS level output swings.

The VHCT138A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.
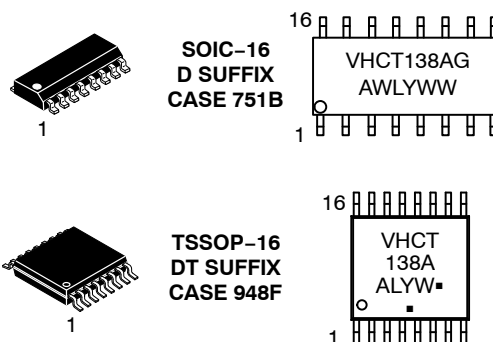
Features

- High Speed: t_{PD} = 7.6 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates
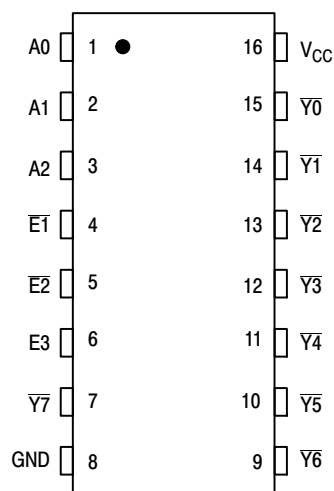- These Devices are Pb−Free and are RoHS Compliant

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MARKING DIAGRAMS

SOIC−16
D SUFFIX
CASE 751B

16
VHCT138AG
AWLYWW
1

TSSOP−16
DT SUFFIX
CASE 948F

16
VHCT
138A
ALYW■
1

A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

A0	1 ●	16	V_{CC}
A1	2	15	$\overline{Y0}$
A2	3	14	$\overline{Y1}$
$\overline{E1}$	4	13	$\overline{Y2}$
$\overline{E2}$	5	12	$\overline{Y3}$
E3	6	11	$\overline{Y4}$
$\overline{Y7}$	7	10	$\overline{Y5}$
GND	8	9	$\overline{Y6}$

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74VHCT138A
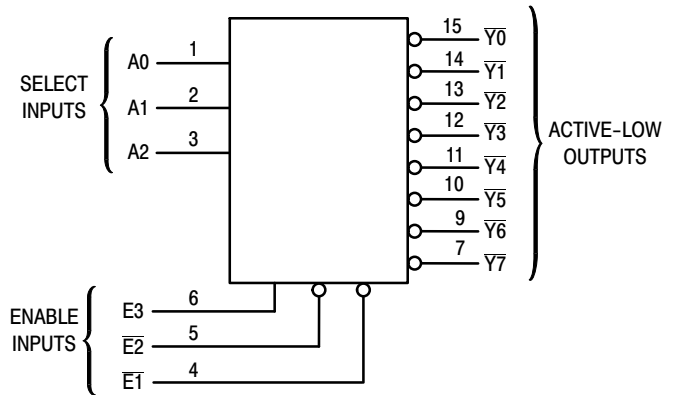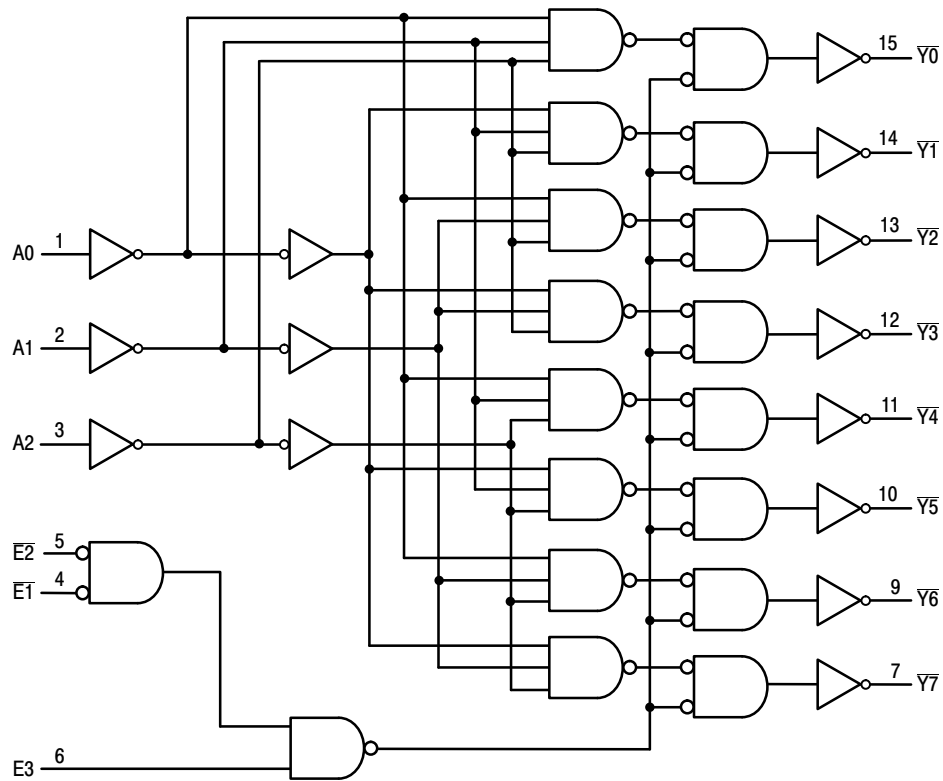
FUNCTION TABLE

Inputs						Outputs							
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

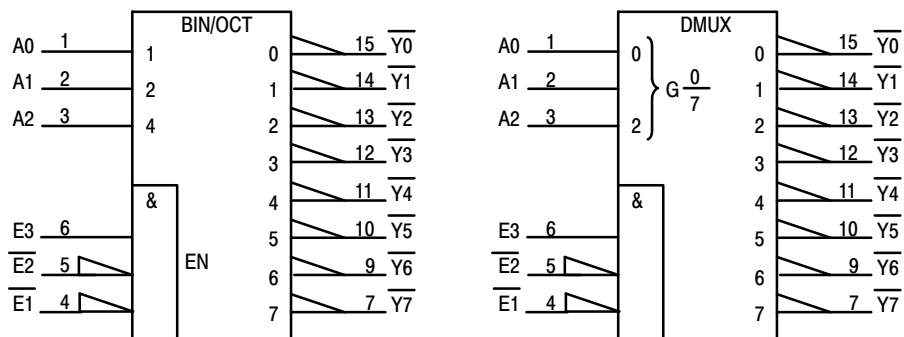H = high level (steady state); L = low level (steady state);
X = don't care

LOGIC DIAGRAM

EXPANDED LOGIC DIAGRAM

IEC LOGIC DIAGRAM

MC74VHCT138A

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
V_{in}	DC Input Voltage		-0.5 to $+7.0$	V
V_{out}	DC Output Voltage	$V_{CC} = 0$ High or Low State	-0.5 to $+7.0$ -0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current		-20	mA
I_{OK}	Output Diode Current ($V_{OUT} < GND$; $V_{OUT} > V_{CC}$)		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†		500 450	mW
T_{stg}	Storage Temperature		-65 to $+150$	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
†Derating – SOIC Packages: -7 mW/°C from 65° to 125°C
TSSOP Package: -6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		3.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage	$V_{CC} = 0$ High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 5.0V \pm 0.5V$	0	20	ns/V

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

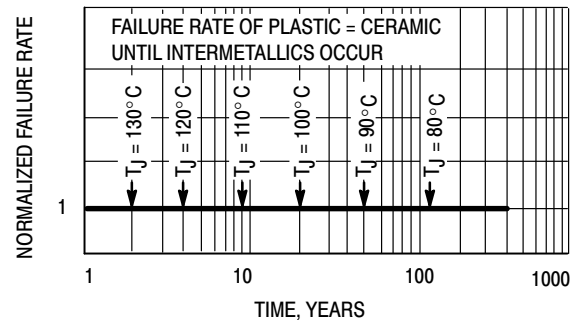| Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Figure 1. Failure Rate vs. Time
Junction Temperature

MC74VHCT138A

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \leq 85°C$ Min	$T_A \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50$ μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			4.0		40.0		40.0	μA
I_{CCT}	Quiescent Supply Current	$V_{IN} = 3.4$ V	5.5			1.35		1.50		1.50	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5$ V	0.0			0.5		5.0		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = \leq 85°C$ Min	$T_A = \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Y	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF		9.5 10.8	14.5 15.5	1.0 1.0	16.0 17.0	1.0 1.0	16.0 17.0	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF		7.6 8.1	10.4 11.4	1.0 1.0	12.0 13.0	1.0 1.0	12.0 13.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input E3 to Y	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF		9.7 9.5	13.0 14.0	1.0 1.0	14.5 15.5	1.0 1.0	14.5 15.5	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF		6.6 7.1	9.1 10.1	1.0 1.0	10.5 11.5	1.0 1.0	10.5 11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input $\overline{E1}$ or $\overline{E2}$ to Y	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF		10.1 9.9	14.0 15.0	1.0 1.0	15.5 16.5	1.0 1.0	15.5 16.5	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF		7.0 7.5	9.6 10.6	1.0 1.0	11.0 12.0	1.0 1.0	11.0 12.0	
C_{IN}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1)	49	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.
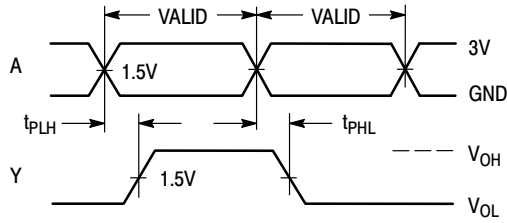
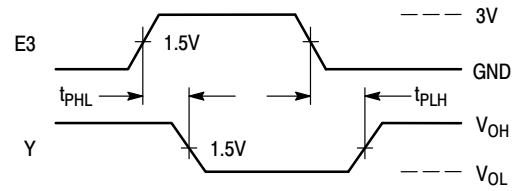## SWITCHING WAVEFORMS

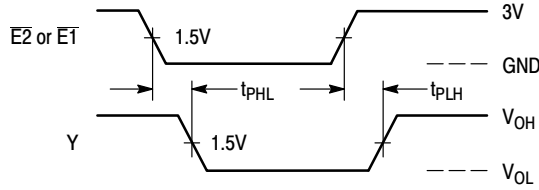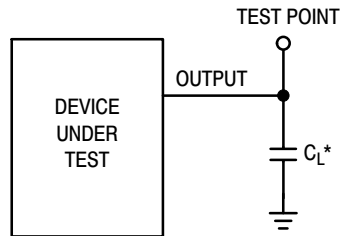**Figure 2.**

Figure 3.

Figure 4.

*Includes all probe and jig capacitance

Figure 5. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74VHCT138ADR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74VHCT138ADTRG	TSSOP−16*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
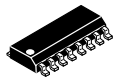
*This package is inherently Pb−Free.

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006
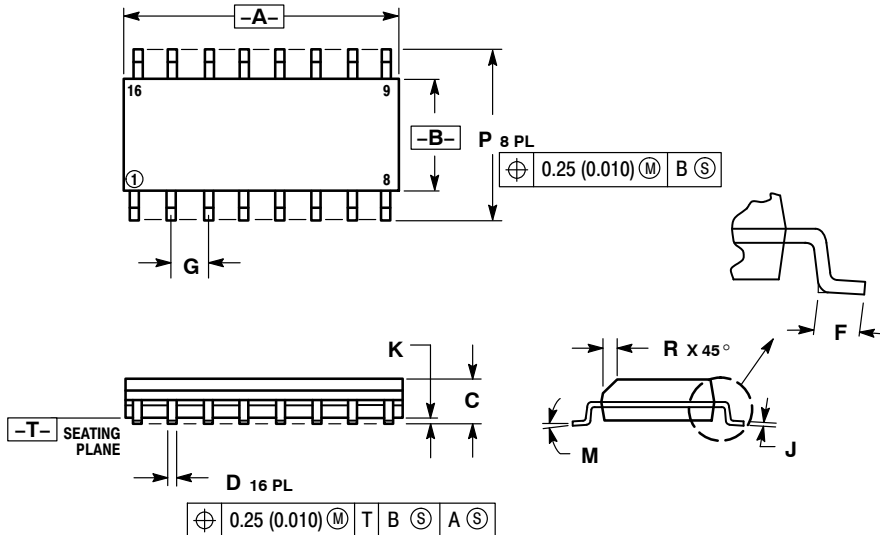
SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

−A−

16   9

−B−   P 8 PL

⊕ | 0.25 (0.010) Ⓜ | B Ⓢ

① 8

G

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

K

C

−T− SEATING PLANE

D 16 PL

R X 45°

F

M   J

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT

8X
6.40

16X 1.12

1   16

16X
0.58

8   9

1.27
PITCH
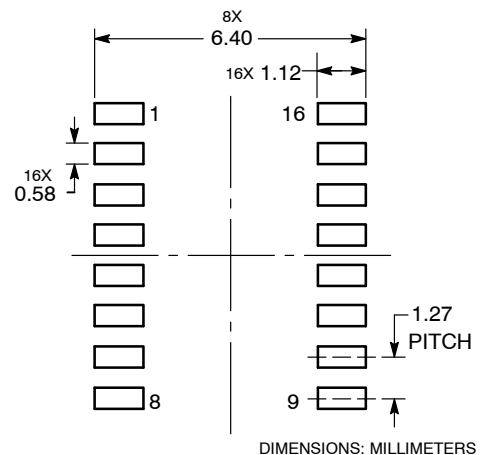
DIMENSIONS: MILLIMETERS

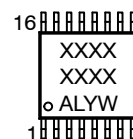| DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16		PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®
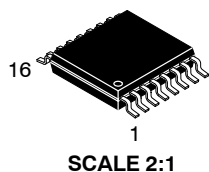
TSSOP−16
CASE 948F−01
ISSUE B

DATE 19 OCT 2006
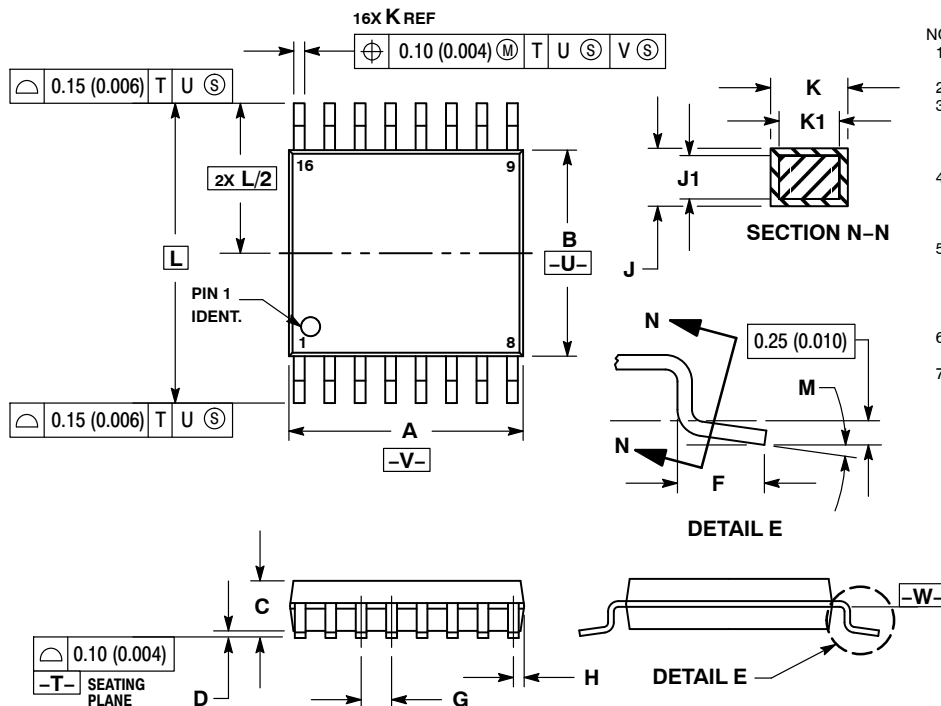
16

1

SCALE 2:1

16X **K** REF

⊕ | 0.10 (0.004) (M) | T | U (S) | V (S)

| 0.15 (0.006) | T | U (S)

2X **L/2**

L

PIN 1
IDENT.

| 0.15 (0.006) | T | U (S)

A
−V−

16   9

B
−U−

1   8

K
K1

J1

J

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

C

| 0.10 (0.004)

−T− SEATING
PLANE

D

G

H

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS
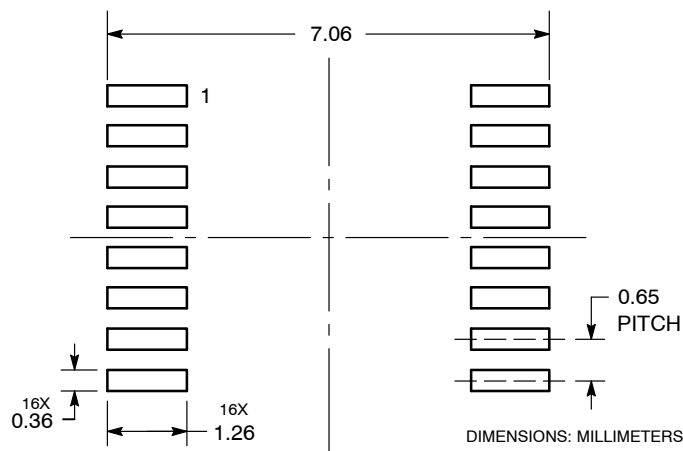
GENERIC MARKING DIAGRAM*

16

XXXX
XXXX
ALYW

1

XXXX   = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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PUBLICATION ORDERING INFORMATION

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