Si21662

Dual DVB-S/S2 Digital TV Demodulator

Description

The Si21662 integrates two separate high performance DVB-S, DVB-S2 and DSS digital demodulators into a single compact package for satellite TV standards. Leveraging Silicon Labs' proven digital demodulation architecture, each embedded demodulator achieves excellent reception performance for each standard while significantly minimizing front-end design complexity and cost. Connecting the Si21662 to a dual satellite tuner, results in a high-performance and cost optimized TV front-end solution.

The satellite demodulation functionality allows demodulating widely deployed DVB-S, DIRECTV™ (DSS) legacy standards, and new generation DVB-S2 (AMC compliant) satellite broadcasts. A zero-IF interface allows for a seamless connection to market proven satellite silicon tuners.

Constant Coding Modulation (CCM), QPSK/8PSK demodulation schemes and broadcast profile are the main specifications of the DVB-S2 demodulator. Silicon Labs' innovative LDPC and BCH decoding architecture delivers best-in-class reception while exhibiting low power dissipation.

The Si21662 offers an on-chip blind scanning algorithm for DVB-S/S2 standards. It also integrates two DiSEqC™ 2.0 LNB interfaces for satellite dish control and, for each satellite demodulator, an equalizer to compensate for echoes in long cable feeds from the LNB to the satellite tuner RF input.

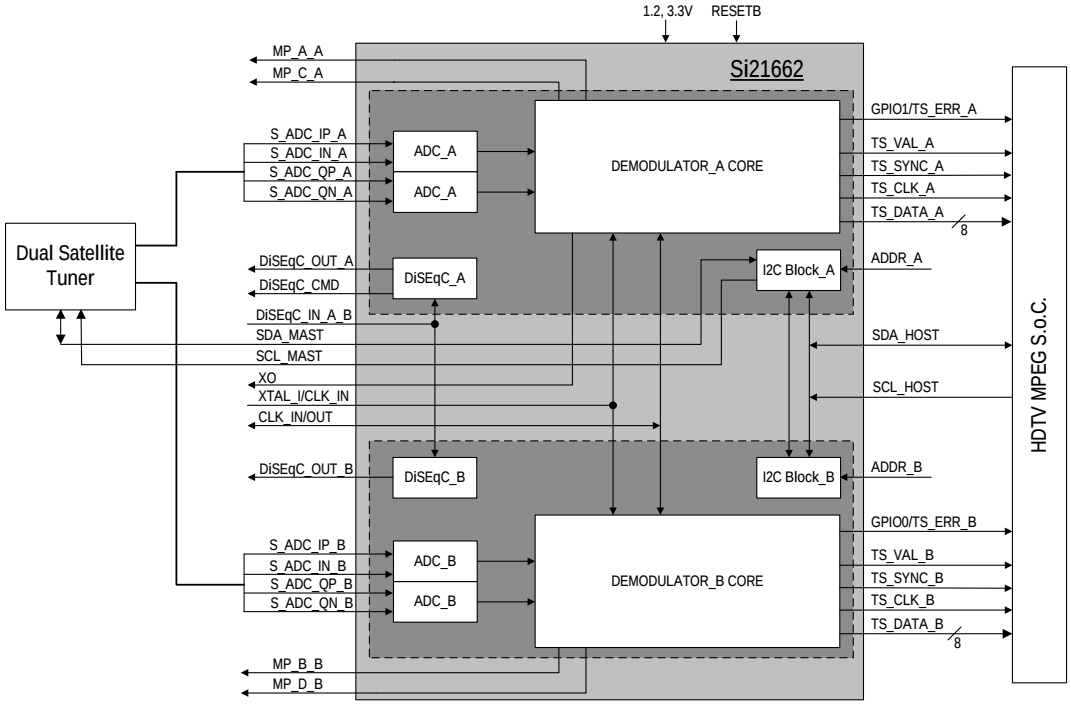
The Si21662 embeds two independent programmable transport stream interfaces which provide a flexible range of output modes and are fully compatible with all MPEG decoders or conditional access modules to support any customer application.

Features

- DVB-S2 (ETSI EN 302 307 and TR102-376)
  - QPSK/8PSK demodulator and FEC decoder
  - Broadcast profile CCM, 64800 bits frame, single TS
  - 1 to 45 MSymbol/s
  - DIRECTV™ AMC compatible
- DVB-S (ETSI EN 300 421)
  - QPSK demodulator and enhanced FEC decoder
  - 1 to 45 MSymbol/s
- Dual DiSEqC™ 2.x interface, Unicable support
- Enhanced immunity to co-channel interferers
- I^2C serial bus interfaces (master and host)
- Dual independent differential ZIF I/Q inputs
- GPIOs and multi-purpose ports (two per demodulator)
- Firmware control for upgradeability
- Separate flexible TS interfaces with serial or parallel outputs
- Fast lock times for all standards
- Only two power supplies: 1.2 and 3.3 V
- 8x8 mm, QFN-68 pin package, Pb-free/RoHS compliant
- Pin-to-pin and API compatible with all dual demodulator family: Si216x2

Applications

- Multi-receiver iDTV: on-board or in a NIM
- Advanced multimedia PVR STBs
- PC-TV accessories
- PVR, DVD, and Blu-Ray disc recorders



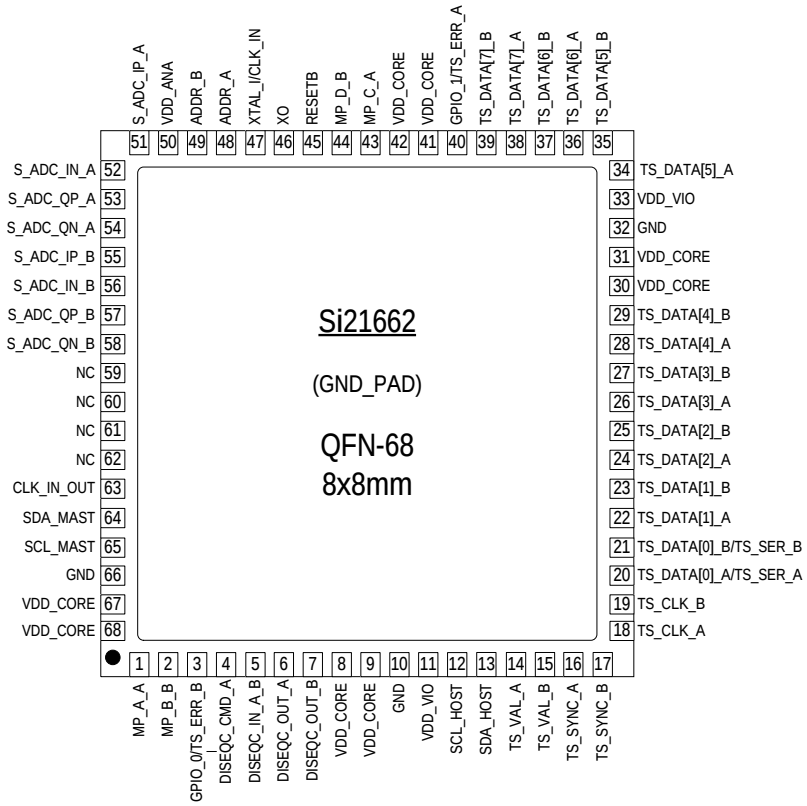
Selected Electrical Specifications

(T_A = –10 to 70 °C).

Parameter	Test Condition	Min	Typ	Max	Unit
General					
Input clock reference		4	—	30	MHz
Supported XTAL frequency		16	—	30	MHz
Total power consumption for each demodulator	DVB-S[1]	—	240	—	mW
	DVB-S2[2]	—	465	—	mW
Thermal resistance (θ_{JA})	4 layer PCB	—	42	—	°C/W
Power Supplies					
V_{DD_VCORE}		1.14	1.20	1.30	V
V_{DD_VANA}		3.00	3.30	3.60	V
V_{DD_VIO}		3.00	3.30	3.60	V

Notes:
1. Test conditions: 30 MBaud, CR=7/8, parallel TS (at QEF: BER = 2. 10^{-4}).
2. Test conditions: 32 MBaud, 3/5 Code Rate, 8PSK, pilots On, parallel TS, C/N at picture failure (PER = 10^{-4}).

Pin Assignments



Selection Guide

Part #	Description
Si21662-B20-GM/R	Dual Digital TV Demodulator for DVB-S/S2, 8x8 mm QFN-68